AEC-Q100 Rev. J(1) and sub specs

Ulrich Abelein

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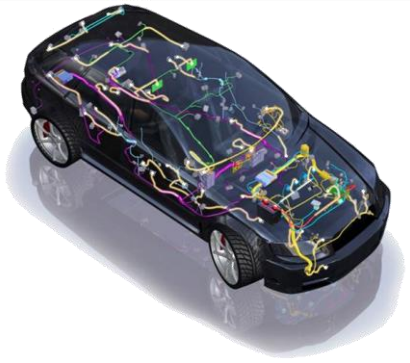
AEC-Q100 Rev. J1

Ulrich Abelein

Motivation

- AEC developed the Excel based AEC-Q100 Rev. A CDC and published it on June 30th, 2025
- The AEC-Q100 main document as Rev. J does not refer to the CDC template but shows a hard copy of it
- Integration of the new CDC needs a change of AEC-Q100 Rev. J
- As there is no substantial change to any other part of the spec the revision is considered minor and published as Rev. J1



Changes in Rev. J1

- **Some typos and company names corrected**
- **Appendix 2 now with reference to new CDC template**

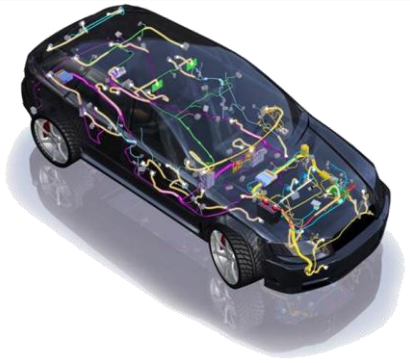
Appendix 2: Q100 Certification of Design & Construction (CDC)

When documenting a device has met the requirements of AEC-Q100, it is necessary to provide information on the construction and processing of the device. This information is provided in a CDC (Certification of Design & Construction) document. The CDC details the major manufacturing locations, material components and design characteristics.

AEC has developed a template that includes all information related to a component containing one or more integrated circuits (ICs). This template can be downloaded from the AEC website at http://www.aecouncil.com. While use of this template is not required, it is recommended as it contains all requested information as well as instructions, guidelines and helpful information (see comments in template for details). If this template is not used, it is up to the IC supplier to provide the information in an alternate format.

All fields in the template should be filled out as completely as possible. Each data entry has information on the format of the field and how each entry should be completed. If a field cannot be entered because it does not apply, it should be filled as "Not Applicable". If a field cannot be filled due to proprietary or other reasons, it should be filled as "Unavailable"

The top portion of the "Overview – Signature" page of the CDC Template is shown below:



AEC-Q100 sub specs

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OVERVIEW – Q100 sub specs under revision

Spec	Rev.	Release Date	Title
AEC-Q100-001	C	1998-10-09	WIRE BOND SHEAR TEST
AEC-Q100-002	E	2013-08-20	HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST
AEC-Q100-004	D	2012-08-07	IC LATCH-UP TEST
AEC-Q100-005	D1	2012-01-09	NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST
AEC-Q100-007	B	2007-09-18	FAULT SIMULATION AND FAULT GRADING
AEC-Q100-008	A	2003-07-18	EARLY LIFE FAILURE RATE (ELFR)
AEC-Q100-009	B	2007-08-27	ELECTRICAL DISTRIBUTIONS ASSESSMENT
AEC-Q100-010	A	2003-07-18	SOLDER BALL SHEAR TEST
AEC-Q100-011	D	2019-01-29	CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST
AEC-Q100-012	-	2006-09-14	SHORT CIRCUIT RELIABILITY CHARACTERIZATION OF SMART POWER DEVICES FOR 12V SYSTEMS

AEC-Q100-012 Rev. A
AEC-Q101-006 Rev. A

Ulrich Abelein

Motivation

- **Wire harness complexity was limited when the spec was developed (2006).**

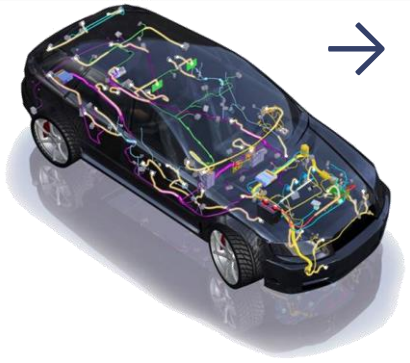
→ **Limited number of test conditions sufficient to cover the majority of possible conditions.**

- **Examples of boundary conditions leading to increased short circuit condition variability in vehicles:**
  - Increased number of semiconductor switches in power distribution
  - New E/E architectures, e. g. zone architectures
  - Fuse replacement by semiconductor switches

- **Conclusion: Rework of test procedure and or conditions necessary.**

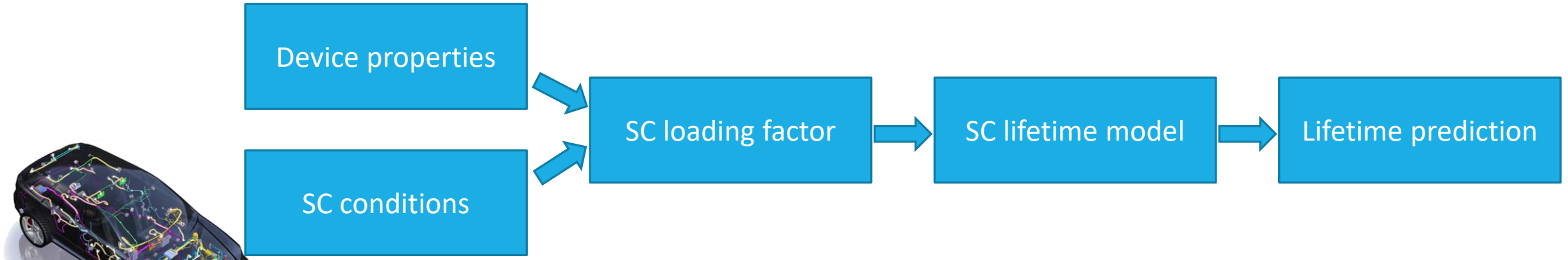
Status

- **81 change requests received**
- **Major items under discussion:**
  - Introduction of other voltage classes (24 V / 48 V)
  - Introduction of “short circuits while ON”
  - Test temperature requirements
  - Inconsistent grading (Grade B logically non existent)
  - Variable Short Circuit Conditions
    - → driven by eFuse applications
    - → introduction of SC lifetime modelling



SC lifetime modelling

- **Under discussion as alternative but not replacement of predefined test conditions**
- **Detailed description of requirements on model creation, application and reporting**
- **Intention to cover wide range of short circuit condition**



AEC-Q100-001 Rev. D
AEC-Q101-003 Rev. B

Claudia Palumbiny / Florian Staub

Motivation

"Problem Statement":

The current spec(s), Q100-001 and also Q101-003, do not address Cu wire bonding.

However, this is the state of the art wire bond interconnect in automotive today.

- **Integrate Cu wire bonding**
- **Reference test method to JESD22-B116**
  - **Define shear force limits in AEC spec(s) based on JESD47**

Strategy

Make use of available knowledge in standards.

Test Method

- JESD22-B116

Shear force limits

- JESD47

Q100-001 & Q101-003 identical – merge rework of both standards.

Note: Approach has been already discussed during Q006 development

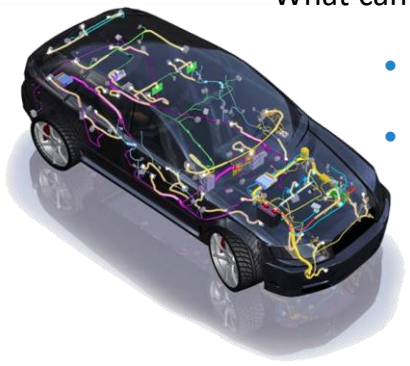
Discussion Status

Task Collection

- **MOU with JEDEC**
  - **for sharing of reference standards & their updates**
- **Shear force limits: get transparency → overview table incl. data sources**
  - **what can be referenced directly**
  - **what needs an adaption**
  - **what needs an additional specification**
  - **provide reasoning for all deviation from JESD47 limits**
  - **clarity on data: premold, 0h/ post decap, ...**
  - no limits for overpad metallization in JESD47
- **shear code assessment**
  - pass/ observation/ poor test setup?
  - cratering?
  - failure modes of B116
  - What can be take over from JESD47?

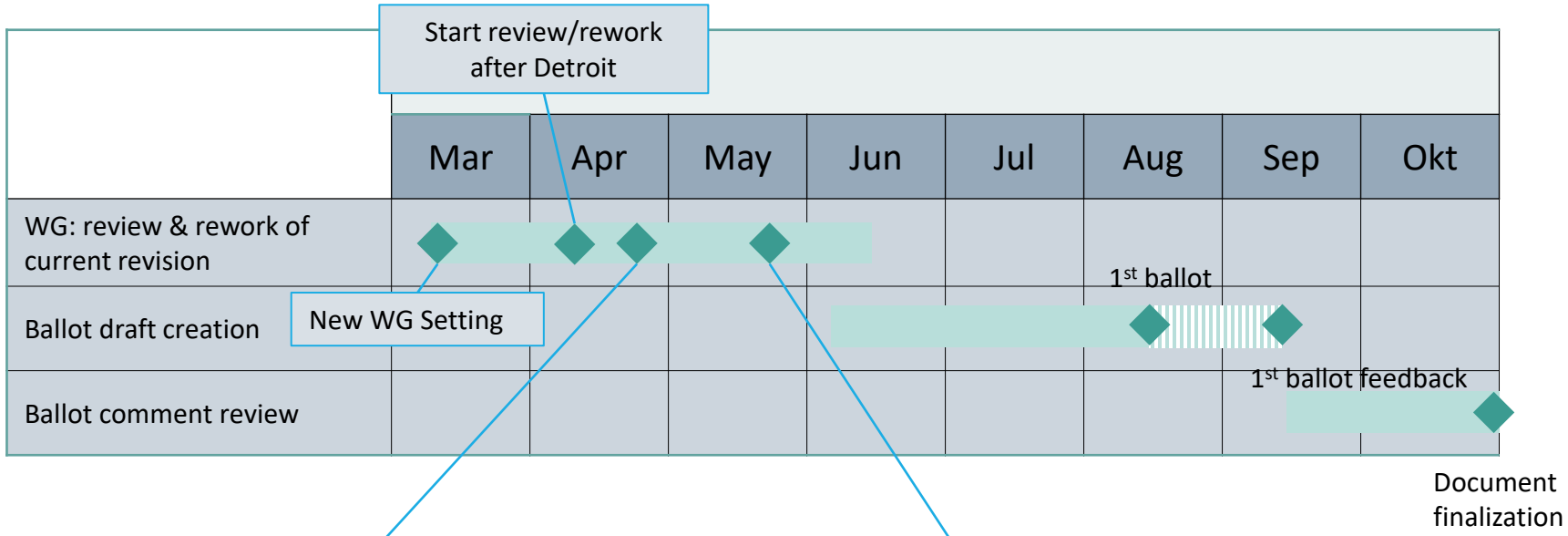
Triggered. Pending release.

Next step for April ´26



- **copyrights for pictures etc.**
- **Publishing**
  - Option1: publish in one central document (Q00x): If the final scope is to have an AEC spec and not refer entirely
  - Option2: publish in two identical documents (Q100-001 & Q101-003): If the final scope is to remove the specs, first keep the two documents

Best case timeline (if no set of new requirements needs to be prepared)



AEC-Q100 ESD/LU Test Methods

Greg O’Sullivan

Motivation

- **AEC-Q100 ESD/LU Test Methods in AEC deviate from current ESD roadmap**
- **AEC Q100-011 Rev D / 2019 CDM - IC Semiconductors**
  - Rev D aligned to JS-002 method, with various exceptions / additions detailed (Corner balls, 3 zaps, …)
  - Contact CDM test method accommodation roadmap for <200V T.C. sensitive devices.
  - 1 Zap vs 3 Zap harmonization.
  - Opportunities to further align, simplify, and adapt to keep up with ESD roadmap, including align on report format improvements (JEP178).
- **AEC Q100-002-rev E / 2013 HBM - IC Semiconductors**
  - Rev E aligned to JS-001 test method, with various exceptions / additions detailed.
    - JS-001 has had the following revisions: 2014, 2017, 2022, 2023, 2024 after rev E.
    - Opportunities to further align, simplify, and adapt to keep up with ESD roadmap, including align on report format improvements (JEP178).

Motivation

- **AEC-Q100 ESD/LU Test Methods in AEC deviate from current ESD roadmap**
- **AEC Q100-004 Rev D / 2012 LU - IC Semiconductors**
  - JESD78 foundational spec has had multiple revisions since 2012, (currently rev F, 2022)
    - JESD78 has absorbed / aligned on many of the Q100-004 ‘Exceptions’ of Rev D: 2012.
      - E-Test, MSV Topics. Clamping voltages. Reporting requirements.
      - Lots of new device examples to help guide correct testing for difficult devices, charge pumps,
    - A comprehensive Technical report (Users Guide) is also in progress with the JESD78 Working Group.
      - Opportunity to engage any remaining concerns with JESD78 working group.

Next steps

- Formation of a task group to collect and review change requests on AEC-Q100 ESD/LU specs
- Plan is to handle all 3 specs in one task group as most likely same experts will be involved
- Start work on new revisions of all three specs
- If you are interested in collaborating please contact

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Scott Ward: s-ward@ti.com

Ulrich Abelein: ulrich.abelein@Infineon.com

NOTE: Separate email with call for change requests and contribution will go to the TC members.

Any questions?