AEC Q100-005

Sumit Tayal

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Scope of the Specifications

- **Adding SSD and mNAND products along with existing NOR and NAND standalone NVM devices.**
- **Non charge based NVM memories: Eg. FeRAM, MRAM, RRAM, PCM also known as 'Emerging Memories' to be added to the specifications**
  - The emerging memories, may be defined as SET and RESET or WRITE0 and WRITE1 instead of conventional '0' and '1' for NAND / NOR.

Challenges

- There is no well defined JEDEC specifications for individual emerging memories.
- Some of the tests specifications are not applicable for emerging memories vs conventional NVMs

Proposal

- **Will propose to have the main spec Q100-005 out for ballot within this year and continue working on ‘emerging memories’ in new appendix.**

Support

- **Members needed for with experience in the following:**
  - MRAM: Support identified from NXP
  - RRAM: Support identified from NXP
  - FeRAM: ?
  - PCM: ?

  - Need more members from Tier 1s who have experience on emerging memories. Presently: Bosch, ZF and Aumovio