

DCI-CBE: A Test Method for ESD Evaluation of an Electronic Module Edge Connector Performance.

Greg O'Sullivan

Senior Member of Technical Staff

(Email: GOSULLIVAN@MICRON.COM)



Automotive: Memory and storage are everywhere

Centralized storage

- NAND (ultra-endurance SSD)
- DRAM
- MCP

Powertrain

- NOR
- DRAM
- NAND (SLC NAND)

Enriched cabin

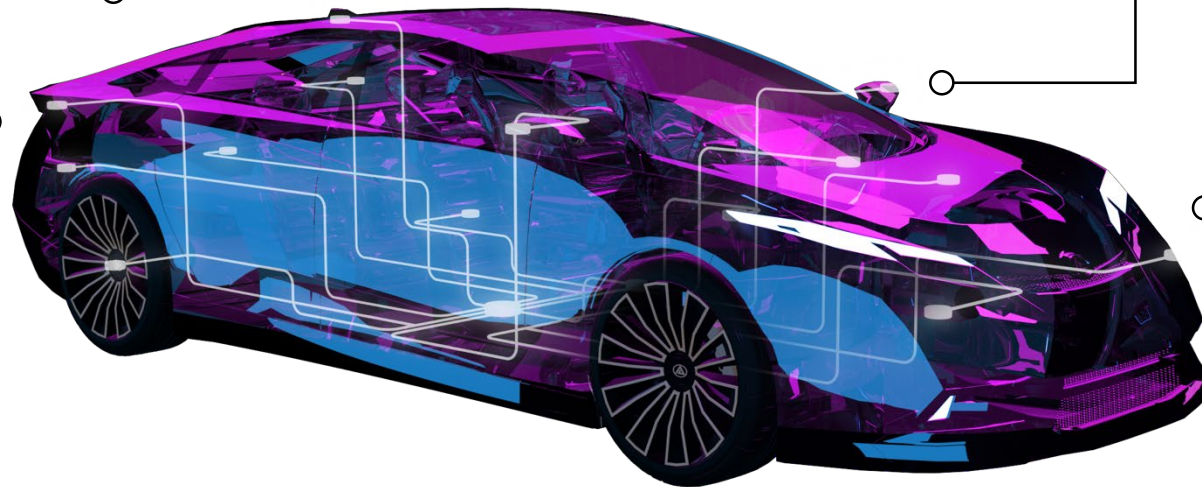
- DRAM
- NAND (e.MMC/UFS/SSD)
- NOR
- MCP

Connected

- e.MMC
- NOR
- MCP

ADAS L2-L5

- DRAM
- NAND (e.MMC/UFS/ultra-endurance SSD)
- NOR
- MCP



Presentation Agenda

- Charged Board Event – TR25
- Motivation – Module ESD Trends
- Measurements (C_{DUT} , CDM)
- Direct Charge Insertion (DCI-CBE)
- Manual Test Method Development
- Automated Tester
- ESD Hardening

Foundations: CBE – Charged Board Events (TR25.0-02-23)

7.0 SUMMARY

Real-world charged board events are case-specific, where the design of the DUT, discharge contact points, and discharge environment can vary. Therefore, CBE test setups need to be tailored for each discharge scenario. This requires knowledge of DUT electrical design, electrostatic charges found in the environment, and how the DUT and other conductive objects come in contact. This may require additional on-site checks and tailored measurements to specify a realistic CBE set up on a test bench. This can make CBE testing complicated when compared to standardized IEC 61000-4-2 system or component level HBM and CDM tests.

5.1 CBE Stress Scenario

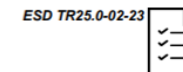
CBE characterization evaluates the ESD sensitivity of electronic assemblies with selected discharge scenarios. These scenarios can be selected based on known or estimated ESD risks and typical contact points on the device under test (DUT) [1–11]. Typical contact points for CBE characterization are:

- high-speed electrical interfaces, such as antenna pads and connector pins
- test and programming interfaces
- cable connection interfaces
- **signal interfaces between sub-assemblies**
- power or ground planes with powered systems
- other product internal interfaces that are accessible only during handling, final assembly, testing, and programming

Memory Module Edge Connector +
Motherboard Socket

The following characterization methods describe test setups that can be chosen based on the type of DUT, accessibility of the test points, availability of tools, and characteristics of the discharge path.

- **Direct Charging and Discharging Method** DCI-CBE
- Field Induction Method
- **CDM Tester Method** CDM-CBE
- Field Collapse Event Method
- Step Response Analysis



*For Electrostatic Discharge
Sensitivity Testing*

*Charged Board Event (CBE)
Characterization Methods for
Electronic Assemblies*

Authors:
**Working Group 25.0,
Device Testing - CBE**
EOS/ESD Association, Inc.

*EOS/ESD Association, Inc.
218 West Court Street
Rome, NY 13440*

Published September 21, 2023

Copyright 2025 by EOS/ESD Association, Inc. Licensed, by agreement, for use by Micron.
No other reproduction or transmission in any form is permitted without written permission of the ESDA.
For inquiries or to report unauthorized use, contact info.eosesda.org.

ESD TR25.0-02-23

5.2 Direct Charging and Discharging Method

5.2.1 Initial Conditions

An example test setup and simplified equivalent circuits are shown in Figures 1 and 2.

DUTs should be completely neutralized before charging. The purpose of neutralization is to ensure that all materials of the DUT have the same initial electrical potential. This can be done by grounding the power or ground planes of the DUT. An ionizer can be used to neutralize charges on dielectric surfaces.

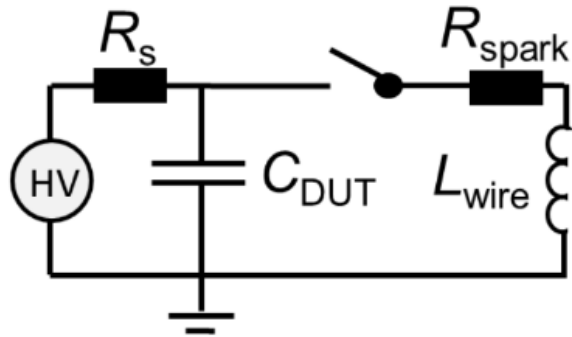


Figure 1: A Simplified CBE Discharge RLC Circuit

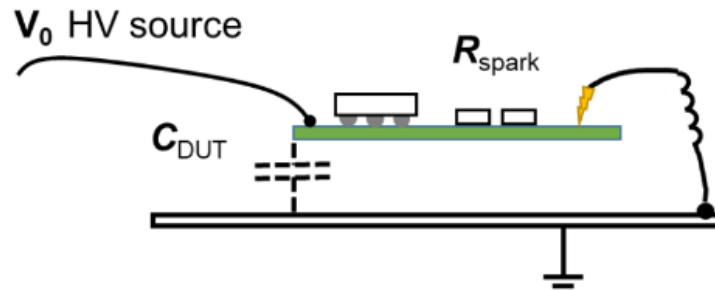


Figure 2: An Example Discharge Setup

Charging:

$$Q_{DUT} = C_{DUT} * V_o$$

C_{DUT} = Capacitance of PCB

V_o = Voltage applied to PCB

$$E_{total} = \frac{1}{2} C_{DUT} * V_o^2$$

Q_{DUT} = Total DUT Charge

E_{total} = Total DUT energy

Discharging:

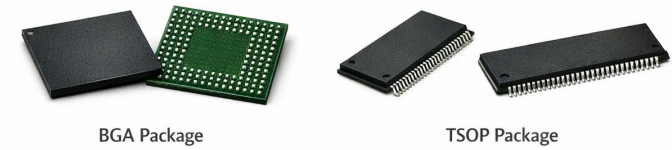
$$i(t) = \frac{V_o}{L\omega} e^{-\left(\frac{tR}{2L}\right)} \sin(\omega t), \quad (1)$$

$$\omega = \sqrt{\frac{1}{LC_{DUT}} - \frac{R^2}{4L^2}} \quad \text{and for overdamped, } \omega = \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$$

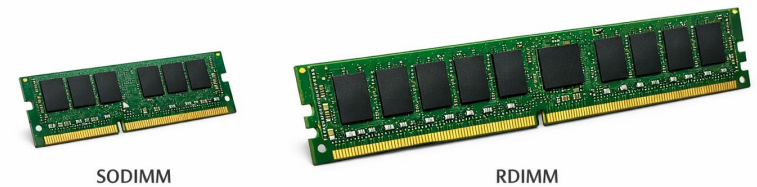
Motivation – Module ESD Risk Increased with DDR5

- Faster devices have lower ESD fail thresholds [5]
 - DDR4 Components: JEDEC CDM Target > 500V
 - DDR5 Components: JEDEC CDM Target > 250V
- CDUT Module >> CDUT Component
- Component ESD testing / limits are well defined (JS-002)
- PCB (Module) ESD testing method / limit are not defined
- ESD risks exist for customers during PCB handling + insertion
 - Customers need to manage risks with effective ESD control measures.
- Module vs glove material tribo-charging experiments
 - Base material has large effect. Ex: Polyurethane vs Nitrile
 - Considerable Supplier variation: charging + resistance over time.
- Can PCB / module edge connector design be improved (ESD hardened)?
- How would you test / measure effectiveness of different designs?

Memory Component Packages



Memory Modules

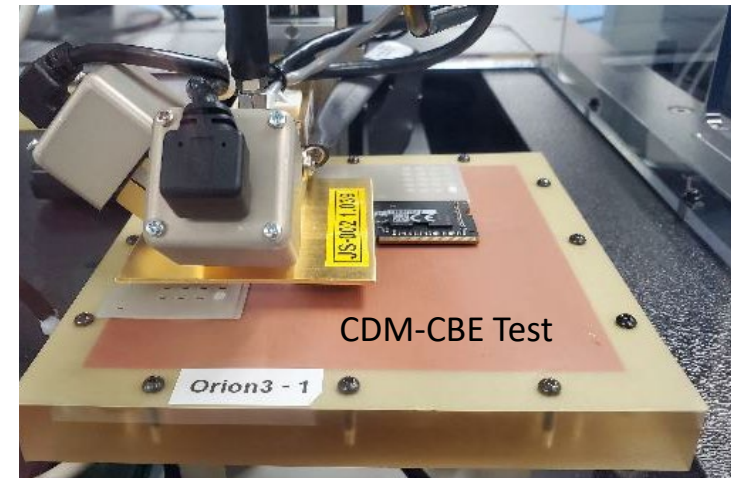
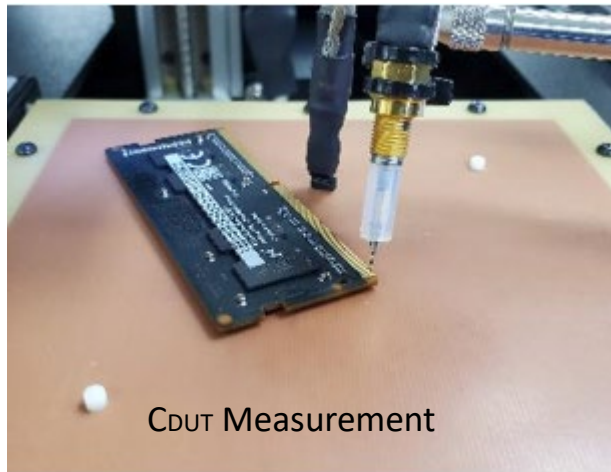
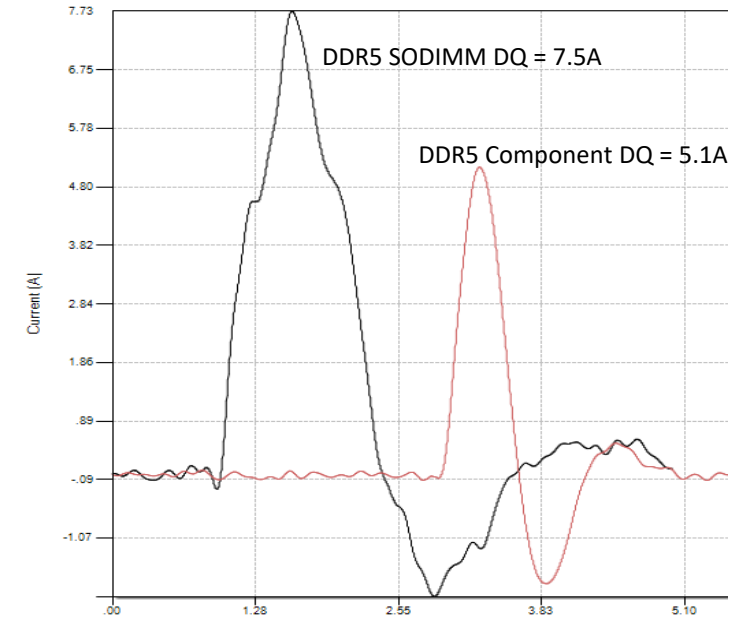
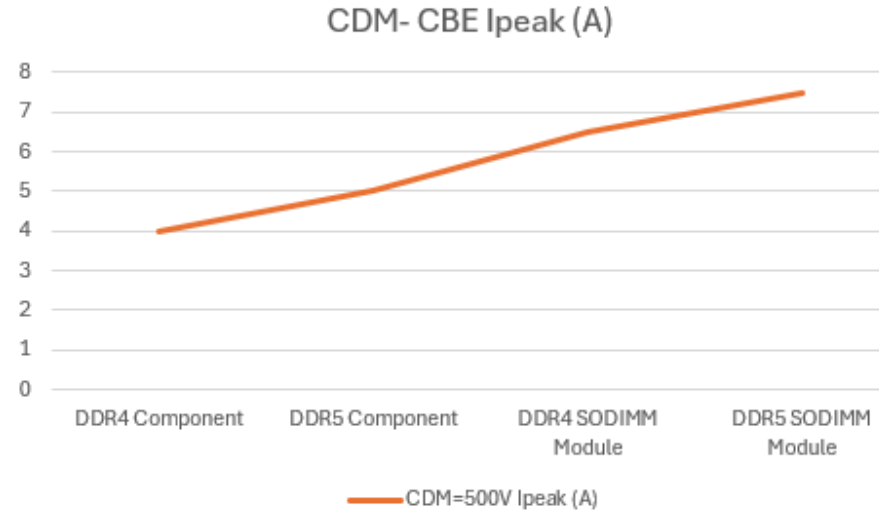
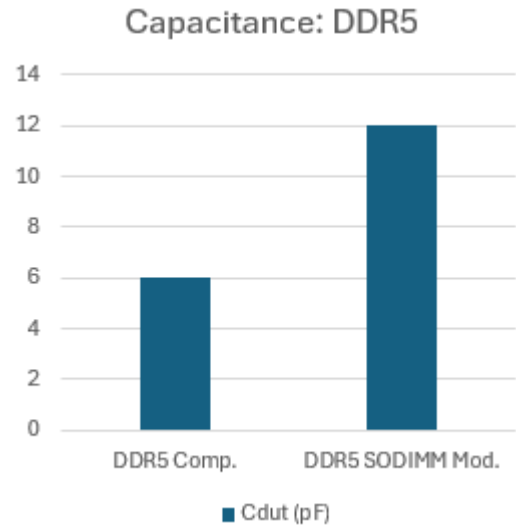


CDM Event Detection Experiment (EMI detector)

Gloved hand insertion into motherboard socket. Ionizer off.

No	Supplier A	Supplier B	Supplier C	CDM Limit
Slot 1	0V	212V	0V	200V
Slot 2	575V	161V	109V	200V
Slot 3	0V	0V	0V	200V
Slot 4	0V	188V	103V	200V
Slot 5	493V	159V	126V	200V
Slot 6	0V	110V	113V	200V

Measurements Confirm Motivations



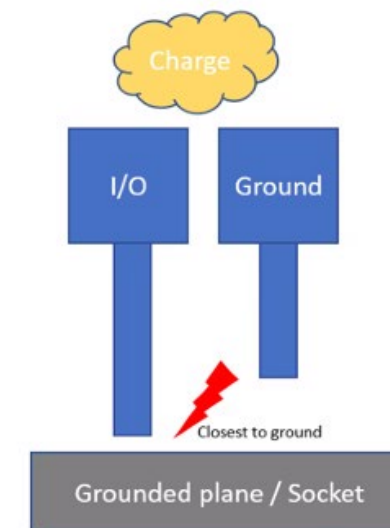
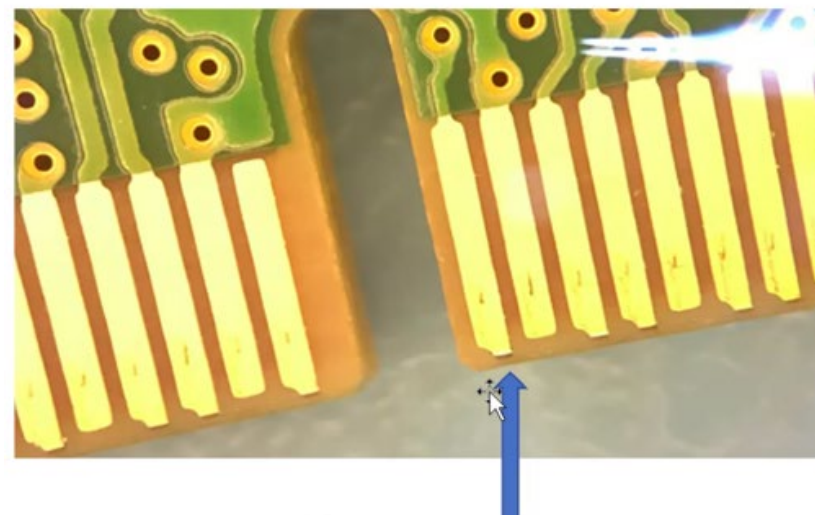
Need: A Module Direct Charge + Grounded Insertion CBE Test → DCI-CBE

How can PCB designs be 'ESD Hardened'?

- Contact First Principal → Discharge to VSS Pin not Signal Pin
 - Extend tie-bars on all VSS pins?
 - Extend VSS Pins / Etch back Signal pins
 - Tie-bars have their own issues
 - JEDEC MO limits / metal keep out zone

How to verify edge connector design changes are effective?

- Simulate charged module ESD events on insertion
- Repeated charge / insertion cycles at a given voltage
- Tribo-charging is not precise
- Direct charging allows precision and repeatability
- Check for damage after every stress level
- Identify at risk pins based on module + socket design



DCI-CBE: Test Development Considerations

1. Charging Control

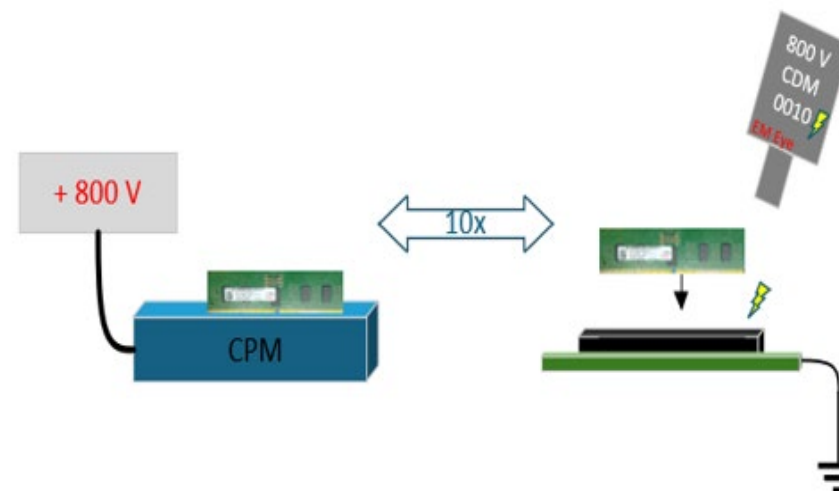
- Maximize Module Capacitance (C_{DUT}) (need ground reference plane)
- Control Module Charging at slow rate
- Avoid charge dissipation before insertion

2. Measurement / Verification

- EMI Event Detectors to confirm ESD events
- Faraday Cup can measure charge on Module
- O-Scope can capture WF

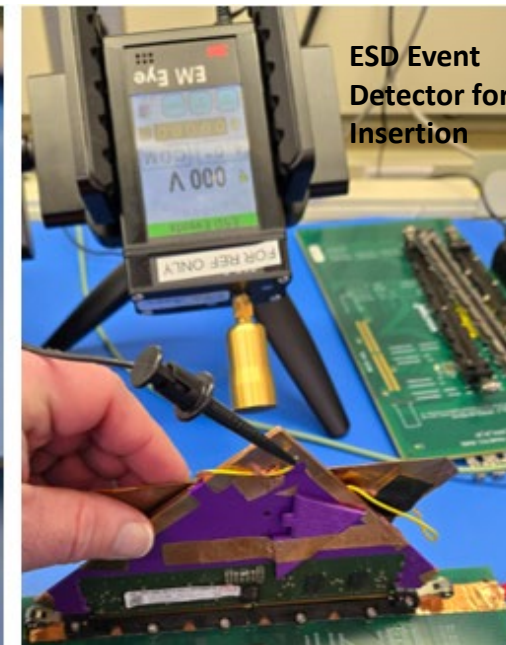
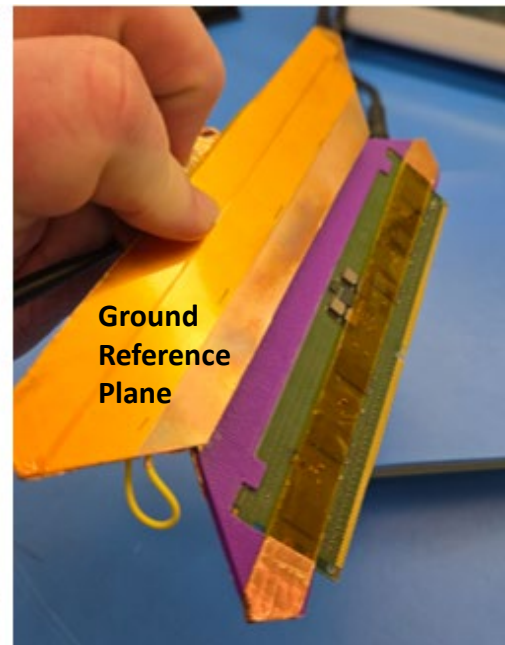
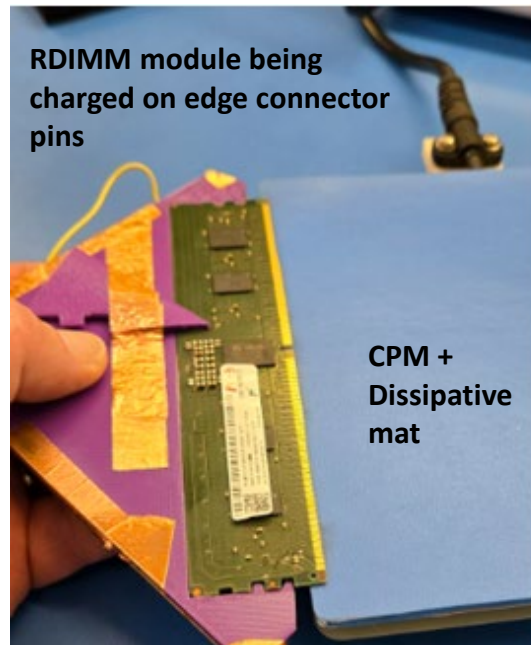
3. Repeatability and Safety

- ESD Failure threshold can be monitored on a different tester
- Manual test setup can provide learnings, proof of concept, and debug
- Automation required for good repeatability and limiting variable

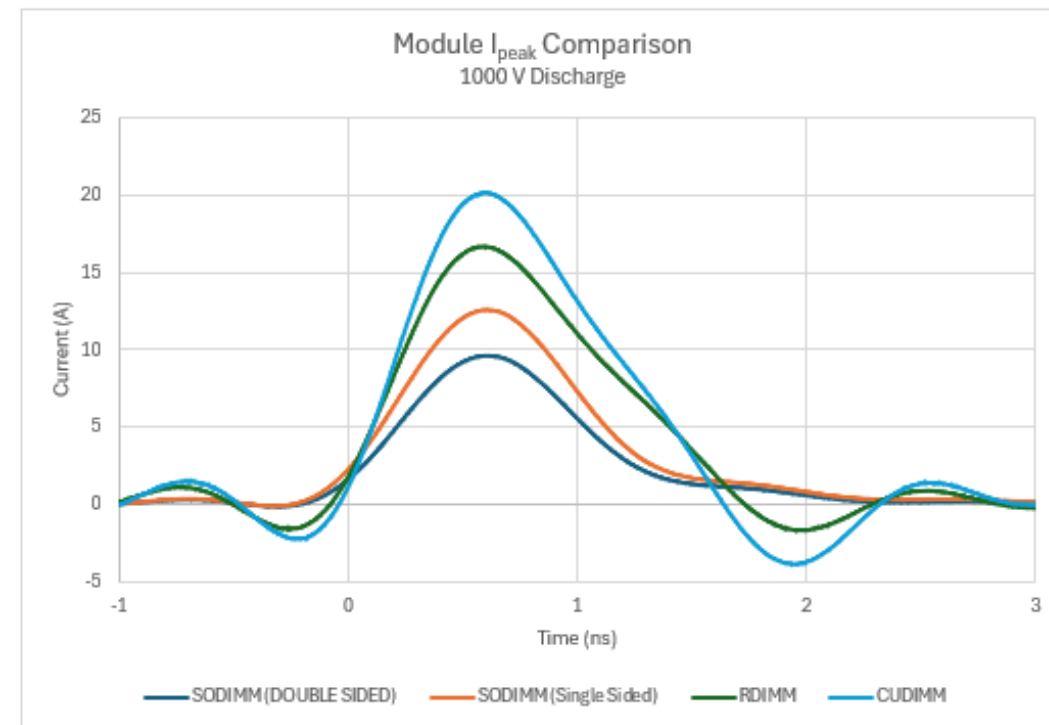
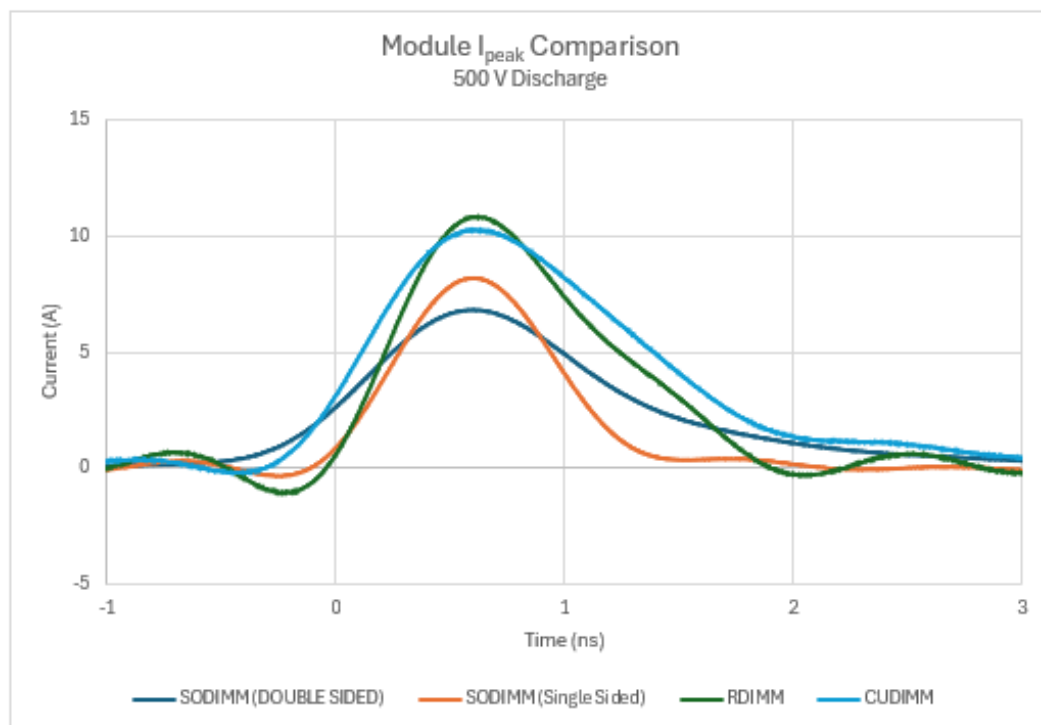


Test Development: Manual Charge/Discharge Setup

- Charge Plate Monitor (CPM) – delivers a safe voltage source 100-1000V
- Insulative material 3D-printed jig to hold module during charging and discharging
- Dissipative ESD blue mat (RTG $\sim 10^9 \Omega$) for slow direct charging CPM to edge connector
- Ground plane below module to create sufficient module capacitance
- EM Eye ESD event detector for approximate DCI-CBE event magnitude



DCI-CBE Charged Module Waveform Comparison



- Charged using hand test fixture (manual DCI-CBE)
- VSS edge pin discharged through CDM head
- I_{peak} : Scales with C_{DUT} and module form factor.
 - CUDIMM ~ RDIMM \gg SODIMM
 - Single Vs Dual sided modules

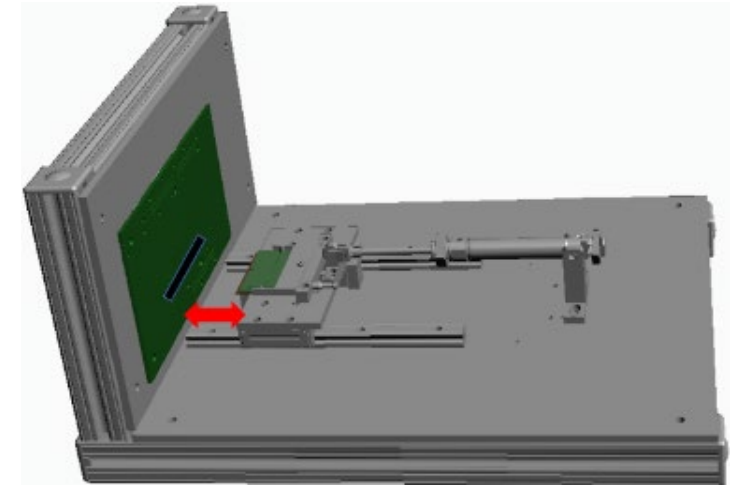
Automated DCI-CBE Tester Design and Build

Design Goals

- Maximize module DUT capacitance.
- Increase the maximum Vstress range and accuracy
- Eliminate human variables which may favor insertion side of module or charge time.
- Allow for some controlled insertion variability.
- Allow for large number of insertion tests to generate high volume data using minimal samples.
- Ensure safe operation by design, given high test voltages

Outcomes

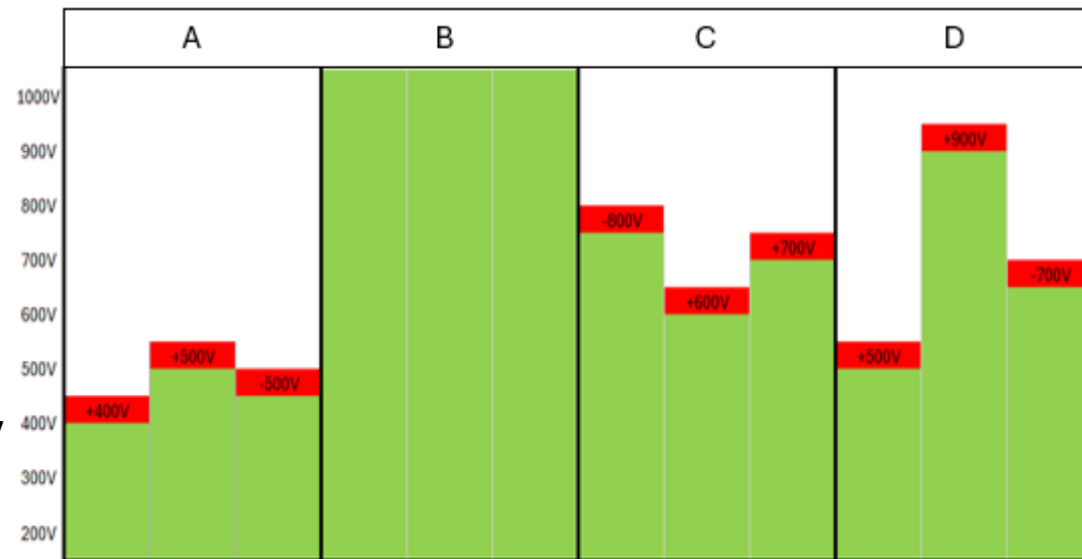
- Test capacitance close to CDM-CBE test setup
- Voltage accuracy greatly improved.
- Voltage range extended from 1000V(CPM max) to 2200V
- Configurable for different module form factors



Double Sided SODIMM Module Charged to 1000 V (Voltage source set to 1000V) Measured using Faraday Cup + Nano Coulomb Meter (20nC Range)				
Test Method	Voltage Source	Voltage @ Charge Bar/Plate	Charge – Faraday Cup (nC)	Calculated Capacitance (pF)
Manual DCI-CBE	CPM	1251	17.18	13.73
Automated DCI-CBE	CPM	1251	15.87	12.69
Auto DCI-CBE	Custom	1002	12.26	12.24
Measured LCR – CDM Tester		--	---	12.30

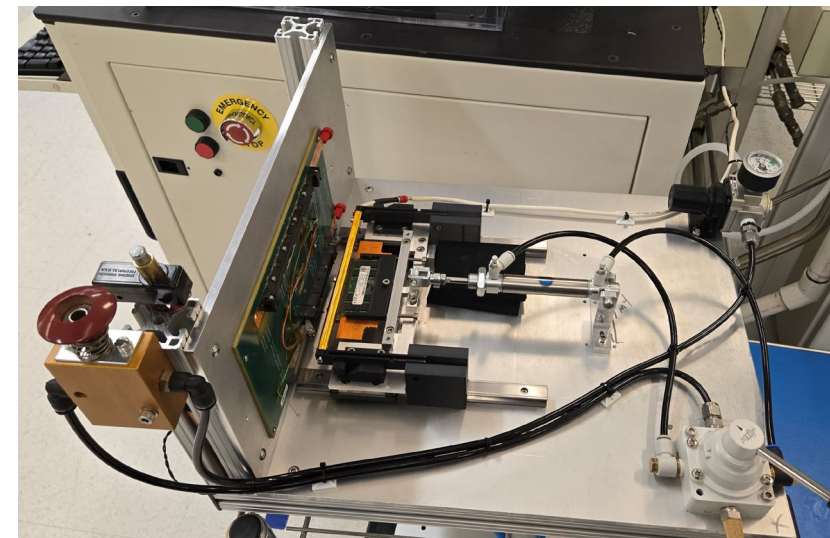
DCI-CBE Testing in Operation

- Different module edge connector designs were supplied and tested for SODIMM, CUDIMM, and RDIMM form factors
- Manual test setup and automated setup generated similar fail levels
- DCI-CBE testing was able to confirm extended VSS lead fingers are the superior design
- Automated testing saved massive test time.
- Module pins at risk of ESD damage were able to be ‘heat-mapped’ in a way that is a combination of risk of discharge + pin ESD sensitivity.



Best Performance
Design B
 All GND Pins Extended with Signal Pins and signal tie-bars recessed.

Worst Performance
Design A
 GND and signal pins same length. Most GND pins without tie-bar.



Video of Automated DCI-CBE Tester During Operation



ESD Hardening

micron[™] **ESD ASSOCIATION** **JEDEC** Global Standards for the Microelectronics Industry **IEC**[™] **Automotive Tier 1 & Tier 2**

SUPPLIER **CUSTOMER**

Effective Communications

ESD Design
ESD Qualification Testing

ESD Safer Materials
Ionizers
\$20.20 Audits

ESD CONTROL SUCCESS

DCI-CBE enables measurable, design-driven ESD hardening

References

1. www.aecouncil.com
2. www.jedec.org
3. www.ESDA.org.
4. [ESD TR25.0-02-23 For Electrostatic Discharge Sensitivity Testing: Charged Board Event \(CBE\) Characterization Methods for Electronic Assemblies](#)
5. Micron Technical Note. [TN-00-38: Anticipating ESD Technology Roadmap Trends.](#)
6. ANSI/ESDA/JEDEC JS-002: For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) Device Level
7. Youngbong Han et. al. Proposing a Strategy to Prevent Module-level Charged Device Model Failures in Dual In-line Memory Modules. ESDA 2024 Symposium.
8. JEP175A: Recommended ESD-CDM Target Levels. 4/2022.