

# HVM “Golden Recipe” Methodology for SiC Substrate Qualification Across Suppliers

## Part 2



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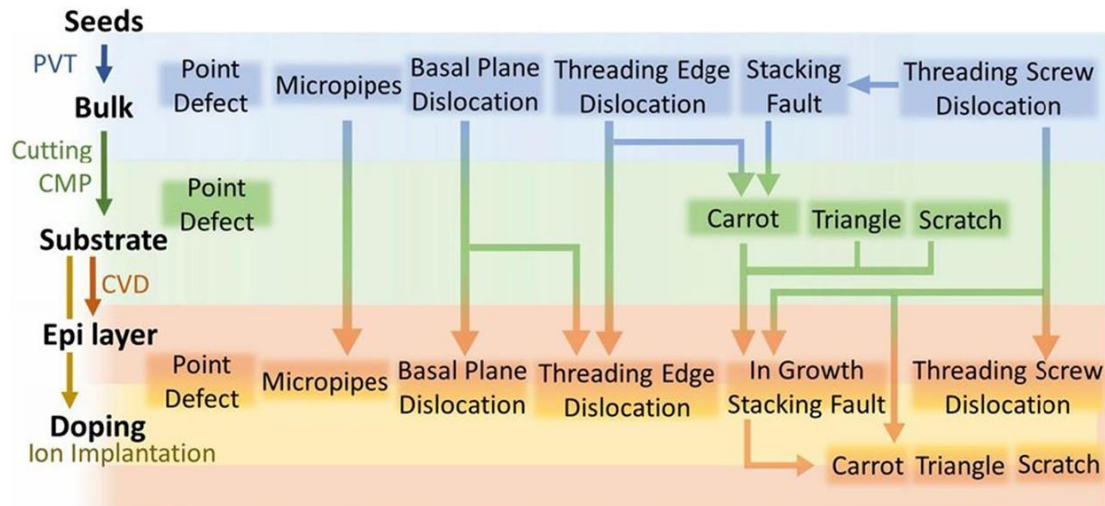


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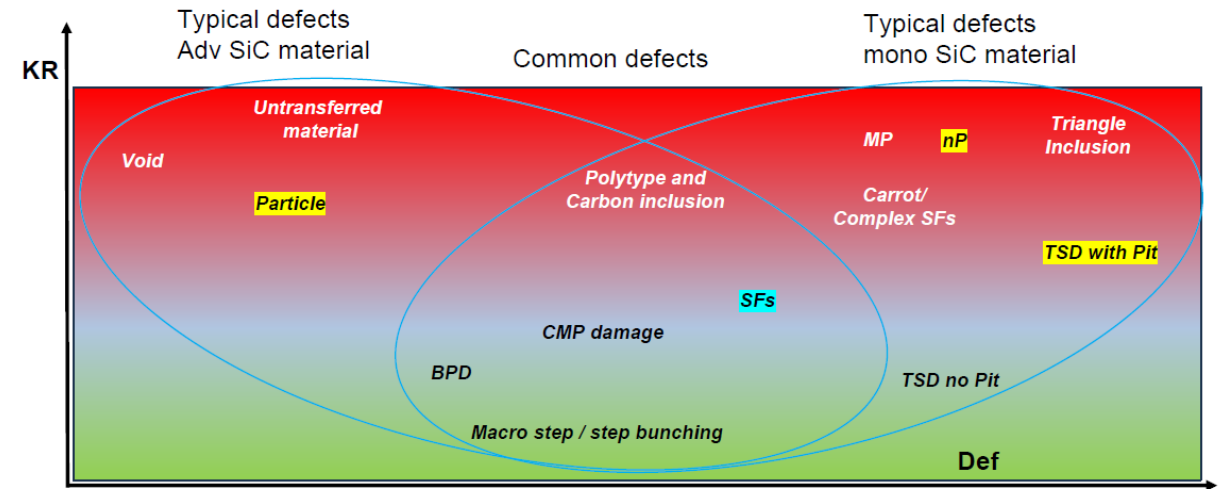
# Agenda

1. Introduction & Problem Statement
2. Data Results and Discussion
3. Conclusions and Next Steps

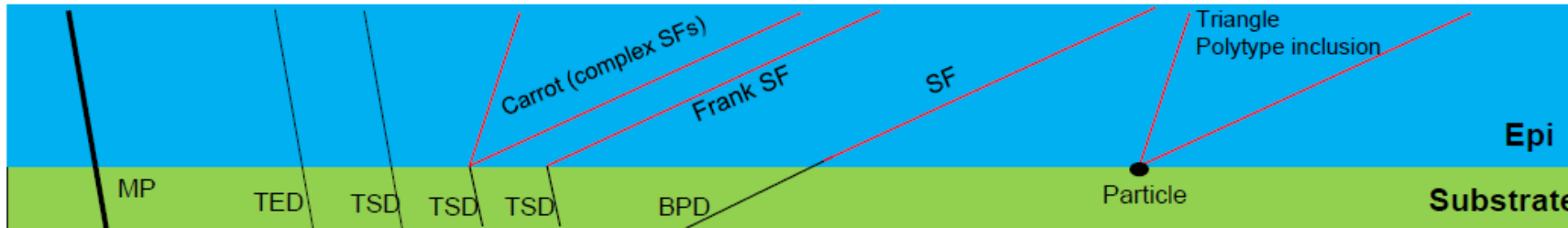
# SiC Substrate Defectivity



Chen et al. Nanoscale Research Letters <https://doi.org/10.1186/s11671-022-03672-w>,



N. Piluso et al. - Influence of starting material on final device in SiC power technologies - IRPS 2025,

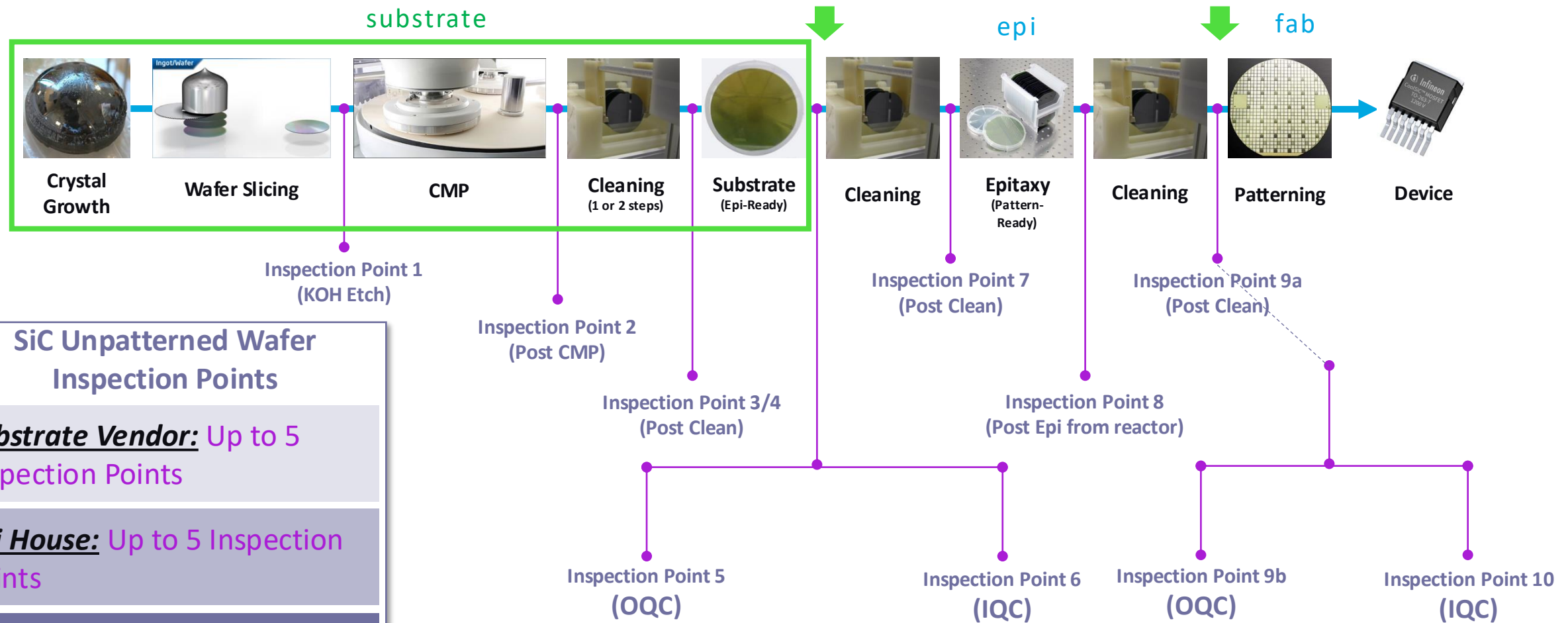


Gupta V. et al. - Defect Inspection for Compound Semiconductor Wafers - CSMANTECH 2020

SiC Substrate Defects Have Outsized Impact on Reliability & Yield

# SiC Power Device

## Unpatterned Wafer Process Flow & Inspection Points



**SiC Unpatterned Wafer Inspection Points**

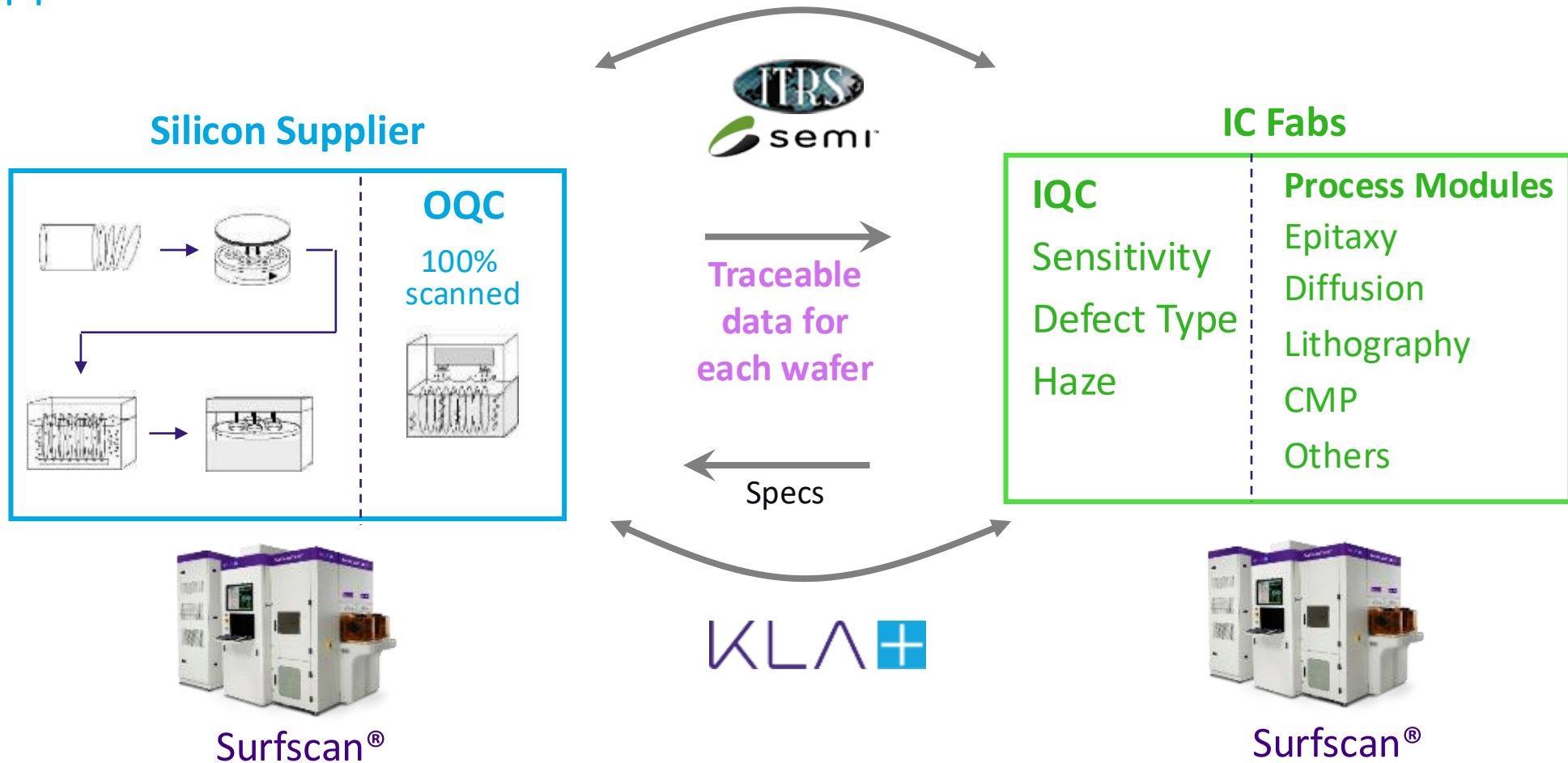
**Substrate Vendor:** Up to 5 Inspection Points

**Epi House:** Up to 5 Inspection Points

**Device Maker:** Up to 7 Inspection Points

# OQC/IQC Methodologies

## Silicon Supplier – Fab Handoff



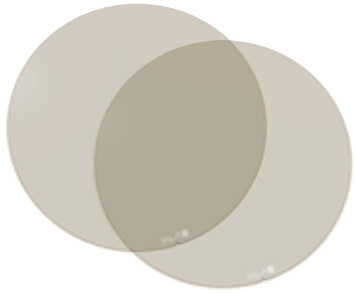
SEMI (industry) standard M59 mandates monitoring of killer defect types in Silicon. M81 controls Silicon Carbide

# Importance of Bare Wafer Inspection

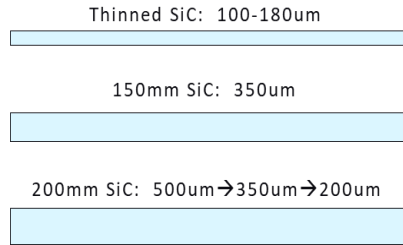


# Requirements for HVM SiC Success

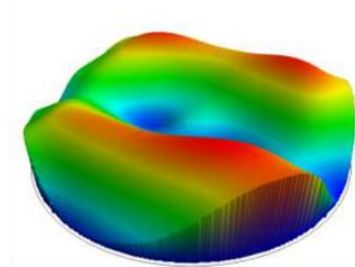
## Handling



Transparent

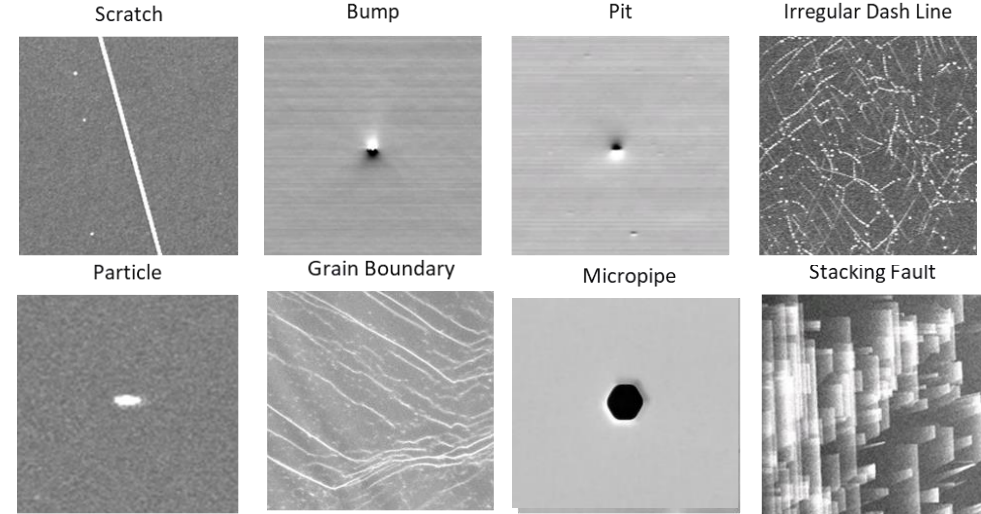


Varied thickness

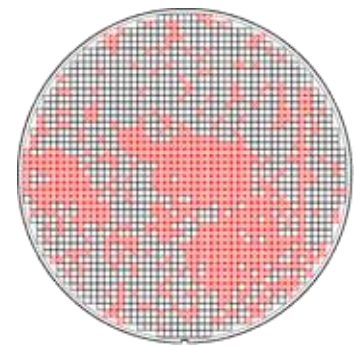


Bow & Warp

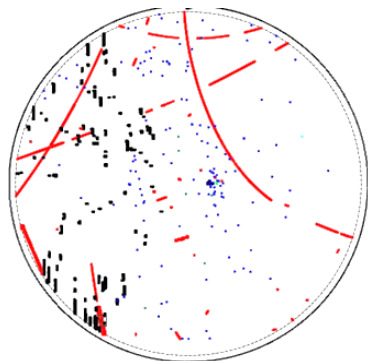
## Sensitivity at HVM Throughput



## Actionable: SPC+



Pseudo-die



Binning

Defect Type	% Wafer Impact	Status
DOI 1	11.59420%	FAIL
DOI 2	17.39130%	FAIL
DOI 3	18.47826%	FAIL
DOI 4	0.36232%	PASS
DOI 5	70.65217%	FAIL
DOI 6	2.17391%	PASS
Total	80.79710%	FAIL

Disposition

## Control Plan-Ready



GR&R



Fleet management & matching

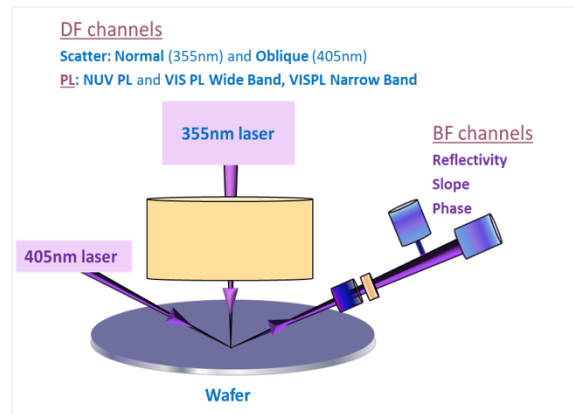
# KLA's Tools in This Space

## Candela® 8520



<1µm sensitivity  
~12WPH @8"

### 405&355nm Laser

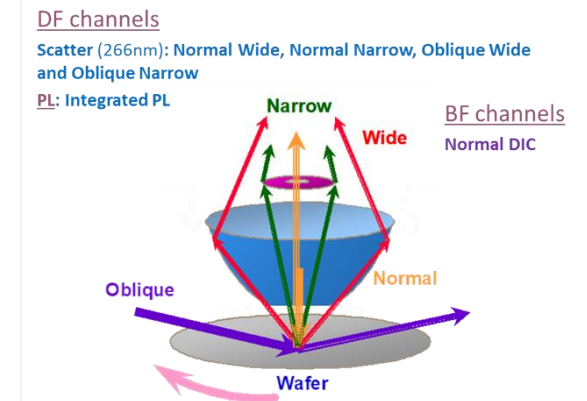


## Surfscan® SC1



<100nm sensitivity  
~32-110WPH @8"

### 266nm Laser



## ■ Original specialty substrate inspector

- 25-year history. 300+ Candela 8520 field units
- Engineering roots: agile/tunable multi-incidence, multi-detector, onboard analysis

## ■ Extension of HVM Si industry standard

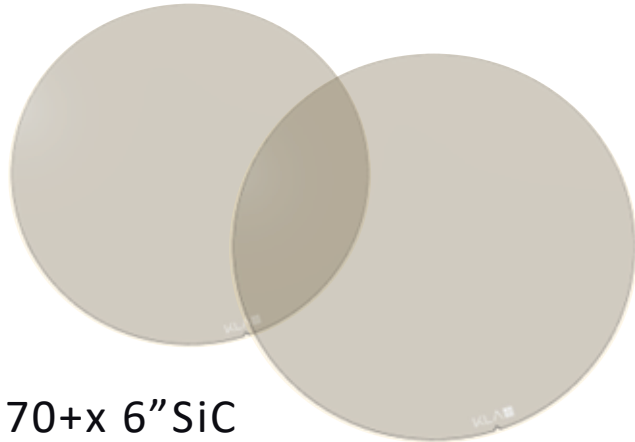
- Built on SPx platform, 1000+ production units
  - Darkfield, Haze, PL. SiC and Si
- Repeatable, matchable

# Results and Discussion



# Data Set and Measurement System

## Wafers



70+x 6" SiC substrates

36x 8" SiC substrates

**13\*** Substrate Providers

Sent to VW for supplier qualification

## Equipment



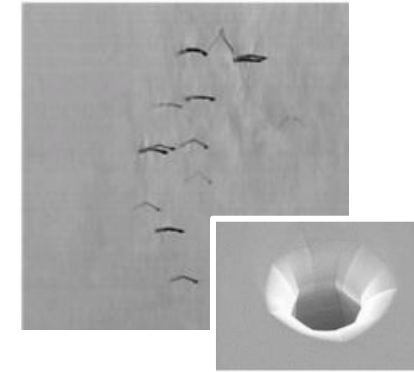
- Common defect inspectors
  - Candela® 8520
  - Surfscan® SC1



"Golden Recipe"

## Typical Defects of Interest\*

Micropipe

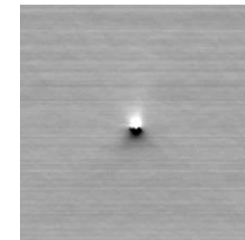


SEM Image

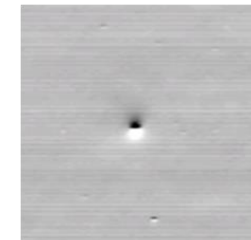
Stacking Fault



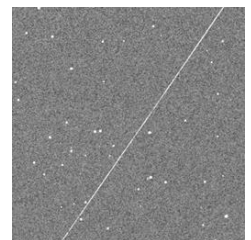
Bump



Pit



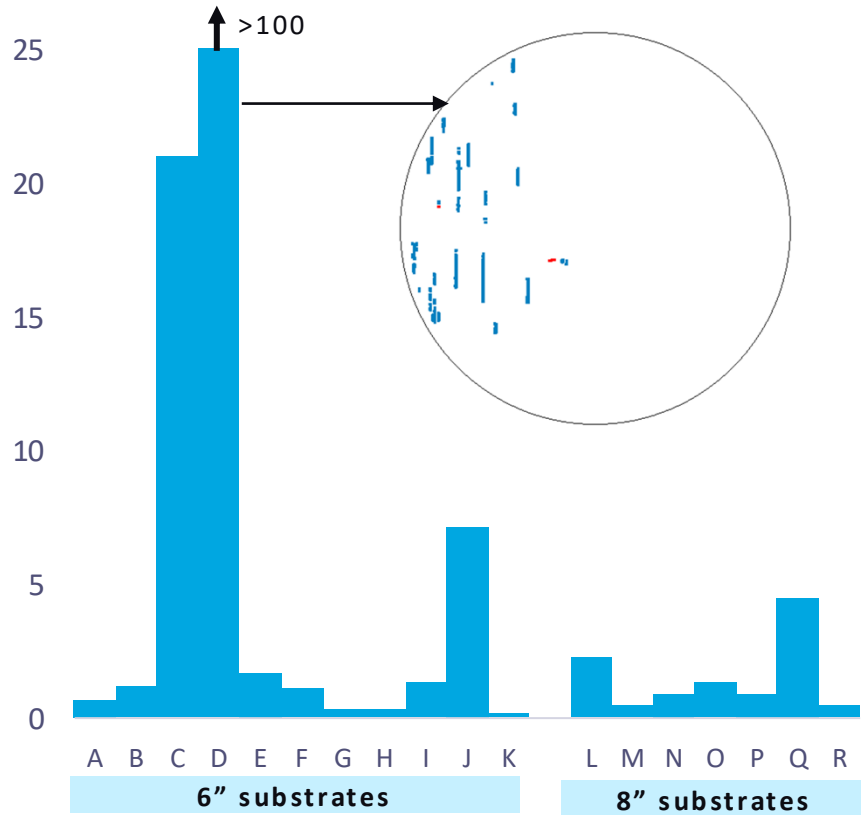
Scratch



\*non-exhaustive

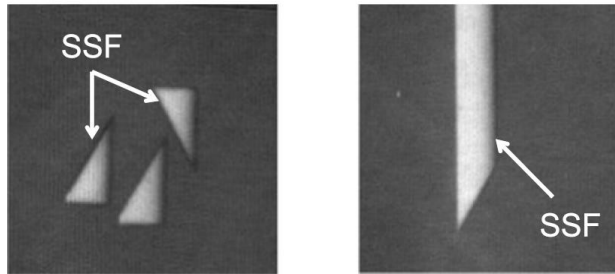
# Supplier Qualification for Stacking Faults

Avg. # of stacking faults per wafer

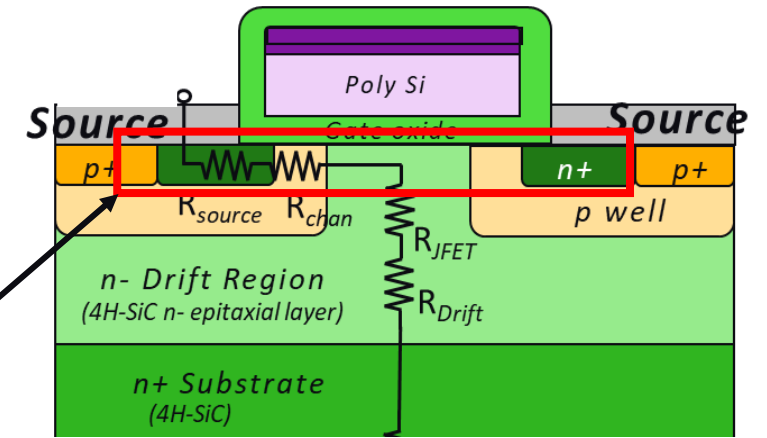


Substrate Supplier

Stacking faults can lead to reliability defect (Bipolar Degradation) through increased resistance in the area covered by the grown SSF

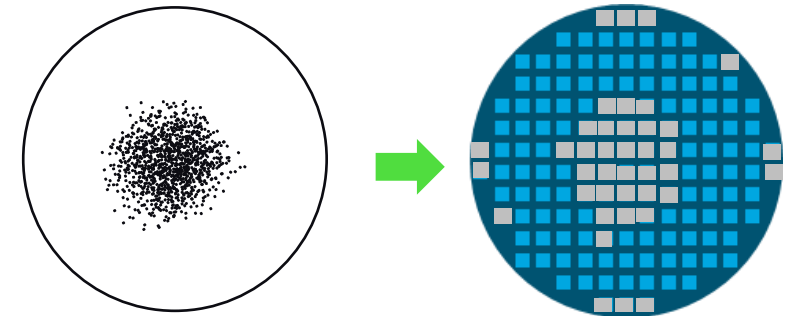


Defect images from: Kimoto, T. "Defect engr. in SiC technology for HV power devices" (2020 Appl. Phys. Exp 13 120201)



## Mitigation:

1. Electrical verification measures
2. Defect screening- ink wafer areas with high defect density.

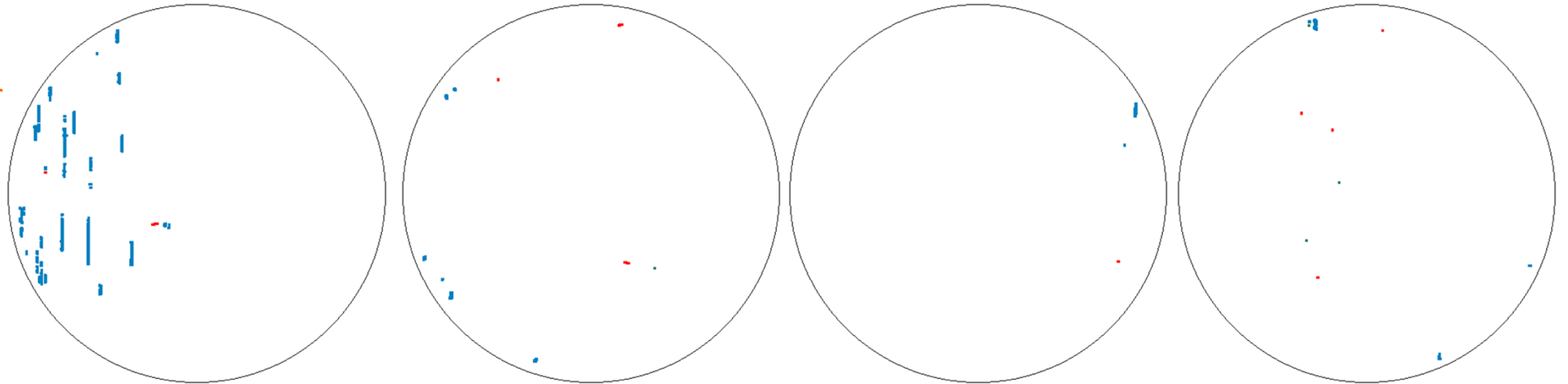


# Sample Defect Maps: Stacking Faults

Variation drives 100% sampling

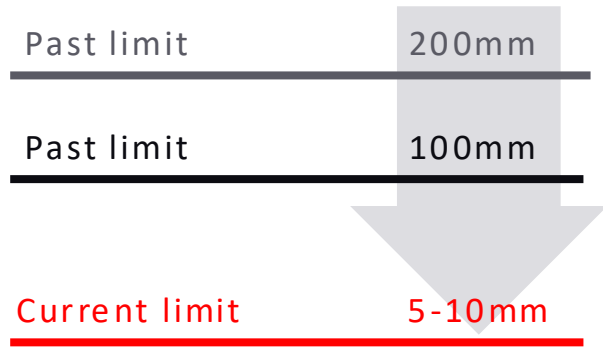
Supplier C

Maverick Wafer  
(same boule)

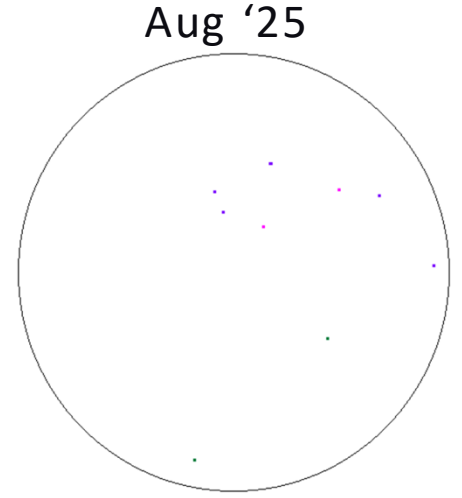
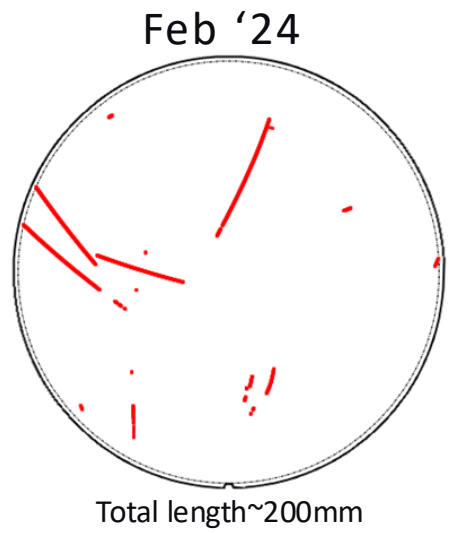


# Supplier Qualification for Scratches

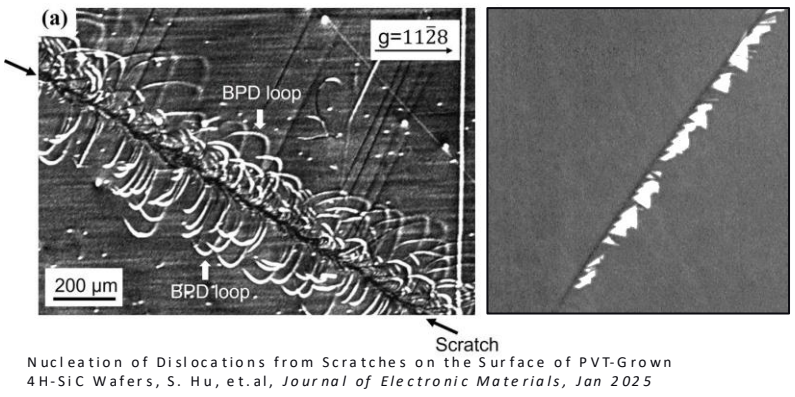
## Industry-wide improvement



Supplier K



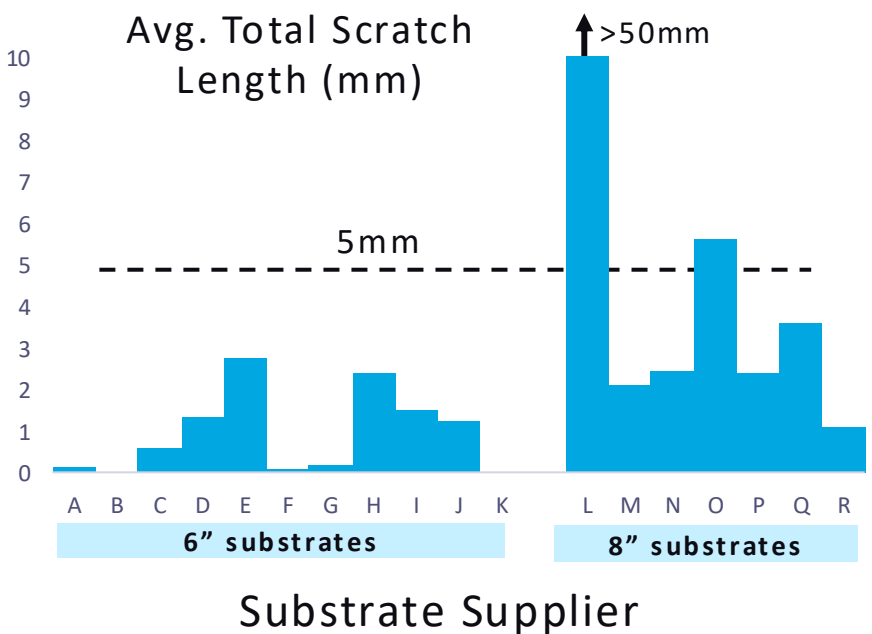
## Scratches can be a nucleation site for defect growth



Nucleation of Dislocations from Scratches on the Surface of PVT-Grown 4H-SiC Wafers, S. Hu, et.al, *Journal of Electronic Materials*, Jan 2025

- BPD Loops
- TEDs (prismatic slip)
- Partial dislocation loop expansion
- Stacking faults, step bunching at EPI

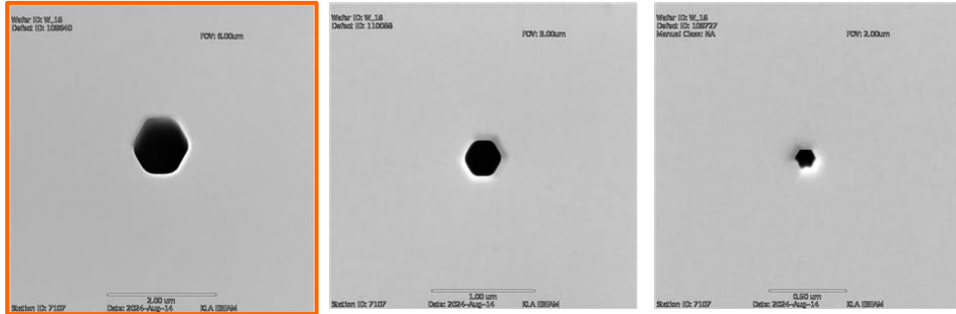
## Possible propagation/mitigation at Epitaxy



# Supplier Qualification for Micropipes

Killer defect: varied sizes

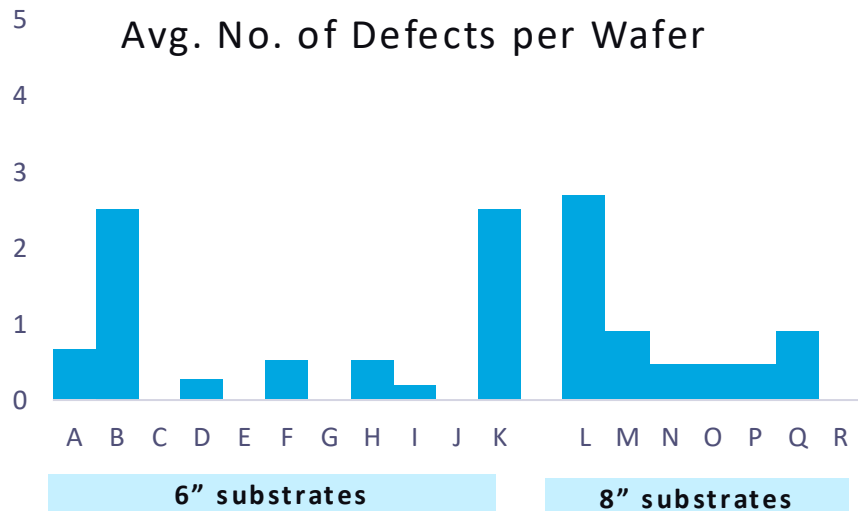
Current industry sensitivity



~800-1000nm

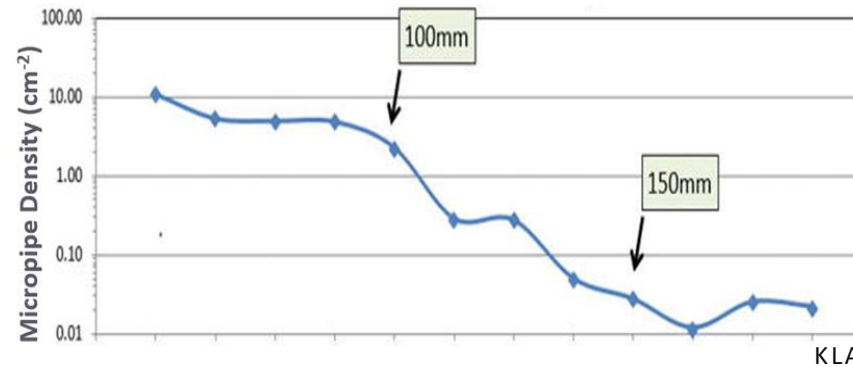
~300nm

~100nm

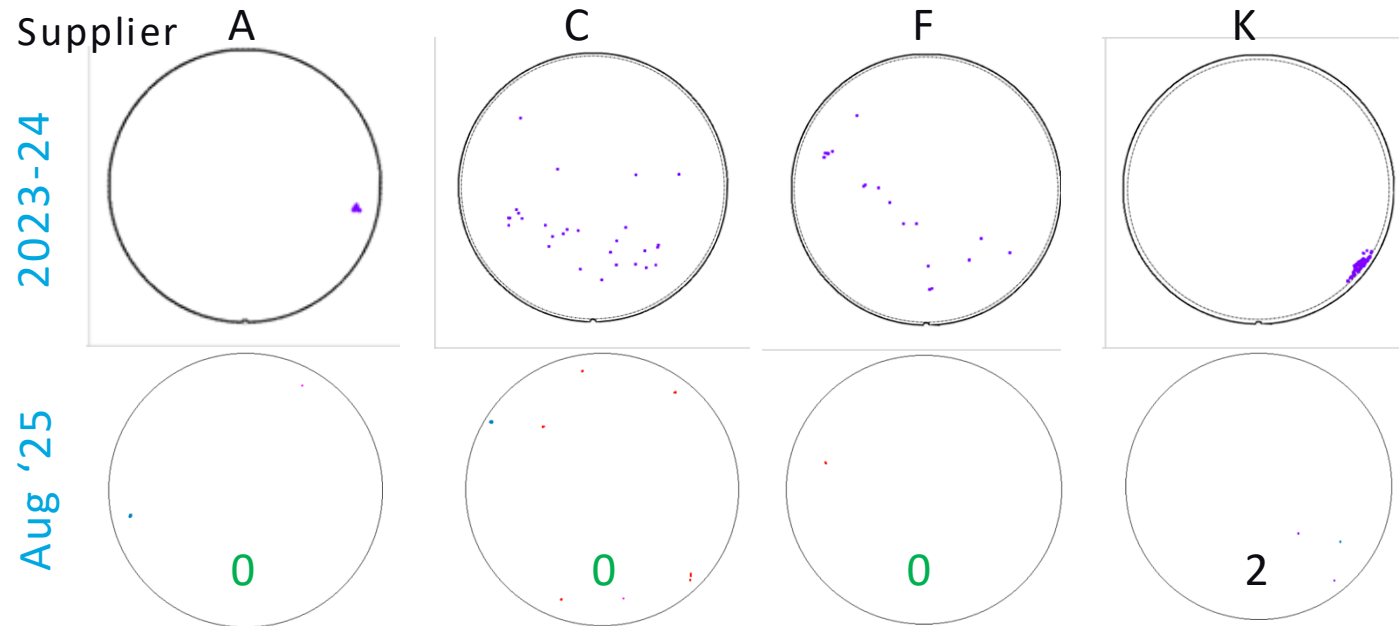


Substrate Supplier

Micropipe density decreasing:  $< .1/cm^2$

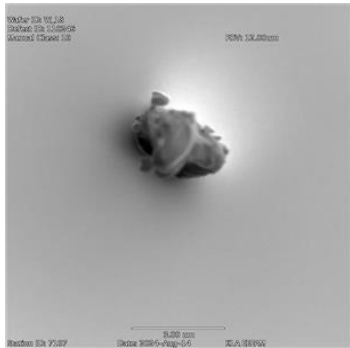


- Smaller diameter micropipes exist
- Characterizing ~100nm now on SC1
- SEM intensive

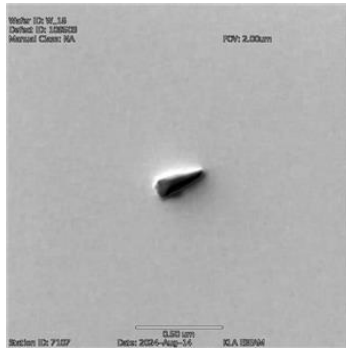


# Supplier Qualification for Particles

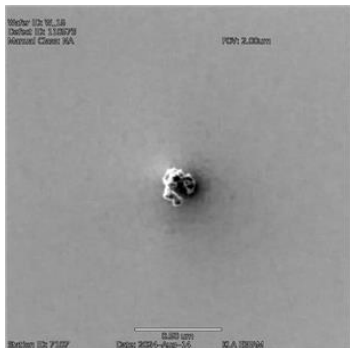
Cleanable\* and embedded



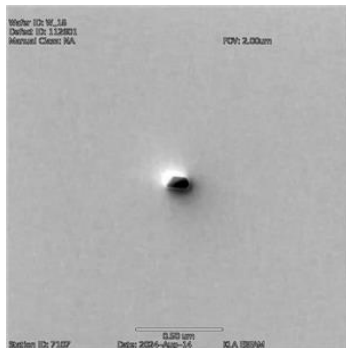
~5 um



~300nm



~150nm



<100nm

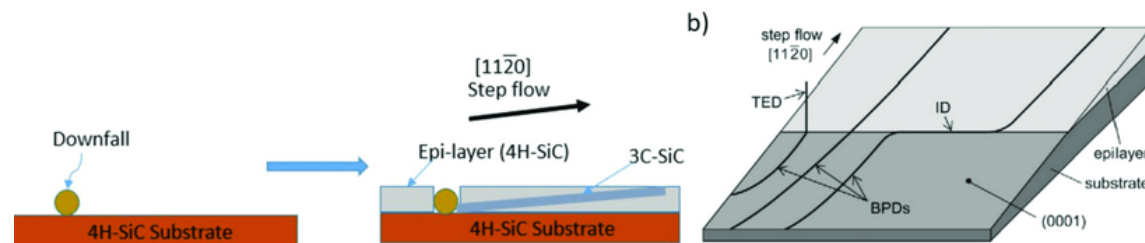
What size matters?

## Sources

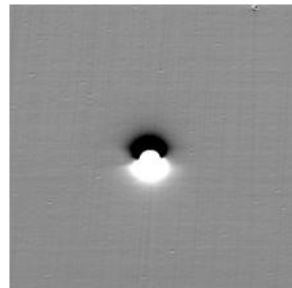
- 3C-SiC particles during crystal growth, powder impurities, furnace debris, slice, grind, CMP, tools, environment, handling

## Effects: Yield and Reliability

- Nucleation site for SF, dislocations and polytype inclusions
- Can propagate through Epi. growth variation, thin GateOx, doping disruption
- Can cause failure, higher leakage currents, higher on-state resistance, premature breakdown, reduced carrier mobility.

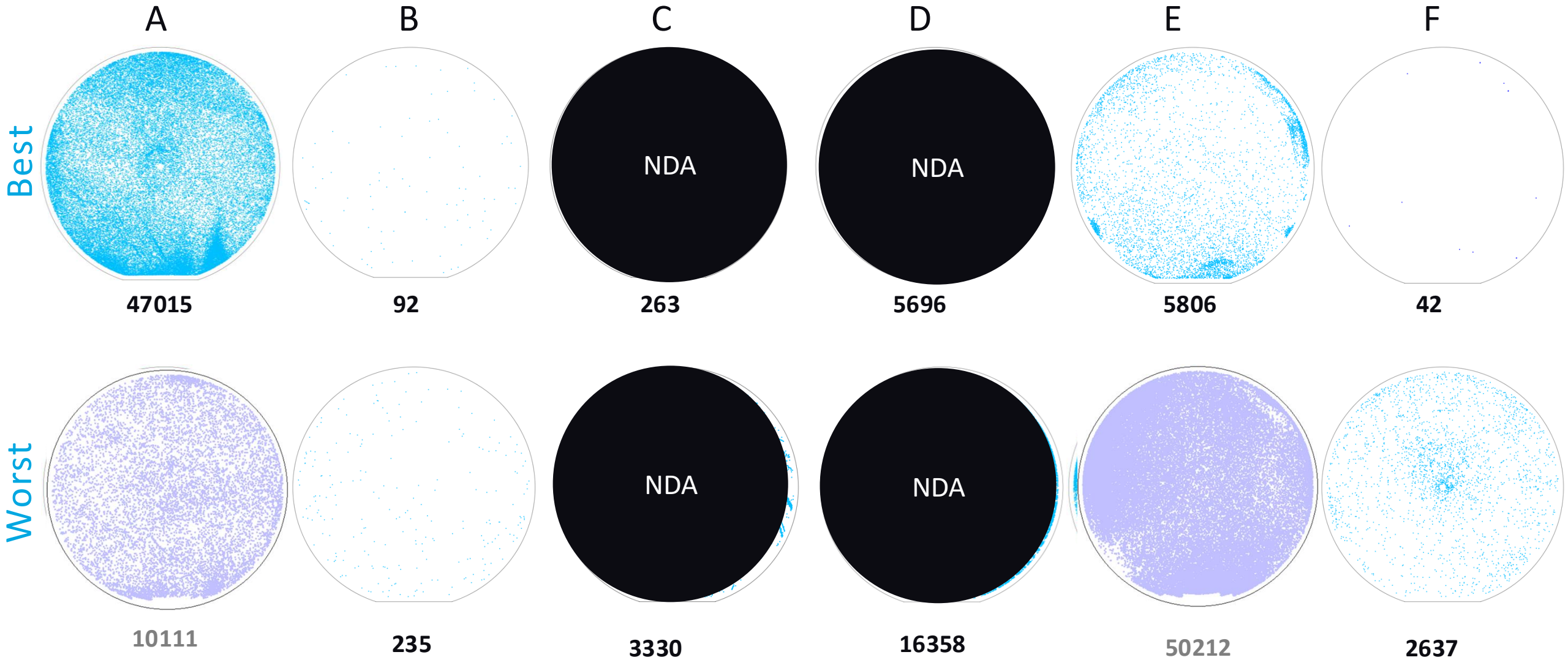


Downfall



Review of Silicon Carbide Process for Power MOSFET, C. Langpoklakpam et.al, Crystals, 2022, www.mdpi.com/journal/crystals

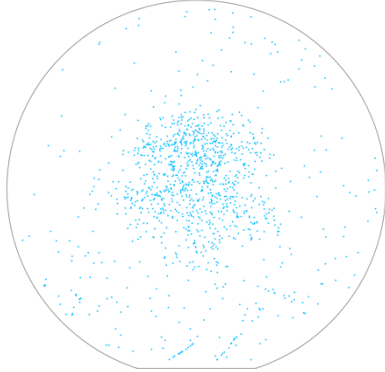
# Supplier Particle Comparisons at 125 WPH (6" wafers)



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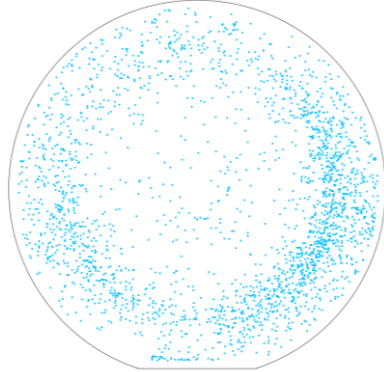
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G



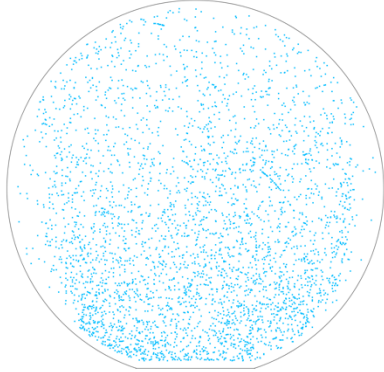
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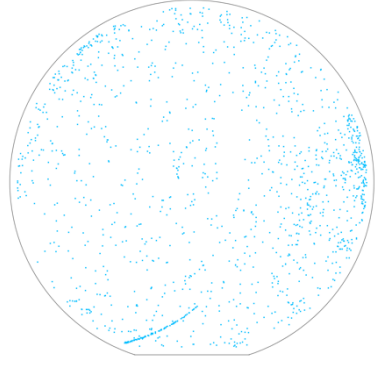
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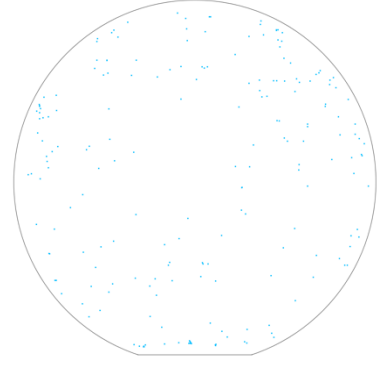
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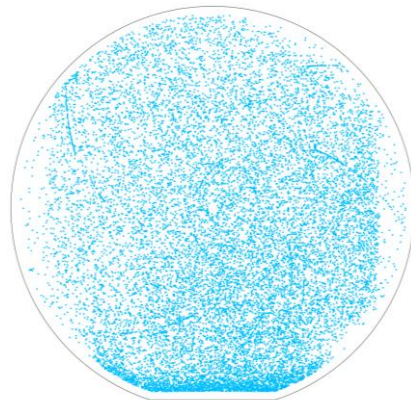
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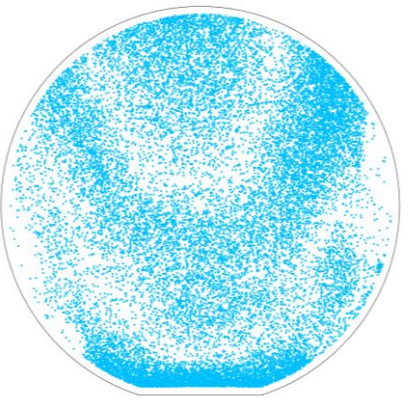


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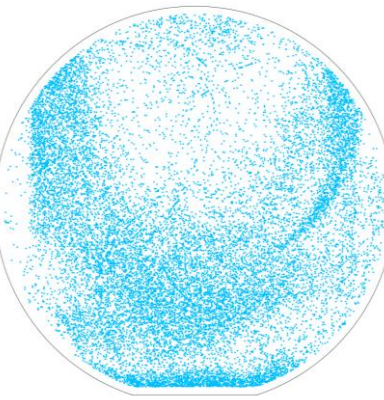
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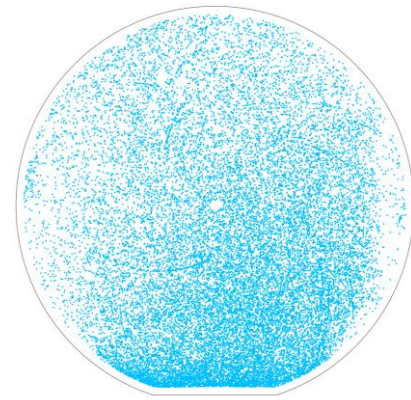
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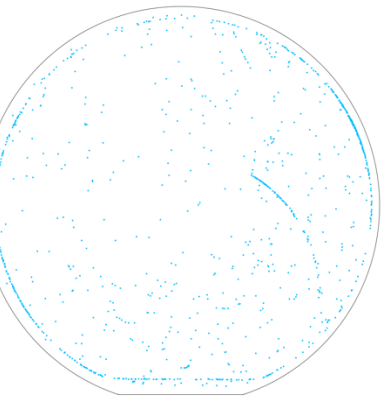
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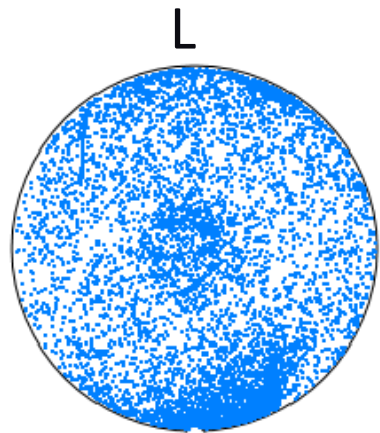
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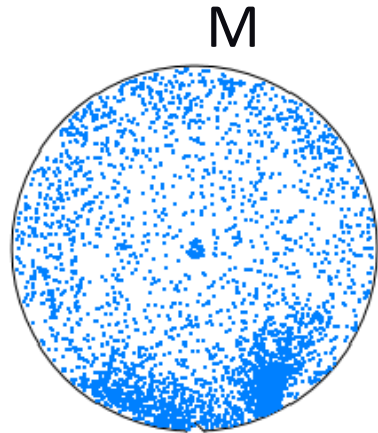
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# Supplier Particle Comparisons at 110 WPH (8" wafers)

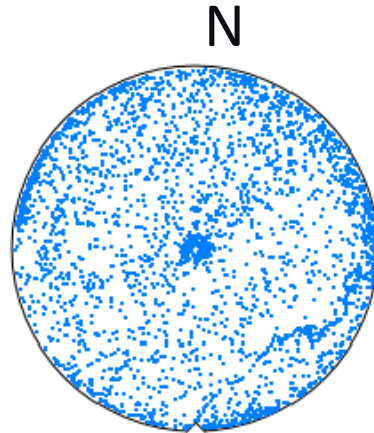
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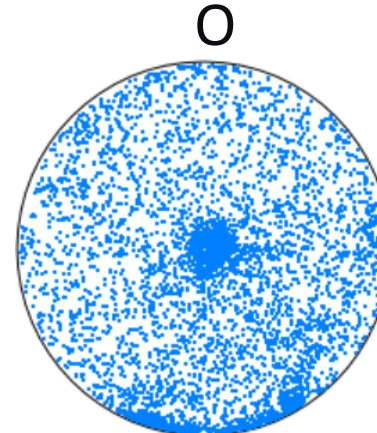
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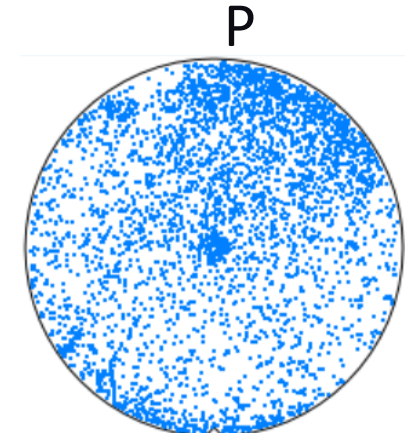
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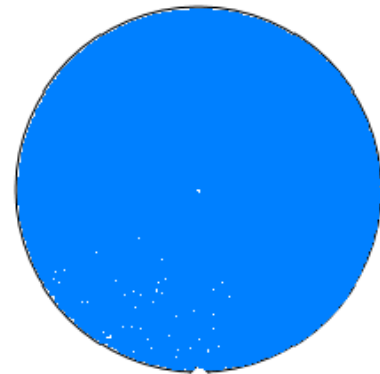


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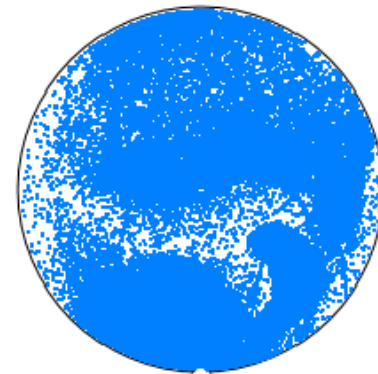


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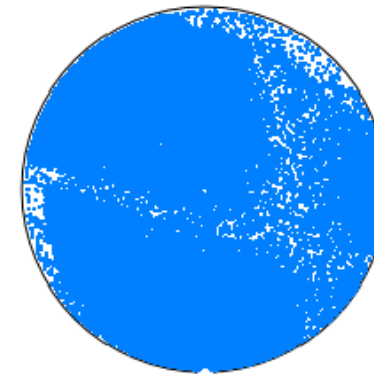
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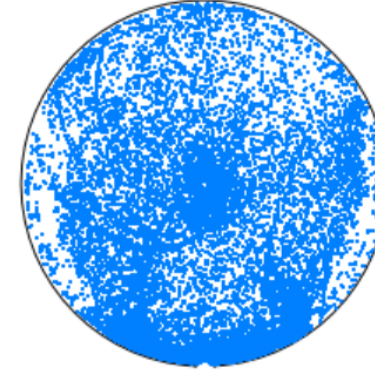
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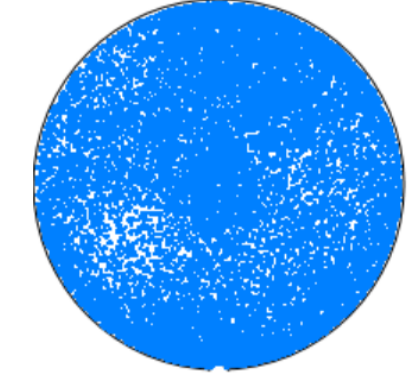
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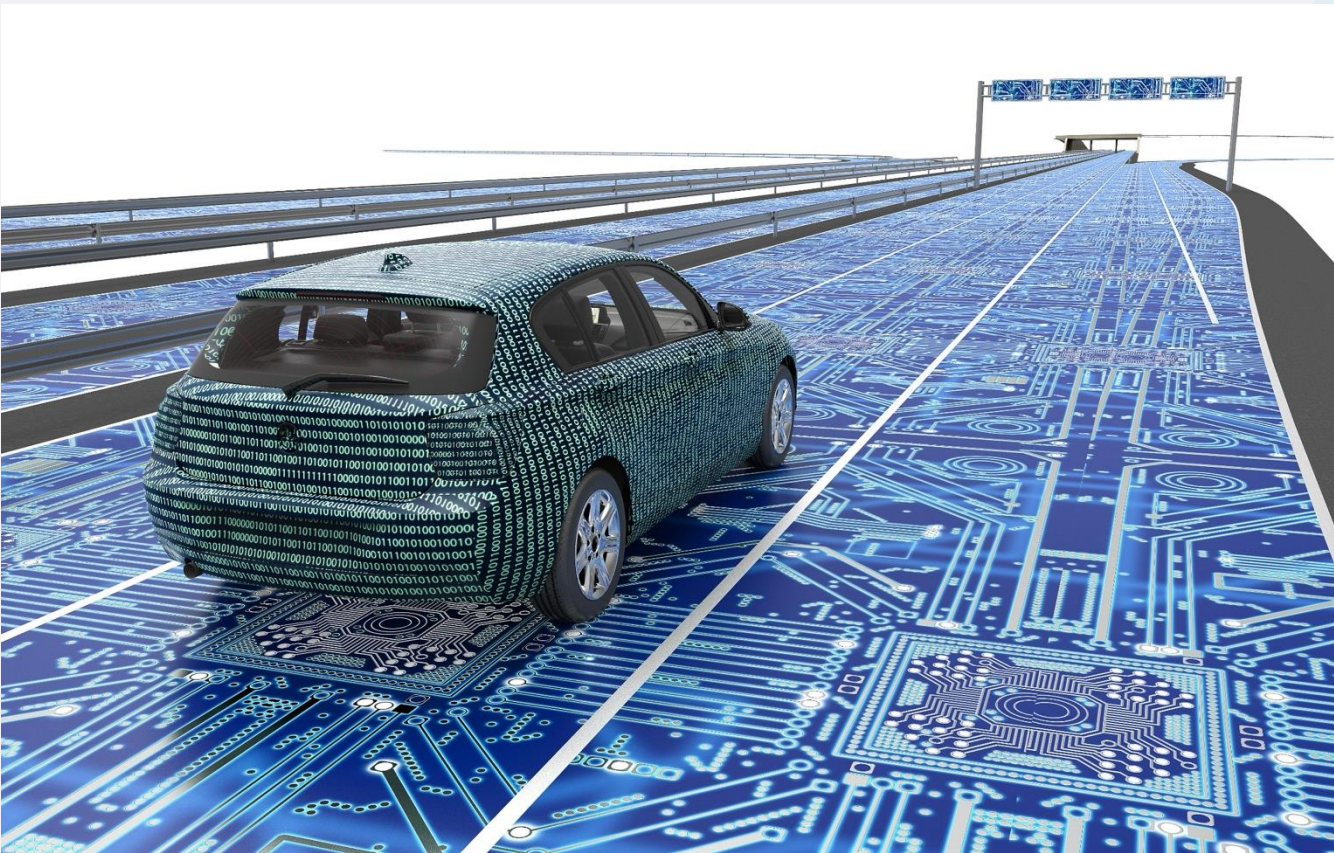


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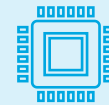


30335

# Summary and next steps



Supplier selection is challenging in a rapidly changing marketplace. Partnership beneficial



Si-like tools and use-cases coming to SiC to drive improvement



Ongoing project to assess 6" and 8" substrates, continuing through Epi and beyond



6" baseline maturing for OM-detectable crystalline defects. Surface defect cleanliness varies widely with room for improvement. Variability drives high sampling



# Thank You

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