Compact IP Protected Models for Electronics Reliability Supply Chain

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Motivation

- Automotive OEMs increasingly requiring simulation from suppliers
  - ➢ More insightful supplier evaluations
  - ➢ Reduction in design validation testing
  - ➢ Improved change management

- Simulation analysts at Tier 1 suppliers often lack insight into Tier 2 semiconductor packaging
  - ➢ Die size, die attach modulus, substrate stackup, etc.

- Inaccurate assumptions about internal geometries and material properties often lead to inaccurate predictions

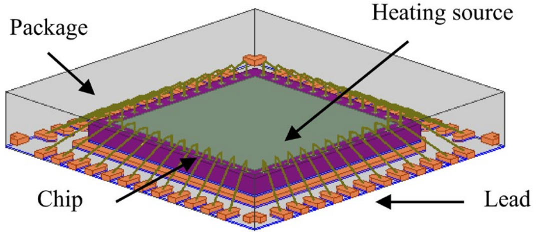
- Directly sharing detailed FE models is not an option
  - ➢ Reveals key IPs
  - ➢ Long simulation time to incorporate detailed FE models of different components

Need for a workflow to create obfuscated component models that protects IP and offers decent accuracy in predictions

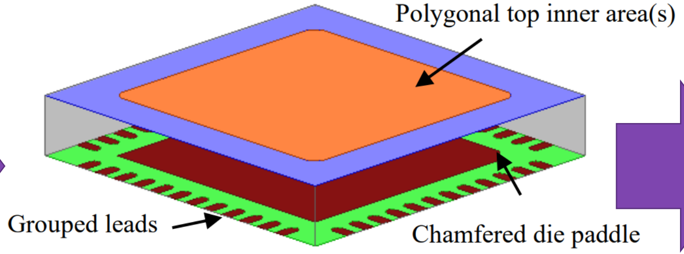
Compact Models for Thermal Analyses

Delphi Network

- Is a thermal resistor network that captures the lumped thermal behavior of the component
- Ansys has provided automation to streamline the generation on Delphi network models in Mechanical



Detailed FE model of the package



Selecting different faces as nodes in the network

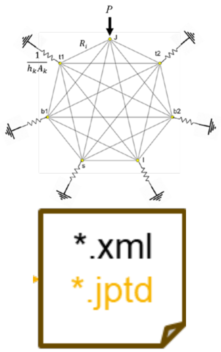
$$f = \sum_{i=1}^{m} \omega_i f_i(X) \;\; with \sum_{i=1}^{m} \omega_i = 1 \; \forall \; \omega_i \geq 0$$

$$f_1(X)|_{\substack{n=s\\n=1}} = \frac{1}{nB} \sum_{b=1}^{nB} \left[\frac{T_{n,D}^{b} - T_{n,C}^{b}(X)}{T_{n,D}^{b} - T_{\infty}} \right]^2,$$

$$\forall \; n \in \{1, \cdots, j, \cdots, nN\}$$

$$f_2(X)|_{\substack{n\neq s\\n>1}} = \frac{1}{nB} \sum_{b=1}^{nB} \left[\frac{1}{nA} \sum_{n=1}^{nA} \left[\frac{q_{n,D}^{b} - q_{n,C}^{b}(X)}{Q} \right]^2 \right]$$

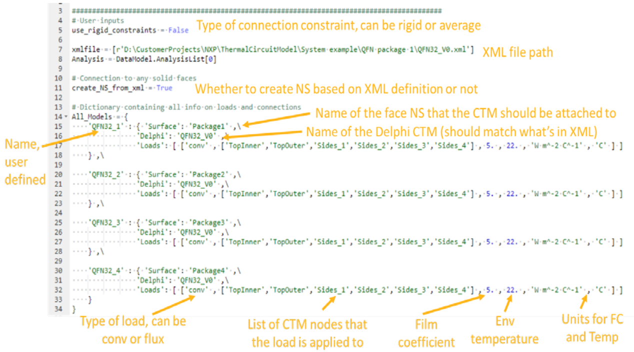
Multi-objective optimization to minimize error on a set of training load cases



Export network

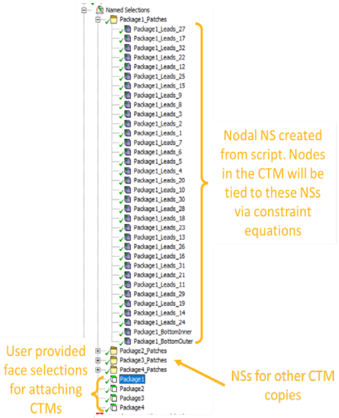
Delphi Network: Use pass

- Automation script was created to turn .xml file into thermal resistor network in Mechanical
- Auto creation of nodal named selections on the interface between the solid model and Delphi network for connecting the network
- Creation of post-processing objects to facilitate result visualization and extraction

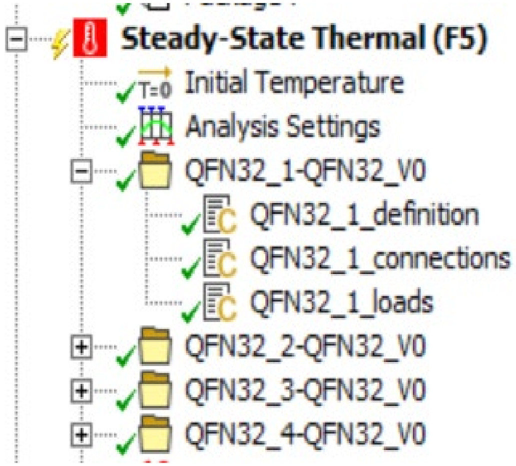


```
######################################################################################
# User inputs
use_rigid_constraints = False

xmlfile = [r'D:\CustomerProjects\NXP\ThermalCircuitModel\System example\QFN package 1\QFN32_V0.xml']
Analysis = DataModel.AnalysisList[0]

# Connection to any solid faces
create_NS_from_xml = True

# Dictionary containing all info on loads and connections
All_Models = {
    'QFN32_1' : { 'Surface': 'Package1' ,\
                  'Delphi': 'QFN32_V0' ,\
                  'Loads': [ ['conv' , ['TopInner','TopOuter','Sides_1','Sides_2','Sides_3','Sides_4'] , 5. , 22. , 'W m^-2 C^-1' , 'C' ] ]
    } ,\

    'QFN32_2' : { 'Surface': 'Package2' ,\
                  'Delphi': 'QFN32_V0' ,\
                  'Loads': [ ['conv' , ['TopInner','TopOuter','Sides_1','Sides_2','Sides_3','Sides_4'] , 5. , 22. , 'W m^-2 C^-1' , 'C' ] ]
    } ,\

    'QFN32_3' : { 'Surface': 'Package3' ,\
                  'Delphi': 'QFN32_V0' ,\
                  'Loads': [ ['conv' , ['TopInner','TopOuter','Sides_1','Sides_2','Sides_3','Sides_4'] , 5. , 22. , 'W m^-2 C^-1' , 'C' ] ]
    } ,\

    'QFN32_4' : { 'Surface': 'Package4' ,\
                  'Delphi': 'QFN32_V0' ,\
                  'Loads': [ ['conv' , ['TopInner','TopOuter','Sides_1','Sides_2','Sides_3','Sides_4'] , 5. , 22. , 'W m^-2 C^-1' , 'C' ] ]
    }
}
```

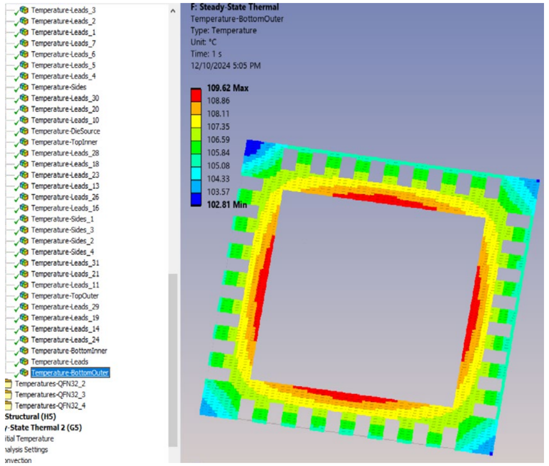
User defines package locations and applied loads on the network



Script creates NS for attachment



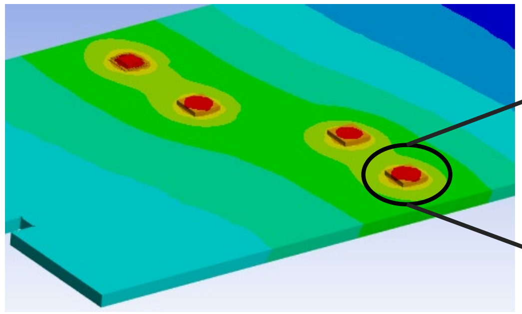
Add Delphi networks as APDL snippets



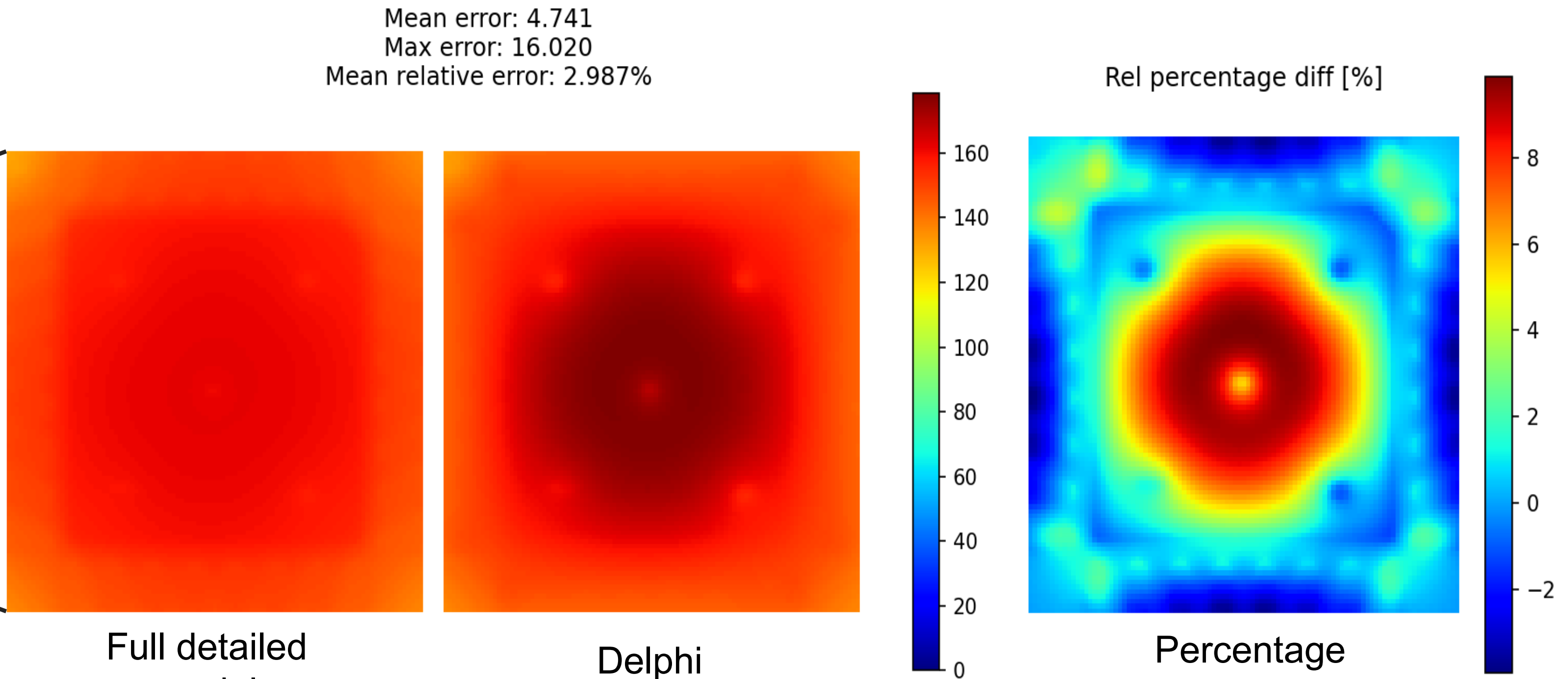
Add post-processing objects

Delphi Network: Use pass

- Results of a steady-state thermal analysis is compared with the equivalent full-solid detailed FE model
  - Loads: Power generation at the center of the chip, convection on all chip exterior sides
  - Inspect the temperature result on the board-chip interface (interface between the solid board model and the Delphi thermal network)



Zooming in to focus on the temperature at the board-chip interface



Full detailed model

Delphi Network

Percentage different in solutions

The Delphi network over-predicts the temperature at the center of the chip, but average error is less than 3% with a max of ~10%

Superelement (SE)

- Superelement, or substructure, is a matrix element representing a collection of multiple regular elements
- Only master degrees of freedom are retained for nodes on the SE to connect to other bodies or apply loads

$$[M]\{\ddot{u}\}+[C]\{\dot{u}\}+[K]\{u\}=\{F\}$$

$$\{u\}=\begin{Bmatrix}\{u_m\}\\ \{u_c\}\end{Bmatrix},\ [M]=\begin{bmatrix}{[M_{mm}]} & {[M_{mc}]}\\ {[M_{cm}]} & {[M_{cc}]}\end{bmatrix},\ [C]=\begin{bmatrix}{[C_{mm}]} & {[C_{mc}]}\\ {[C_{cm}]} & {[C_{cc}]}\end{bmatrix},\ [K]=\begin{bmatrix}{[K_{mm}]} & {[K_{mc}]}\\ {[K_{cm}]} & {[K_{cc}]}\end{bmatrix},\ \{F\}=\begin{Bmatrix}\{F_m\}\\ \{F_c\}\end{Bmatrix}$$

- Subscript ***m*** denotes master(retained) DOF
- Subscript ***c*** denotes condensed(reduced) DOF

$$\{u\}=\begin{Bmatrix}\{u_m\}\\ \{u_c\}\end{Bmatrix}=[T]\{\hat{u}\}$$

Express full DOF vector in terms of master DOFs

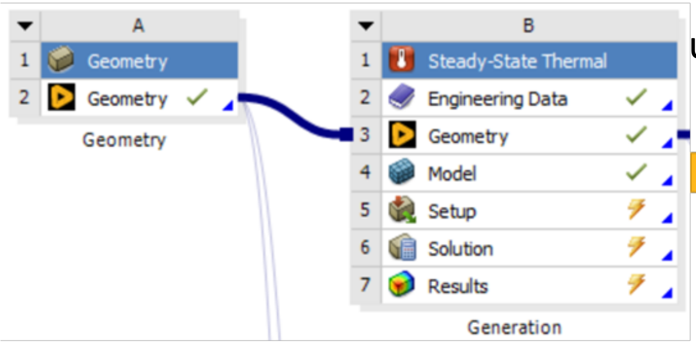
Reduced equation of motion

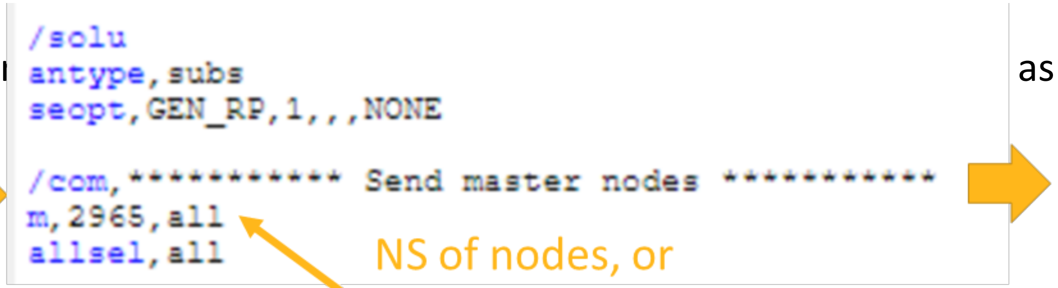
$$[\hat{M}]\{\ddot{\hat{u}}\}+[\hat{C}]\{\dot{\hat{u}}\}+[\hat{K}]\{\hat{u}\}=\{\hat{F}\}$$

Superelement K matrix

Superelement load vector

- Generation pass (for thermal SE):
  - Subs uctu as workaround





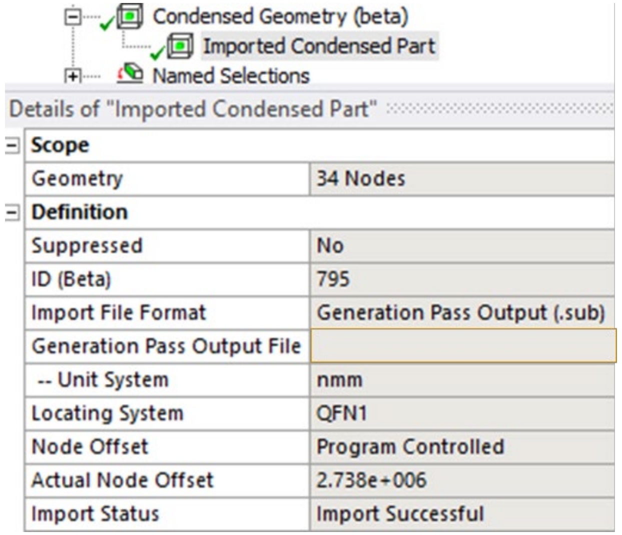
```
/solu
antype,subs
seopt,GEN_RP,1,,,NONE

/com,*********** Send master nodes ***********
m,2965,all
allsel,all
```

NS of nodes, or remote pt as master

.sub file

Superelement: Use pass

- Once the .sub file is generated, the thermal SE can be imported via the imported condensed part feature in the model tree
- SE loads to be added via command snippet

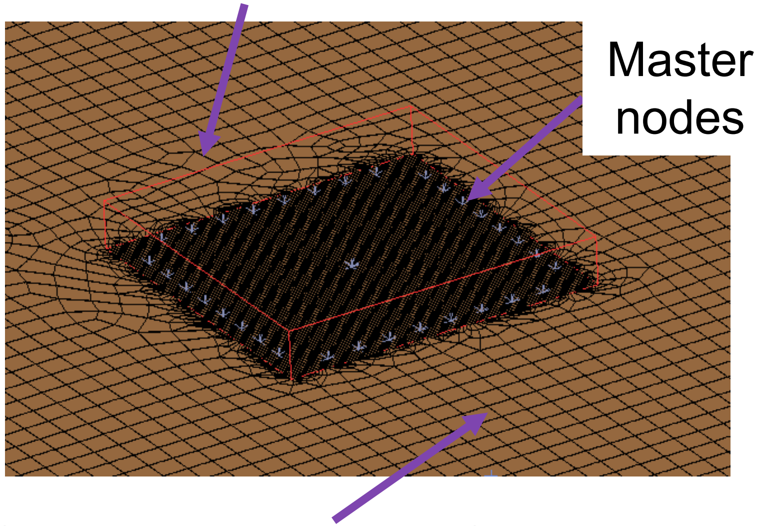


Condensed Geometry (beta)
Imported Condensed Part
Named Selections

Details of "Imported Condensed Part"

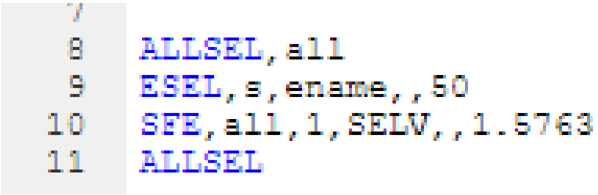
Scope	
Geometry	34 Nodes
Definition	
Suppressed	No
ID (Beta)	795
Import File Format	Generation Pass Output (.sub)
Generation Pass Output File	
-- Unit System	nmm
Locating System	QFN1
Node Offset	Program Controlled
Actual Node Offset	2.738e+006
Import Status	Import Successful

Outline of the SE



Master nodes

Solid element model of the board



```
ALLSEL,all
ESEL,s,ename,,50
SFE,all,1,SELV,,1.5763
ALLSEL
```

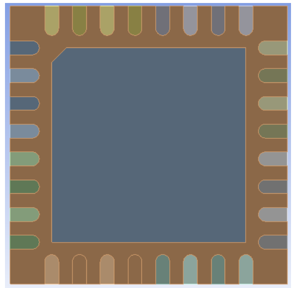
SE load applied via command snippet

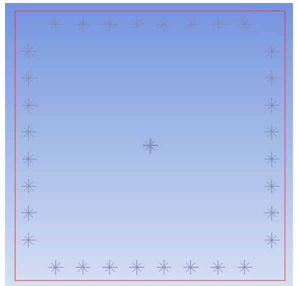
Superelement: Use pass

- Result comparison, different master node selection and interface connection strategies explored
- With SE, different connection strategies and master node arrangements can be used
- Inspect the temperature result on the board-chip interface (interface between the solid board model and the superelement)

Using 1 master node per feature face: 34 nodes, connected using average CEs using the same NSs as in Delphi network

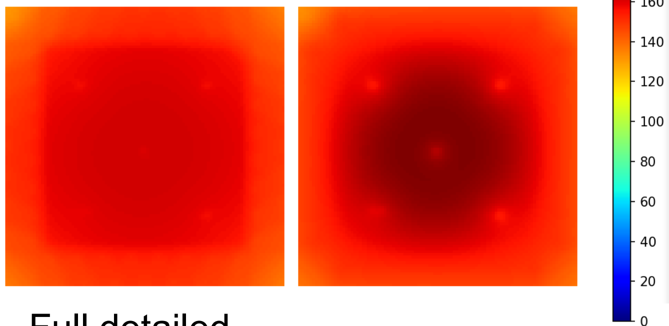
Geometry





Master nodes

Mean error: 2.267
Max error: 7.702
Mean relative error: 2.494%



Full detailed model

Superelemen
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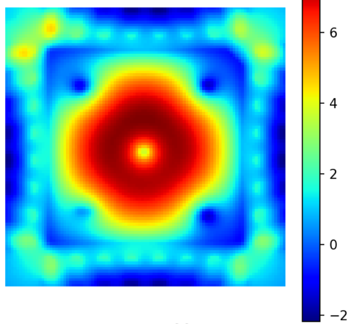
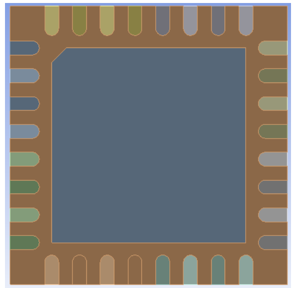
Rel percentage diff [%]

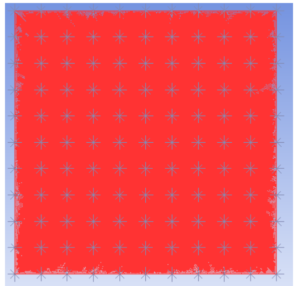


Percentage different in solutions

21x21 uniform grid of master nodes: 441 nodes, connected using node-to-surface contact

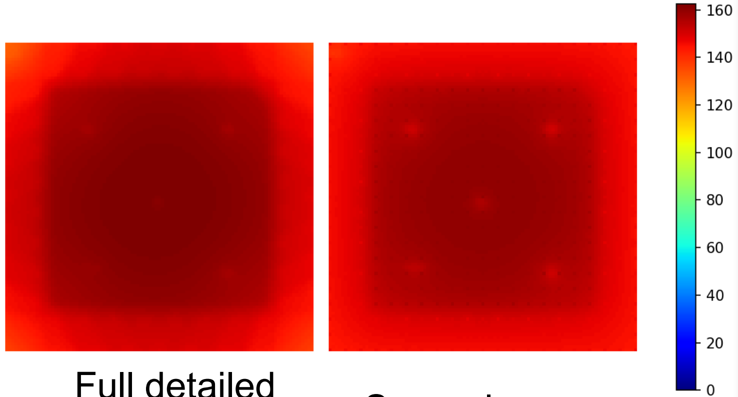
Geometry





Master nodes

Mean error: -1.163
Max error: 11.242
Mean relative error: 1.689%



Full detailed model

Superelemen
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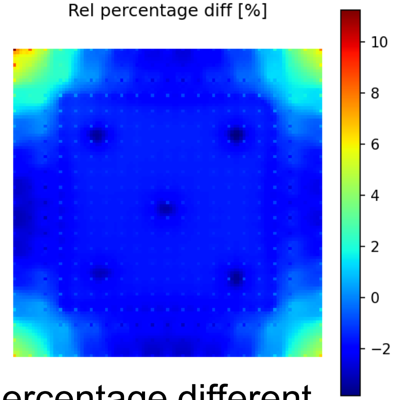
Rel percentage diff [%]



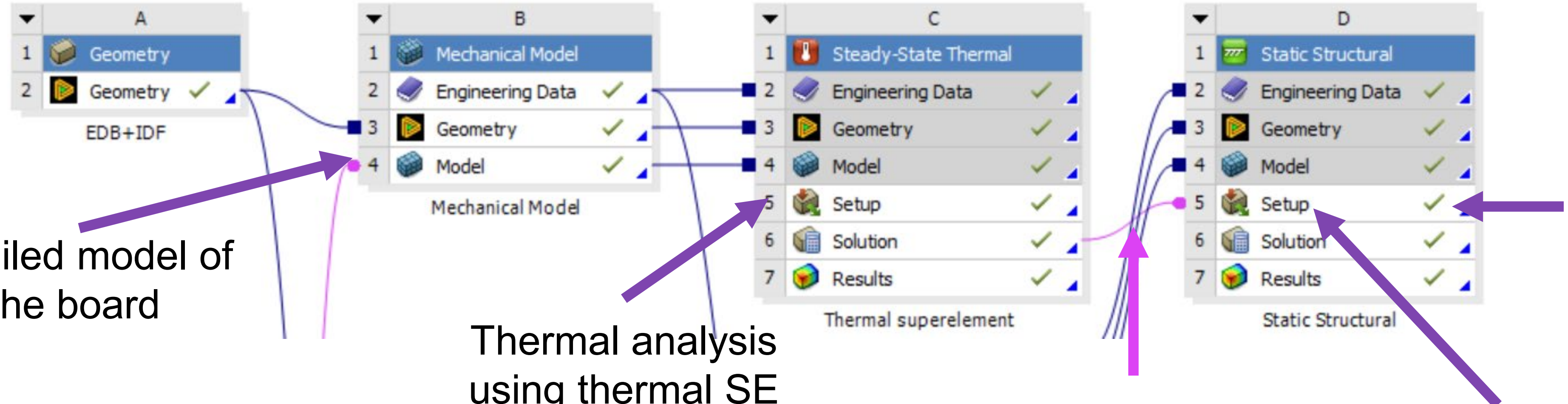
Percentage different in solutions

Compact Models for Thermal-Mechanical Analyses

Superelements for uncoupled thermal stress analysis

Workflow:

- Generate thermal SE and use in thermal analysis
- Generate structural SE
- Import temperature field from thermal analysis, then simulate thermal stress with structural SE

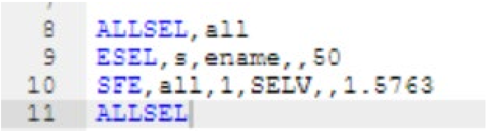


Detailed model of the board

Thermal analysis using thermal SE

Transferring temperature field to structural analysis

Thermal stress analysis using structural SE



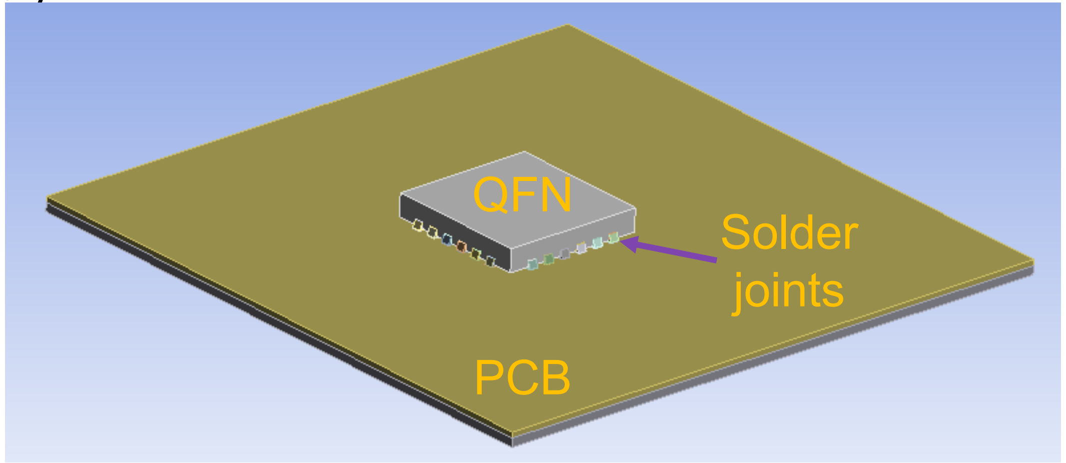
```
ALLSEL,all
ESEL,s,ename,,50
SFE,all,1,SELV,,1.5763
ALLSEL
```

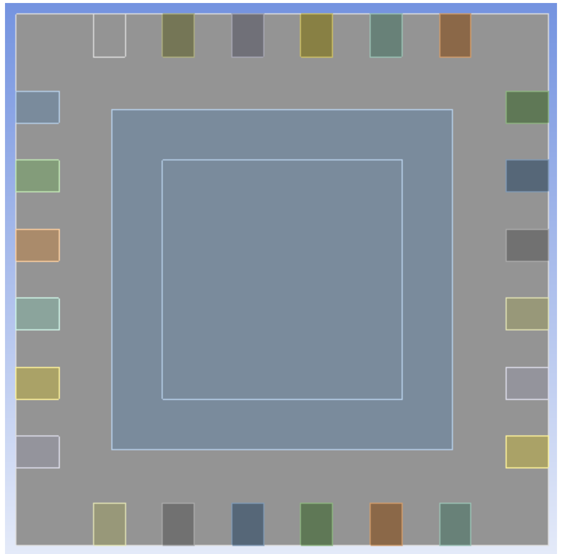
Apply thermal condition to structural SE via element load to induce thermal expansion on chip

Detailed Comparison of Superelement and full-model solutions

Superelement: A detailed comparison

- Fidelity of the superelement depends on the selection of master DOFs
- We show comparison in the ideal case where all interface nodes are retained as master DOFs to minimize difference
- Cases tested:
  1. Modal analysis
  2. Steady-state thermal simulation
  3. Thermal cycling with temperature field, evaluating fatigue on the solder connections
- Geometry:



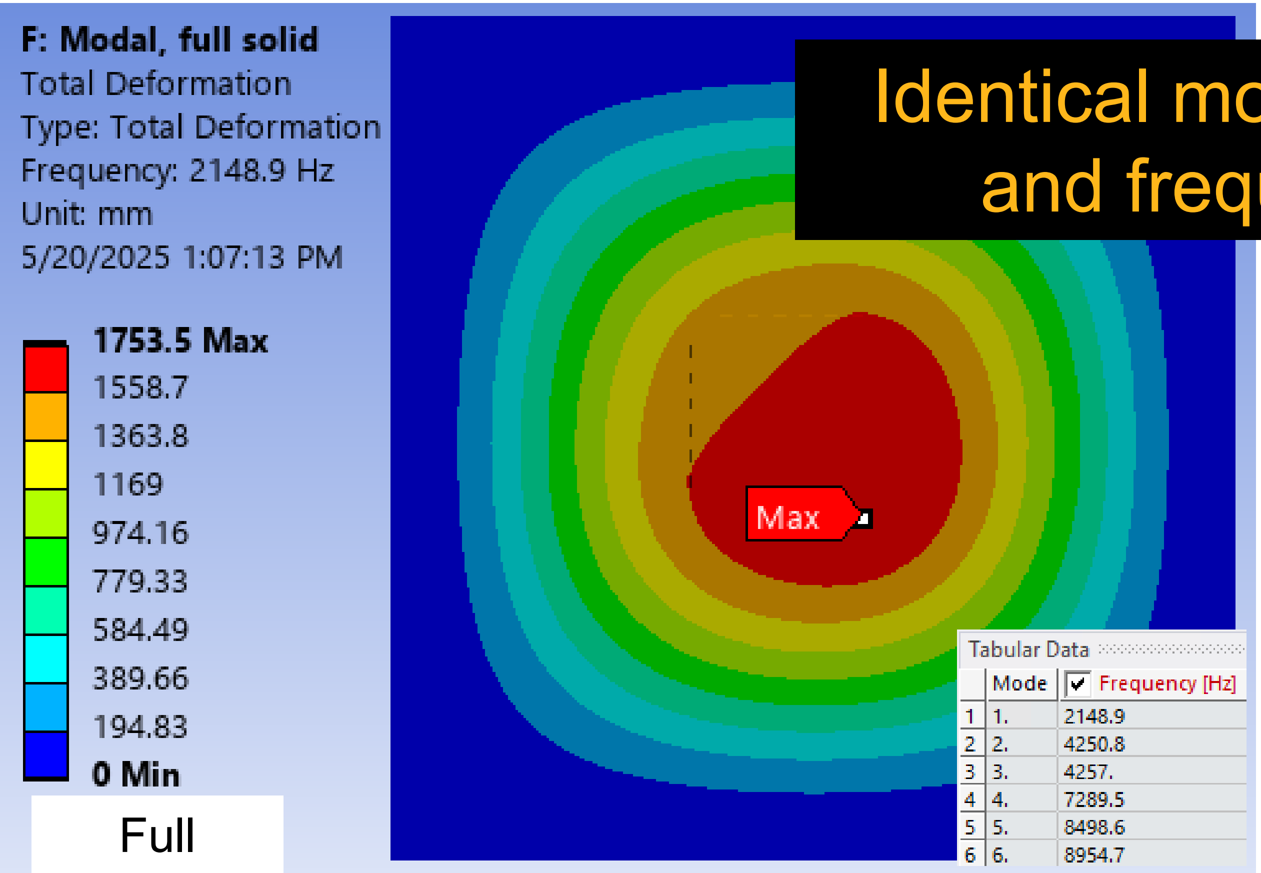


Bottom-up view of the generic QFN model

Modal analysis

- BCs:
  - PCB fixed on all 4 sides

Identical mode shapes and frequencies

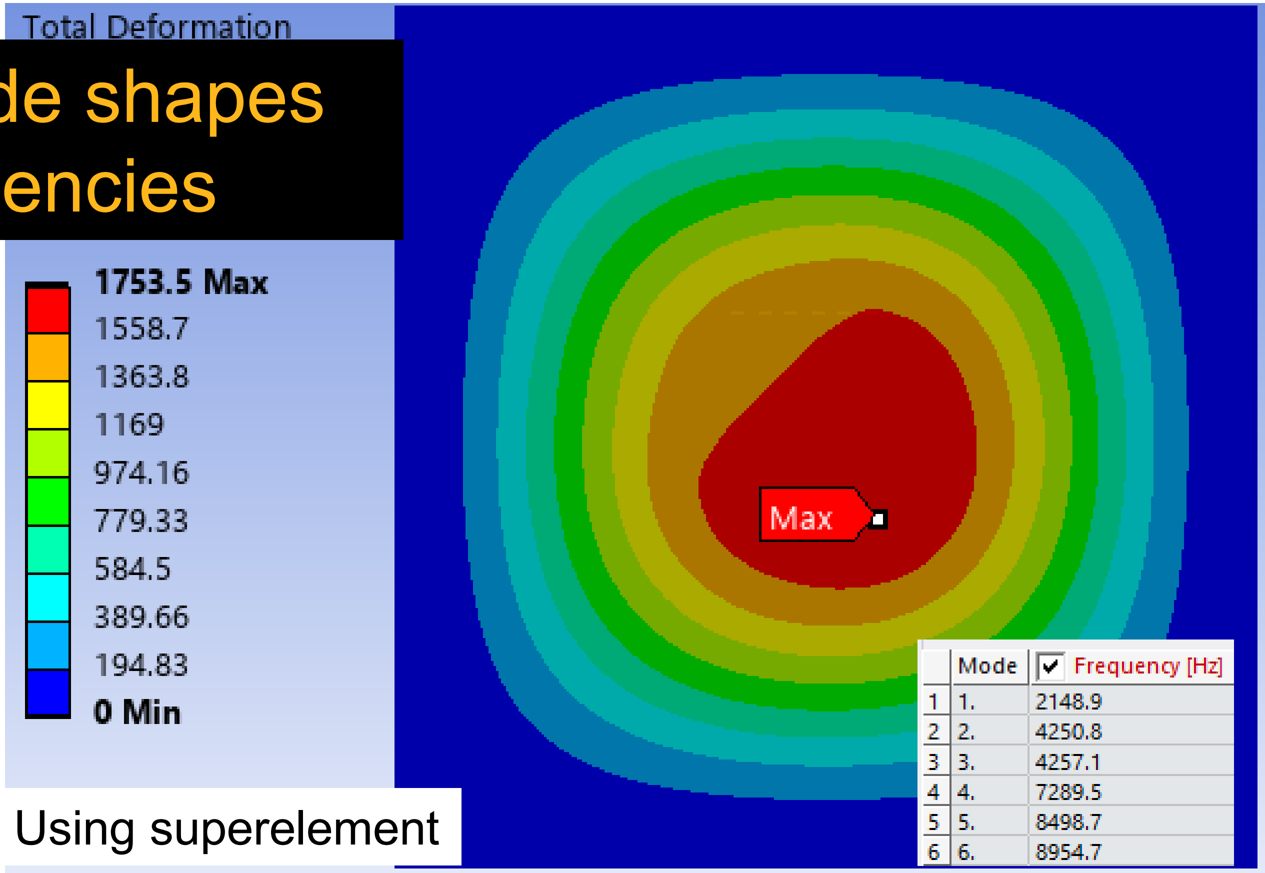


F: Modal, full solid
Total Deformation
Type: Total Deformation
Frequency: 2148.9 Hz
Unit: mm
5/20/2025 1:07:13 PM

Tabular Data

	Mode	☑ Frequency [Hz]
1	1.	2148.9
2	2.	4250.8
3	3.	4257.
4	4.	7289.5
5	5.	8498.6
6	6.	8954.7

Full model



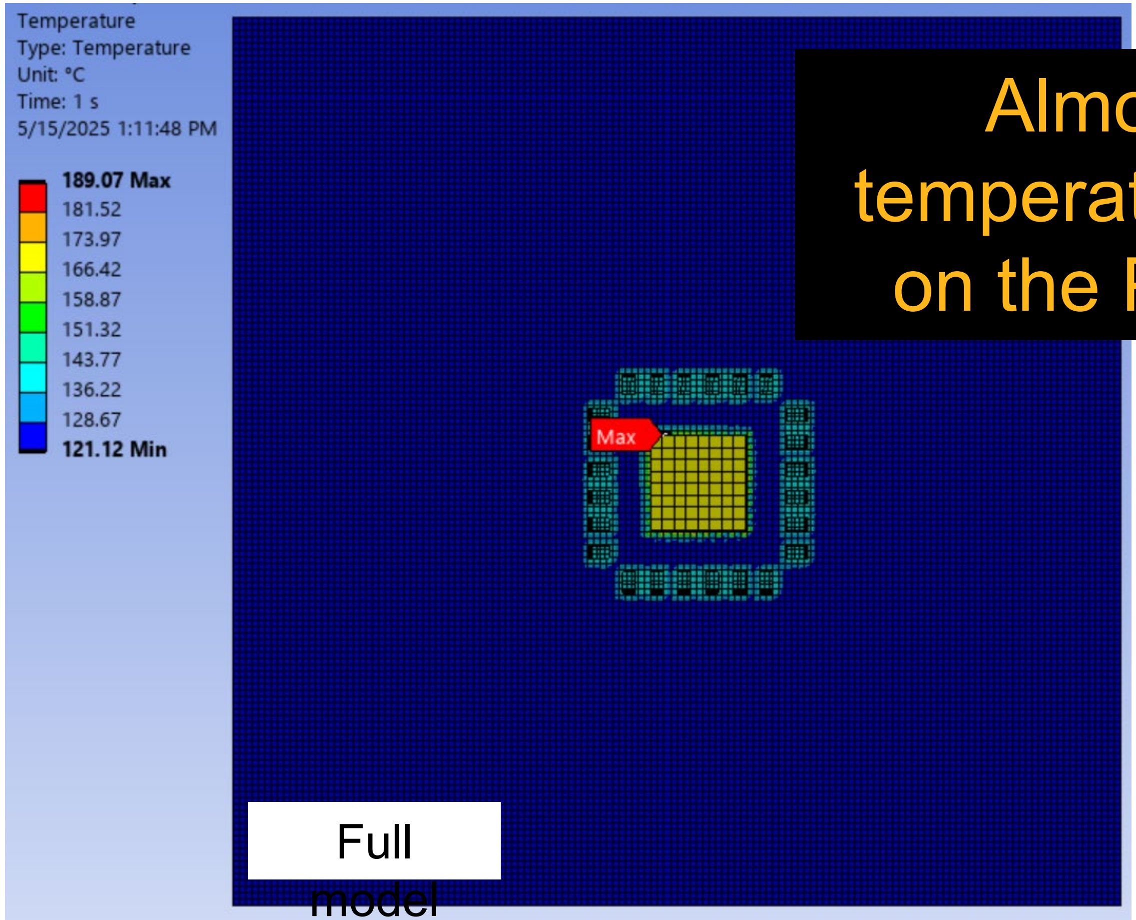
Total Deformation

	Mode	☑ Frequency [Hz]
1	1.	2148.9
2	2.	4250.8
3	3.	4257.1
4	4.	7289.5
5	5.	8498.7
6	6.	8954.7

Using superelement

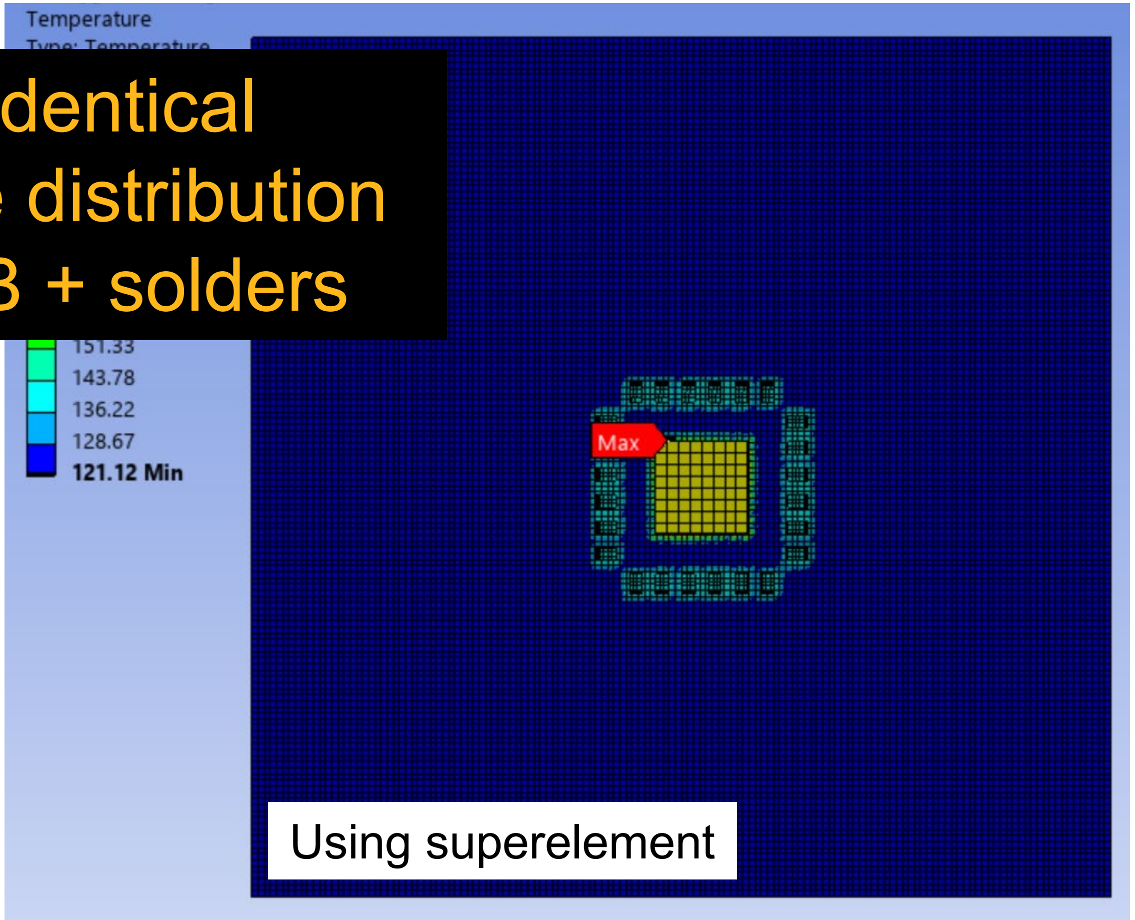
Thermal simulation

- Loading and BCs:
  - 0.75W heat generation at the die
  - Convection applied to all exterior surfaces



Full model

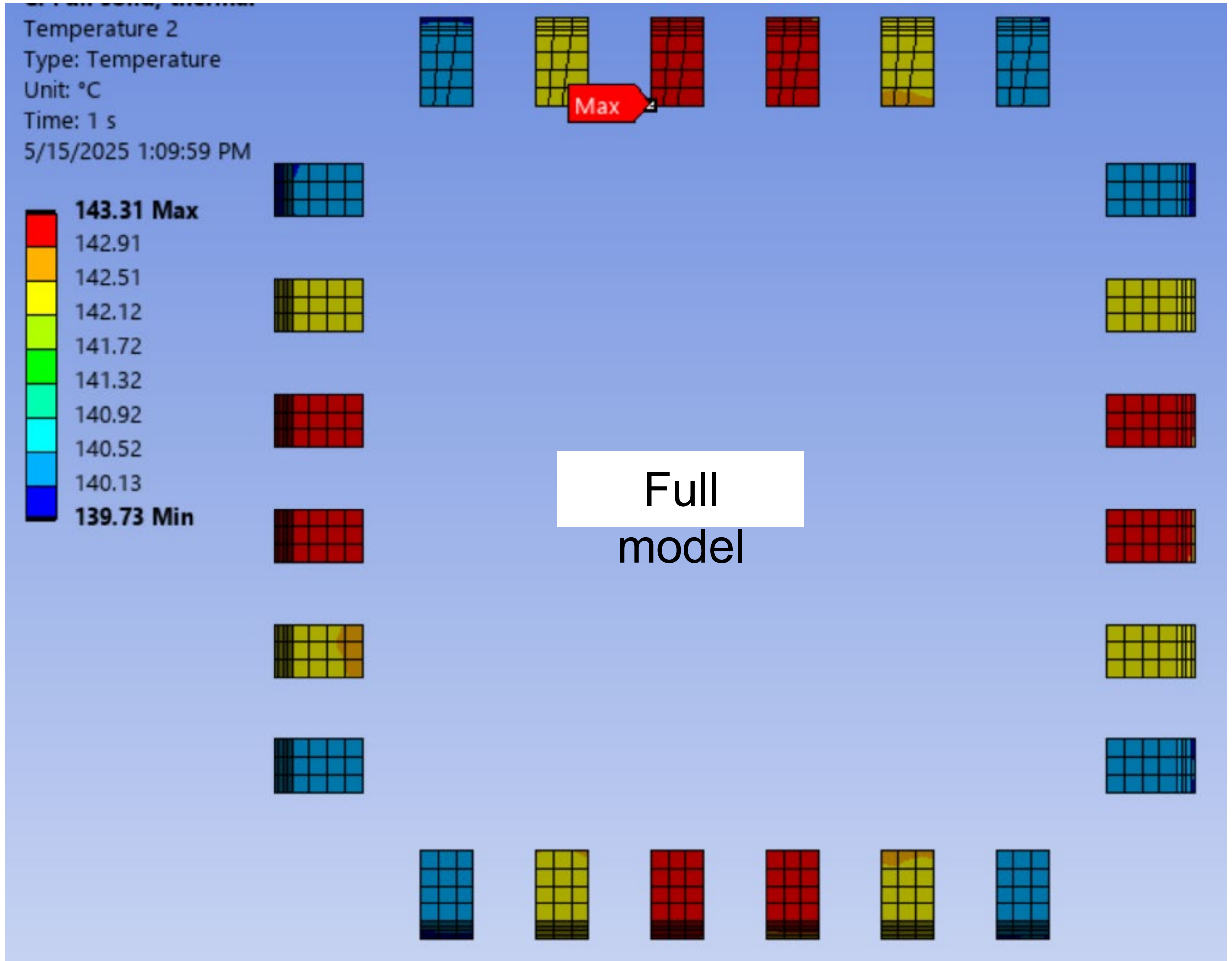
Almost identical temperature distribution on the PCB + solders



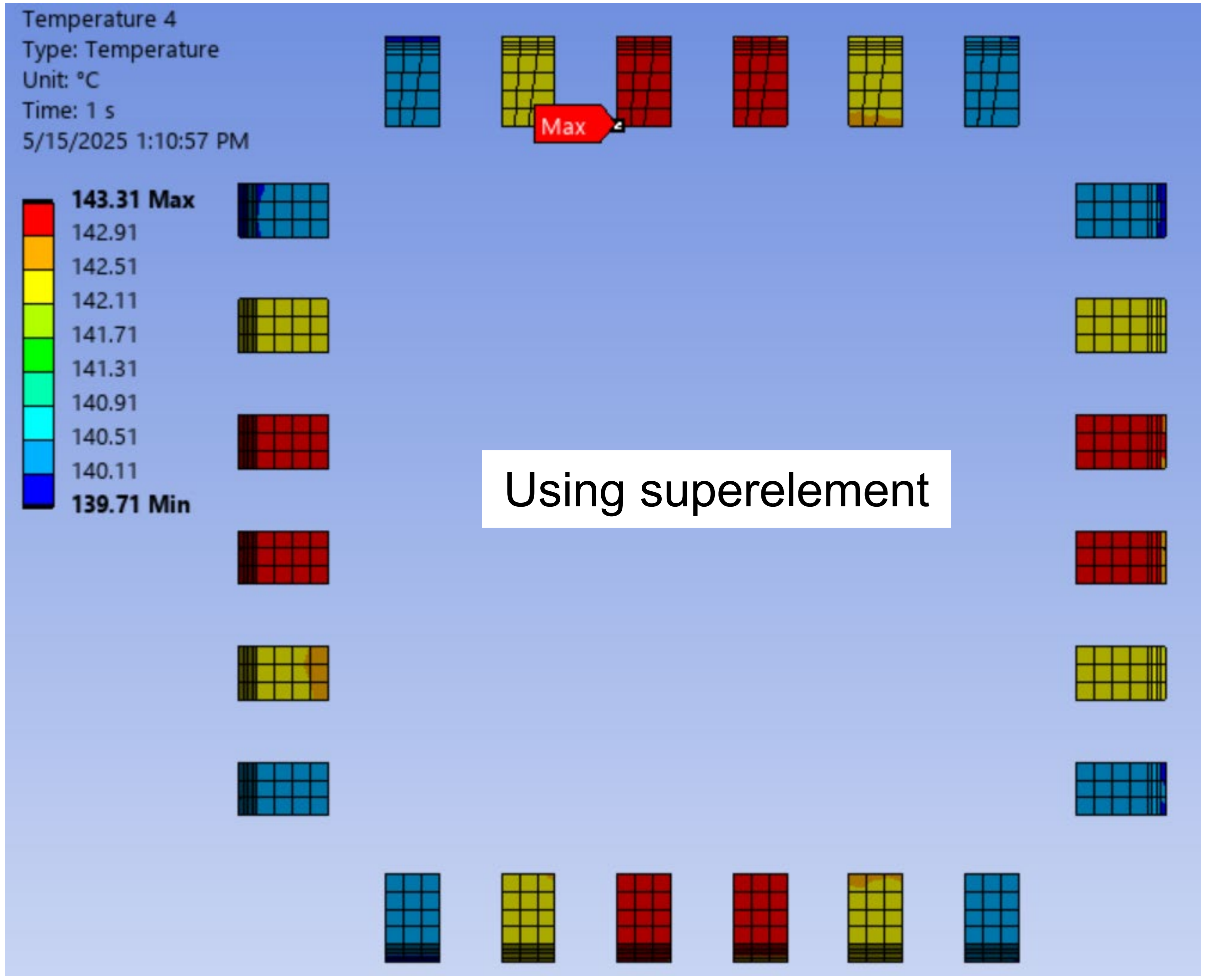
Using superelement

Thermal simulation

- Focusing on just the solder joints



Full model



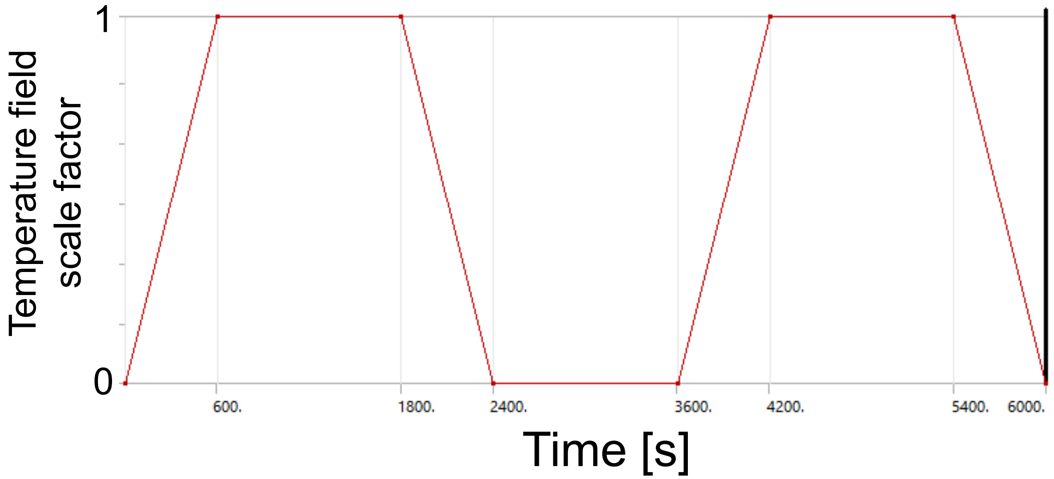
Using superelement

Max temperature difference: **0.02 ℃**

Mean difference: **0.0092 ℃**

Thermal cycling and solder fatigue

- Loading and BCs:
  - Temperature profile obtained from thermal simulation
  - 2 thermal cycles
  - PCB fixed on all 4 sides



- Solder fatigue evaluation:
  - The volume averaged plastic work range between the last two cycles is typically used to correlate with solder fatigue life
  - We compare the plastic work range between t=6000s and t=2400s for each of the 24 solder joints

- Note:
  - The temperature field simulated using SE is used in the SE thermal cycling simulation, and the full-model temperature field is used in the full-model thermal cycling

Thermal cycling and solder fatigue

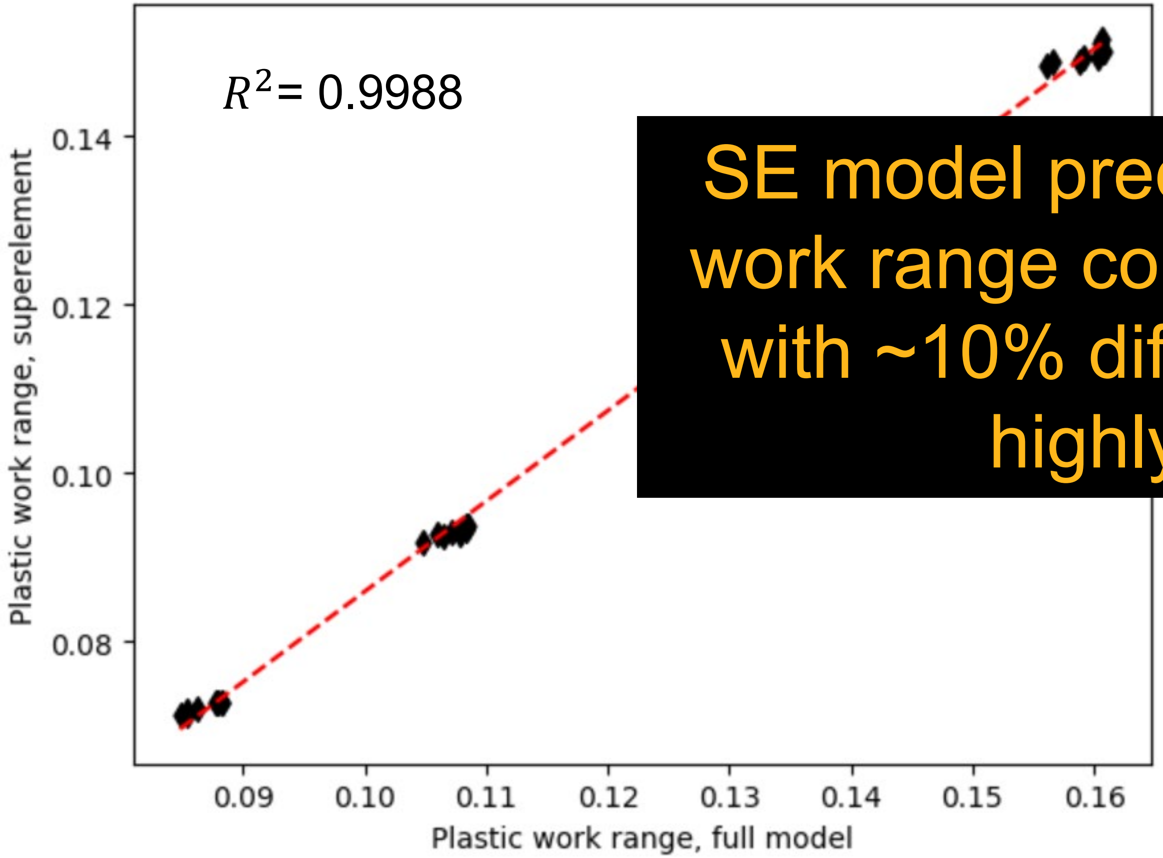
- Computational cost comparison

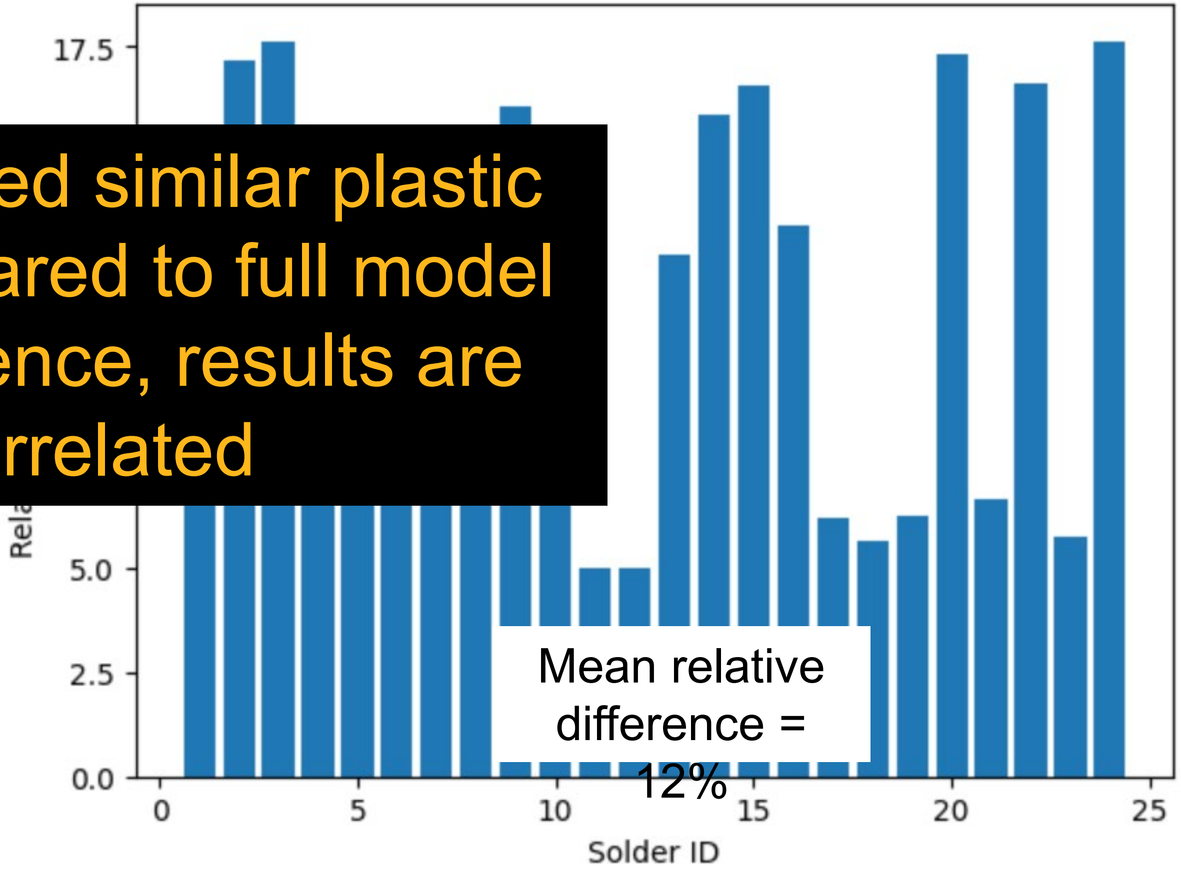
	Total # of DOFs	Solution time [s]	Max RAM used [GB]
Full model	311652	250	1.13 (Iterative solver)
SE model	295485	302	2.93 (Direct solver)

- SE model shows a 5% reduction of total DOFs by replacing the detailed QFN model with a single SE
- Solution time and RAM used is longer for the SE model since all nodes at the interface are retained as master DOFs, which is very memory intensive

Thermal cycling and solder fatigue

- When generating the structural SE, a uniform temperature change in the QFN is assumed (i.e., the thermal load to the SE is controlled by a single ΔT value instead of a full temperature field within the SE)
- In the thermal cycling analysis, thermal load is applied to the SE using the mean QFN temperature, which is a source of difference compared to the full-model solution


R^2= 0.9988

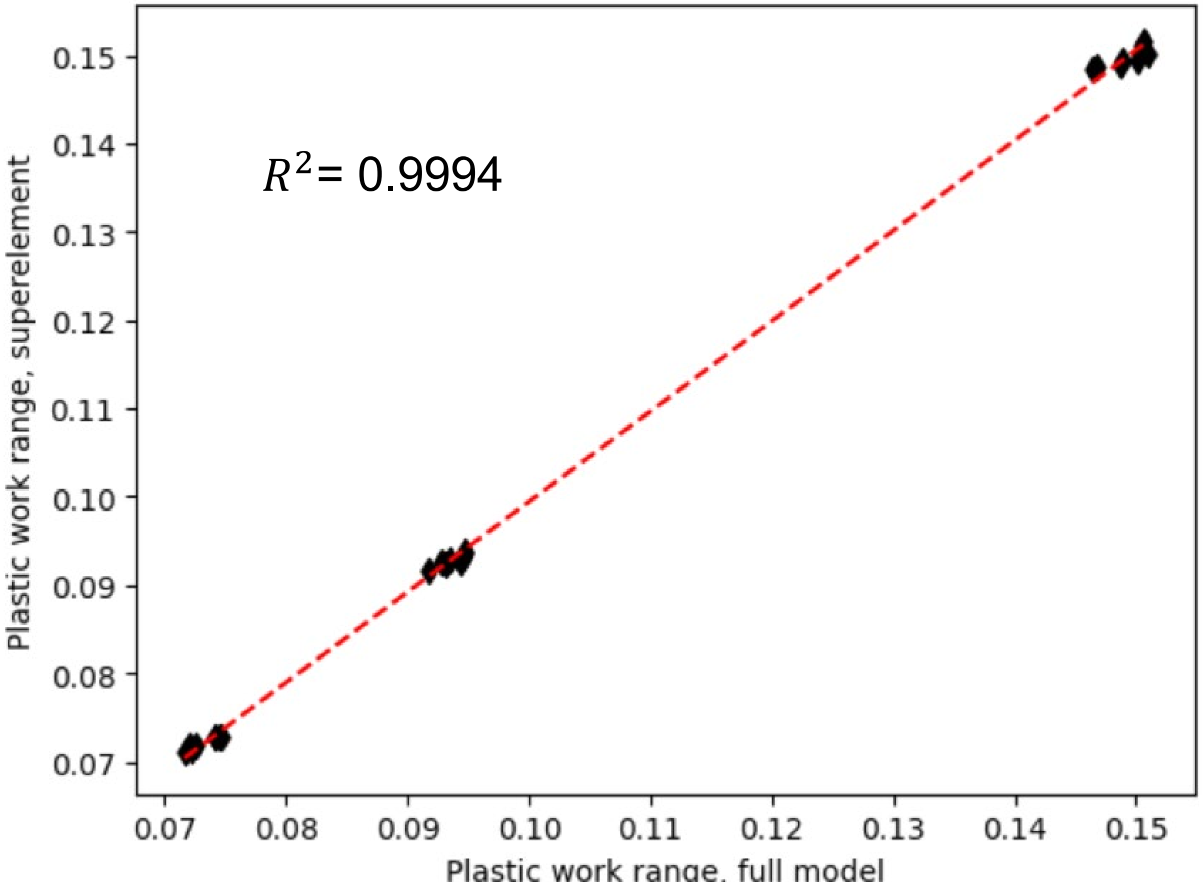


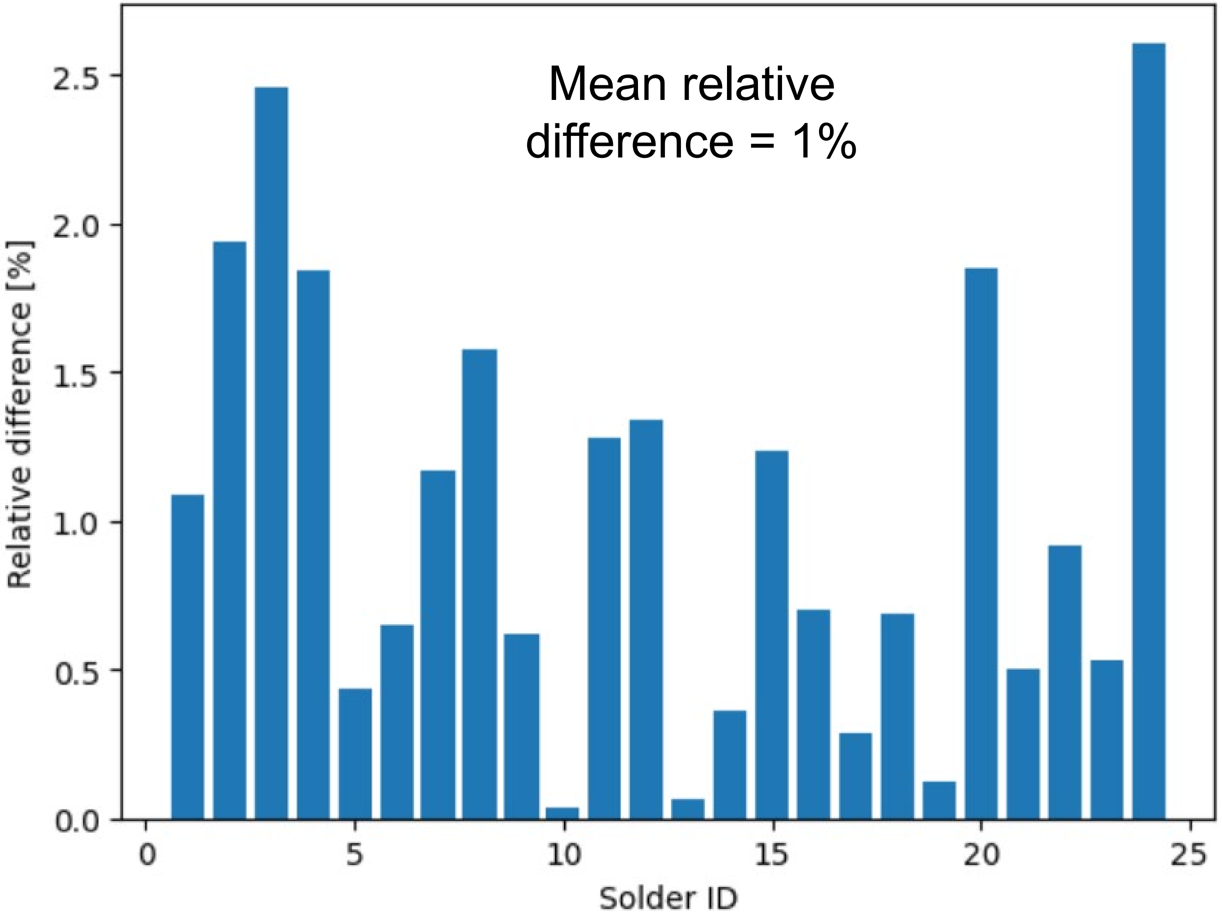
Mean relative difference = 12%

SE model predicted similar plastic work range compared to full model with ~10% difference, results are highly correlated

Thermal cycling and solder fatigue

- If we apply a uniform ΔT to the QFN in the full-model (keeping the mapped temperature field in other bodies) to match the limitation in the SE model, we see an almost perfect match between the full-model and SE predictions of plastic work range





Conclusion

- Ansys provides workflows like Delphi network, superlement and fragility surface to enhance accuracy of board-level electronics reliability simulation with obfuscated IP
- Delphi networks and superelements can be generated automatically to be used in simulations
- Pros & Cons of the Delphi network vs. superelement:

	Pros	Cons
Delphi network	• Standardized format • All information on network definition contained in a single .xml file	• Multiple simulations needed to generate the network • Lumped properties are constant • Is a thermal network only
Superelement	• Can be generated in a single simulation • Can be used in thermal and structural simulations	• Element stiffness is constant

Thank you