AEC-100 Rev. J – Sub Specs

AEC Reliability Workshop Europe 2025
October 8th - 9th, 2025

Agenda

- AEC-Q100 Status
- AEC-Q100 Sub Specs
- New CDC Integration

AEC-Q100 Status

- AEC-Q100 Rev. J was a major revision of the main document. The task group discussed more than 100 change requests and finally achieved release without disapprovals.
- To maintain the overall quality of the standard also the sub specs must be kept up to the current state of the art technologies and requirements.
- So far 3 spec have been identified as outdated and task groups to address a new revision will be formed.
- The remaining Q100 sub specs will be subject of a review to decided if a new revision is needed.

OVERVIEW – Q100 Sub Specs

Spec	Rev.	Release Date	Title
AEC-Q100-001	C	1998-10-09	WIRE BOND SHEAR TEST
AEC-Q100-002	E	2013-08-20	HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST
AEC-Q100-004	D	2012-08-07	IC LATCH-UP TEST
AEC-Q100-005	D1	2012-01-09	NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST
AEC-Q100-007	B	2007-09-18	FAULT SIMULATION AND FAULT GRADING
AEC-Q100-008	A	2003-07-18	EARLY LIFE FAILURE RATE (ELFR)
AEC-Q100-009	B	2007-08-27	ELECTRICAL DISTRIBUTIONS ASSESSMENT
AEC-Q100-010	A	2003-07-18	SOLDER BALL SHEAR TEST
AEC-Q100-011	D	2019-01-29	CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST
AEC-Q100-012	-	2006-09-14	SHORT CIRCUIT RELIABILITY CHARACTERIZATION OF SMART POWER DEVICES FOR 12V SYSTEMS

AEC-Q100-001 Wire Bond Shear Test

- The current spec does not address Cu wire bonding, which is the state of the art wire bond interconnect in automotive today.
- JESD22-B116 provides a suitable test method which can be included to address Au and Cu properly.
- Shear force limits need to be defined by AEC and located in Q100-001. Reasonable and proven values are available and documented in JESD47.
- Approach has been already discussed during Q006 development
- Final call for participation and change requests was send to Technical Committee Members on Sept. 16th
- If your company is able to contribute to the new spec please approach your AEC representative and let him/her answer to the call
- Kick off is planned for end of October

AEC-Q100-005 NVM Reliability

The spec was written mainly for NOR and little NAND where the ECC was managed by the external SOC.

→ **Outdated with respect to state of the art automotive memory technologies, e. g. managed NAND etc.**

Details of Section to revisit

Section	Details	Comments
3.1, 3.3	Low Temp. P/E edurance: Low temp revisit; Low Temp data retention storage life	Min temp. should be lower
3	High temp. and low temp. degradation processes	Revisit
3	Other degradation processes (e.g., Stress Induced Leakage Current (Flash-SILC)	Revisit
3.1.b.1	High Temp cycling	Revisit: 15% accelerated criteria
3.1.b.2	Low Temp cycling	Revisit: 15% accelerated criteria
3.1.c	Cycling	Revisit: Might be N/A for TLC, Quad
3.1.c.3	Wear Leveling	Only applicable to NAND / NOR stand alone
3.1.c.3	ECC section	Outdated
3.2.a	After completing Program/Erase Endurance Cycling testing as described in Section 3.1, the devices shall be programmed with a worst-case pattern for the specific technology, such as topological checkerboard (i.e., where each bit is surrounded by its complement) or all bit cells programmed. A	Revisit: SLC, TLC, Quad
3.2.c	Only data pater verification…	Revisit: N/A anymore?
3.4.e	In the latter case, recoverable (soft) bit data errors occurring during HTOL testing at times beyond the equivalent HTDR life period will not be counted towards HTOL failures but rather as HTDR failures at time points exceeding the qualification stress time requirement.	Revisit: Not practical?
Appendix B	Activation Energy	Revisit

Starting AEC Q100-011 sub committee: Nov 2025

Please contact Sumit Tayal;

Email: stayal@micron.com

Low Temperature Program/Erase Endurance Cycling per Section 3.1 and Q100 Test B3 Low Temperature Data Retention Storage Life (LTDR) per Section 3.3: should be done at <= RM instead of <=55C.

Separate testing for high temperature and low temperature degradation processes is required since, while some degradation processes are accelerated by temperature, Revisit this paragraph

other degradation processes (e.g., Stress Induced Leakage Current (Flash-SILC)) heal with temperature and may not show up in the high temperature flow: Any additional testing?

High Temperature Cycling: Cycling shall be performed at temperature T ≥ 85°C, with total cycling time not exceeding 15% of the accelerated product life. See Appendix A for an example of calculating maximum cycling time at selected cycling stress temperature. Delays in between cycles or between groups of cycles are allowed as long as the delays are spread evenly over the cycling period and the total cycling duration, including delays, does not exceed above rule. 2. Low Temperature Cycling: Cycling shall be performed at temperature of T≤ 55°C Delays in between cycles or between groups of cycles are allowed as long as the delays are spread evenly over the cycling period, and the total cycling duration, including delays, does not exceed 15% of product life.: Revisit Appendix A for clarity on 15%

Cycling is performed continuously, with one cycle being defined as a transition from one state to another and back to the original state (i.e., from "1" to "0" and back to "1"; or from "0" to "1" and back to "0") on all bit cells in the memory array. During the endurance test, each program and erase operation must be verified to have successfully completed and the intended data state is to be validated through a read operation. Endurance test cycling is described below. : For TLC, Quad… might not be applicable needed to be revisited

For memory devices employing on-the-chip Wear Leveling (WL) algorithm, which force all blocks to cycle evenly, the WL algorithm must be disabled such that cells in the array can be stressed to the array specification. If this is not possible, supplier and user must agree on an alternative stressing procedure. Only applicable to NAND / NOR stand alone

For devices containing memory that uses error correction code (ECC) for fault tolerance, this coding algorithm must be disabled such that all cells in the array can be stressed and tested without the effect of error correction techniques. Outdated

After completing Program/Erase Endurance Cycling testing as described in Section 3.1, the devices shall be programmed with a worst-case pattern for the specific technology, such as topological checkerboard (i.e., where each bit is surrounded by its complement) or all bit cells programmed. Alternative patterns are acceptable when agreed to by the user and supplier. With user acceptance, data may also be written using a mode of programming that is different from that specified in the datasheet, to modify the margins of the cells and obtain additional acceleration. For multi-level-cell (MLC) memories, the pattern must include all possible combinations of cell + cell nearest neighbor combinations.: Separate out for SLC, TLC….

activation energy for data retention as described in Appendix B. Revisit

Alternative patterns are acceptable when agreed to by user and supplier. Revisit

Only data pattern verification and non-array altering functional testing is performed at interim read points. This purposely excludes any program or erase testing of the NVM array.: Should be taken out

In the latter case, recoverable (soft) bit data errors occurring during HTOL testing at times beyond the equivalent HTDR life period will not be counted towards HTOL failures but rather as HTDR failures at time points exceeding the qualification stress time requirement. Not practical

AEC-Q100-012 Short Circuit Testing

Wire harness complexity was limited when the spec was developed.

→ Limited number of test conditions sufficient to cover the majority of possible conditions.

Examples of boundary conditions leading to increased short circuit condition variability in vehicles:

- Increased number of semiconductor switches in power distribution
- New E/E architectures, e. g. zone architectures
- Fuse replacement by semiconductor switches

Conclusion: Rework of test procedure and or conditions necessary.

- Final call for participation and change requests was send to Technical Committee Members on Sept. 16th
- If your company is able to contribute to the new spec please approach your AEC representative and let him/her answer to the call
- Kick off is planned for end of October

Aspects to prioritize revision

Remaining specs will be reviewed for need of revisions

Aspects taken into account

- Change in use cases leading to different mission profiles
- New E/E architectures
- New technologies
- New materials

Overall target is to keep the coverage of the state of the art electronics in passenger cars.

Integration of new CDC

- New AEC-Q100 CDC has been developed
- However AEC-Q100 Rev. J still has a snapshot of the old CDCQ document included
- For a proper reference AEC-Q100 needs a minor revision: AEC-Q100 Rev. J1
- AEC-Q100 Rev. J1 will have no content change besides the integration of new CDC

→ **Limited ballot send out Oct. 2nd**

- Target is publication of both in parallel (CDC and Rev. J1).

Any further questions?