Automotive Electronics Council
Component Technical Committee

Automotive Electronics Reliability Workshop

AEC WIDE BAND GAP (WBG) TASK GROUP

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*on behalf of the **AEC WBG Task Group***

Bordeaux, October 8th 2025

Agenda

- Motivation behind the AEC task group for Wide Band Gap (WBG)
- The defined working groups and timeline of implementation of the SiC guideline
- Structure of the AEC SiC standardization document:
  - SiC Appendix
  - Main differences compared to AEC-Q101
  - Specific SiC qualification test concepts
- GaN standardization
- Q&A session

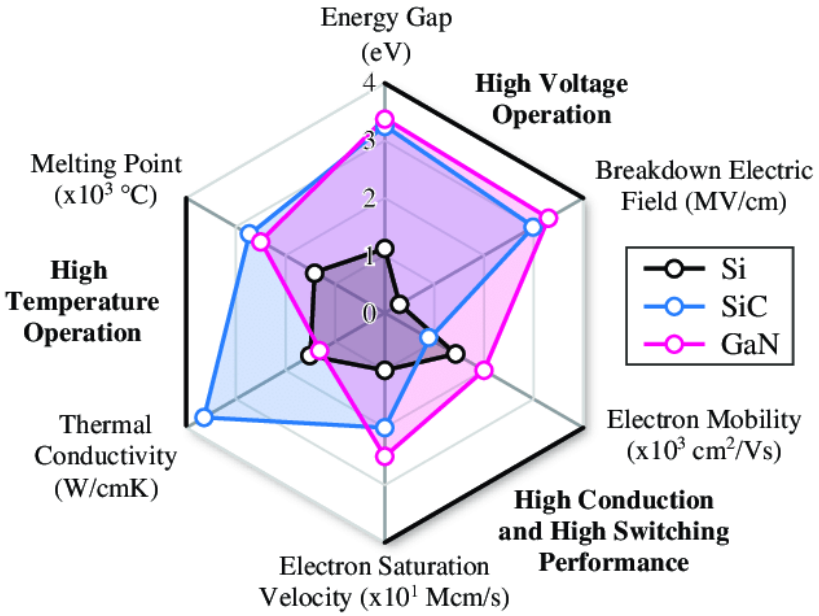
Motivation behind the AEC task group for Wide Band Gap (WBG)

- Today's AEC-Q101 does not adequately cover WBG semiconductors:
  - WBG has some failure mechanisms that silicon does not have, so we may need additional stress tests.
  - WBG can be used in different ways than silicon devices, so we may need different or additional stress conditions (voltage combinations, higher maximum temperature, wider temperature extremes).
  - Bare die versus discrete qualification is also considered.
- Goal is to expand Q101 to define the stress-test-driven qualification requirements for WBG semiconductors, in bare die or discrete form.

Wide Band Gap Materials – Brief Introduction

- Wide Bandgap (WBG) materials such as SiC and GaN are defined by the energy required for an electron to jump from the valence band to the conduction band

physical properties	Si	4H-SiC	GaN
Band gap [eV]	1.12	3.2	3.26
Breakdown field [MV/cm]	0.3	~3.1	~3.3
ideal bulk mobility [cm²/V/s]	1400/450	800/115	2100/2DEG/-
electron saturation vel. [cm/s]	1e7	2e7	2.2e7
thermal conductivity [W/cm/K]	1.5	~3.7	1.3



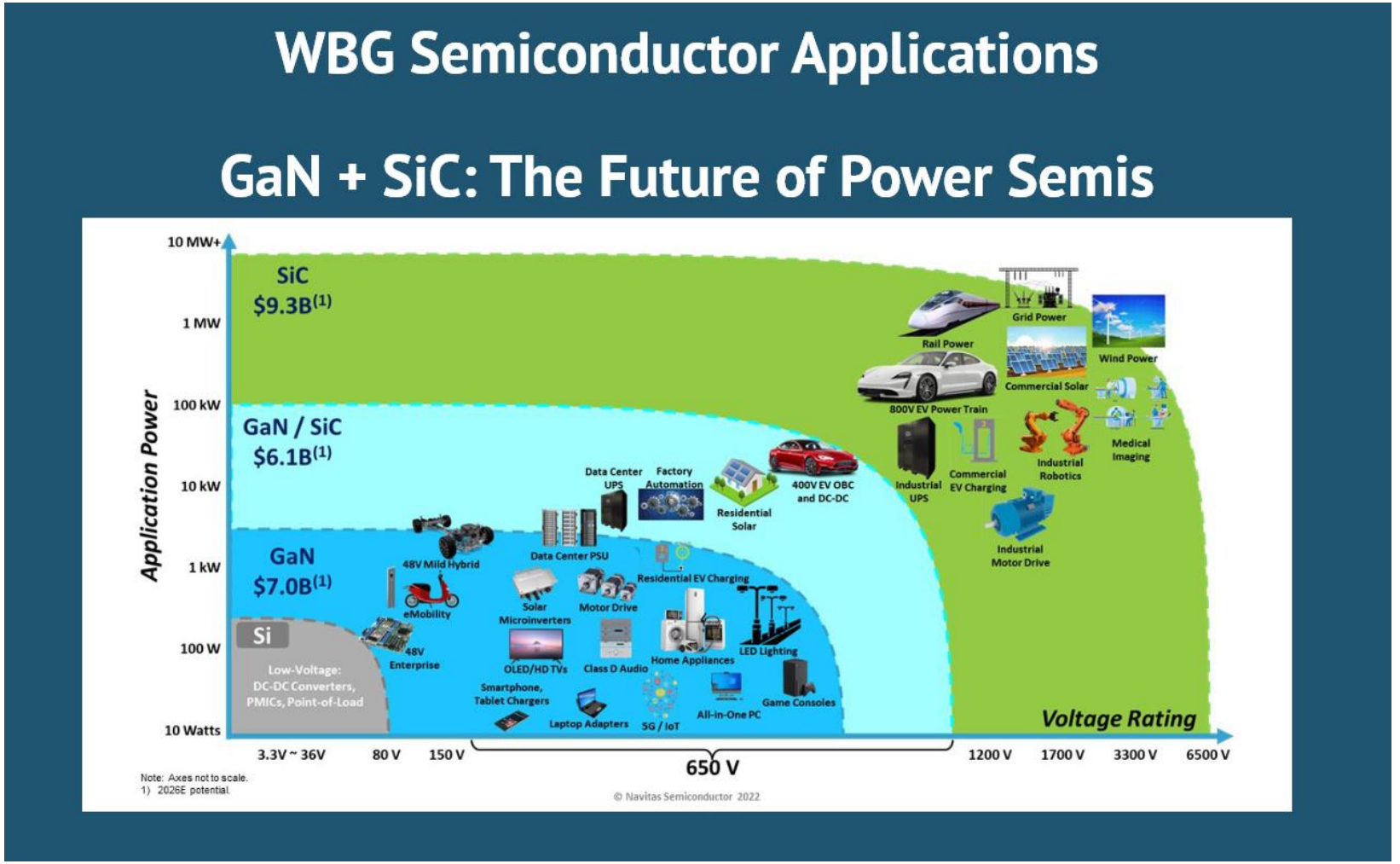
Key material properties of Si, 4H-SiC and GaN at 25°C and atmospheric pressure *

- WBG materials have important advantages over Si:
  - Higher operating temperatures
  - Higher voltages and power
  - Faster switching
  - Overall better efficiency

- Strong growth in SiC and GaN power MOSFETS in Automotive mainly driven by Hybrid and EV market.

* *Source*: New FOM-Based Performance Evaluation of 600/650V SiC and GaN Semiconductors for Next-Generation EV Drives, D. Cittanti, Research Gate, Jan 2022

WBG Material Applications



Courtesy of Navitas: https://navitassemi.com/introduction-to-wide-bandgap-semiconductors/

The four working groups

WG1: Failure mechanisms

- *Purpose*: identify and describe the failure mechanisms related to WBG technology, when operated for an automotive application. Create a connection between the failure mechanisms and the expected lifetime and robustness tests to be developed in the guideline

WG2: Testing and characterization

- *Purpose*: describe the requirements for testing, specific to WBG. Describe the minimum characterization tests in correlation with the main Automotive requirements and the failure mechanisms

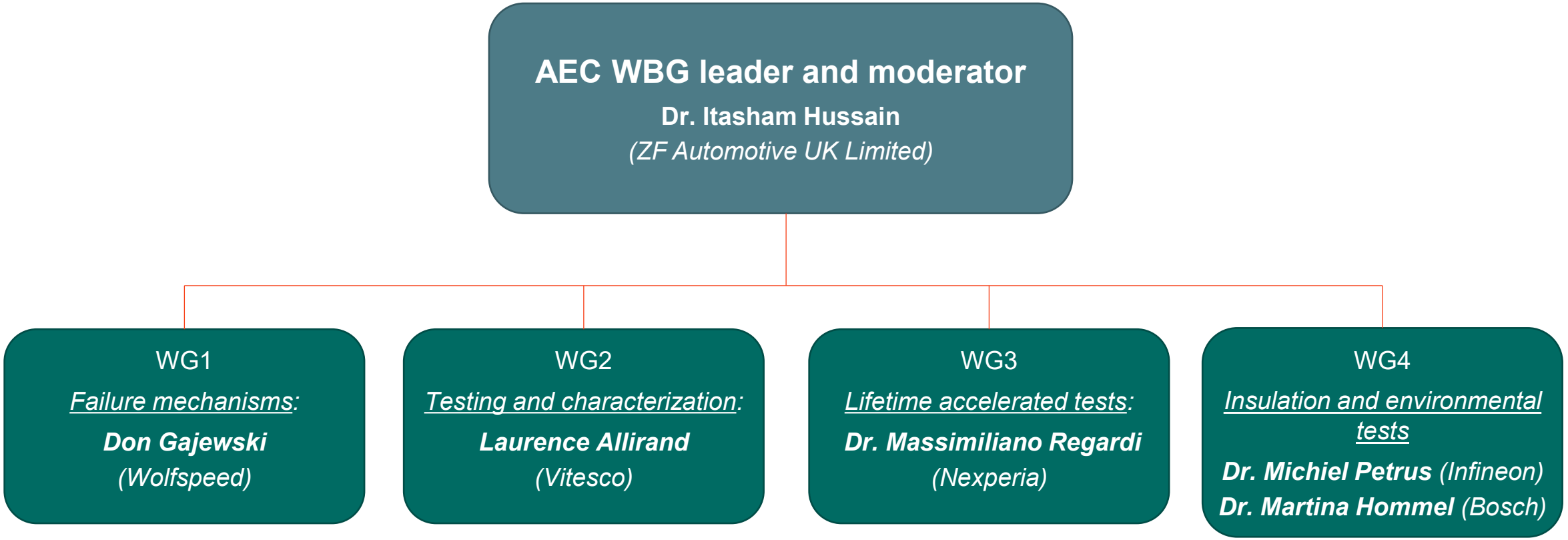
WG3: Lifetime accelerated tests

- *Purpose*: Document the lifetime tests (test to pass) to be considered for products on WBG technologies. Define a static and dynamic set of reliability tests

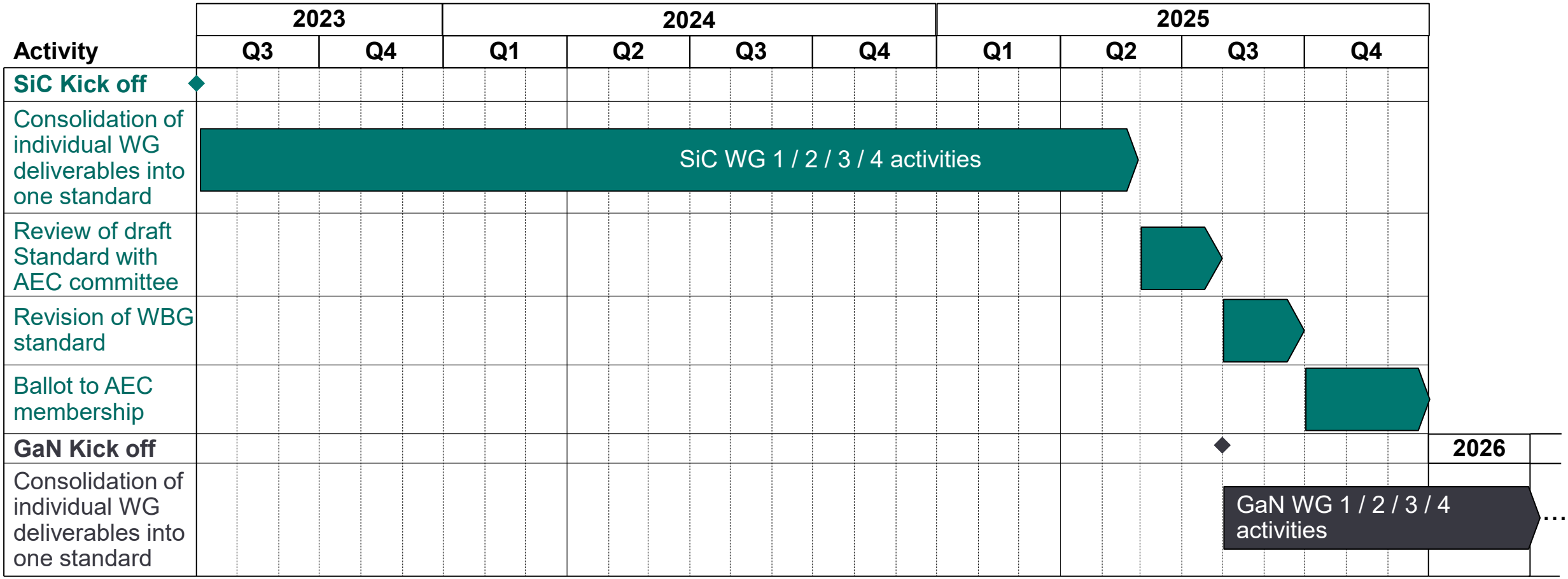
WG4: Insulation and environmental tests

- *Purpose*: Document the insulation and environmental tests to be considered for WBG. Define a set of static and dynamic reliability procedures. This group should focus on the interaction between the technology and the package

AEC WBG SiC organization



Wide Band Gap Task Group Status Update



AEC SiC planned as appendix to the existing AEC-Q101

AEC WBG SiC specific content

Description of SiC failure mechanisms

- Gate oxide wear out and extrinsic
- Charge trapping & mobile ion drift (threshold voltage drift)
- BPD/SSF defect conversion (bipolar stability)
- Reverse bias
- Single-event burn-out (neutrons)
- Short circuit
- (Thermo-)mechanical (delamination, cracking, stress-migration, etc.)
- Unclamped inductive switching
- dVds/dt
- Hot carrier injection
- Electromigration

SiC testing and characterization

- VTH characterization requirements
- Short circuit test requirements
- Bipolar degradation
- ESD test requirements
- Failure criteria

Lifetime and insulation tests

Lifetime accelerated tests

- HTRB test concept (VGS=0 and VGS,neg)
- HTRB and HTGB biased cool down
- Gate Switching Stress test concept
- Unclamped Inductive Switching (UIS)
- Early Life Failure Rate (ELFR)

Insulation and environmental tests

- Perform H3TRB instead of HAST
- Perform H3TRB at VDS = 80%
- Perform UHAST instead of AC
- Definition of bare die relevant tests:
  - H3TRB
  - TC
- Supplier chooses appropriate carrier package for bare die

Structure of AEC SiC standardization

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AEC-Q101 Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications

Appendix 8: Qualification of SiC

AEC-Q101_007
Miscellaneous SiC-Test Methods

- Body Diode Conduction test
- Gate Switching Stress
- Early Life Failure Rate

AEC-Q101_008
Short Circuit test on SiC

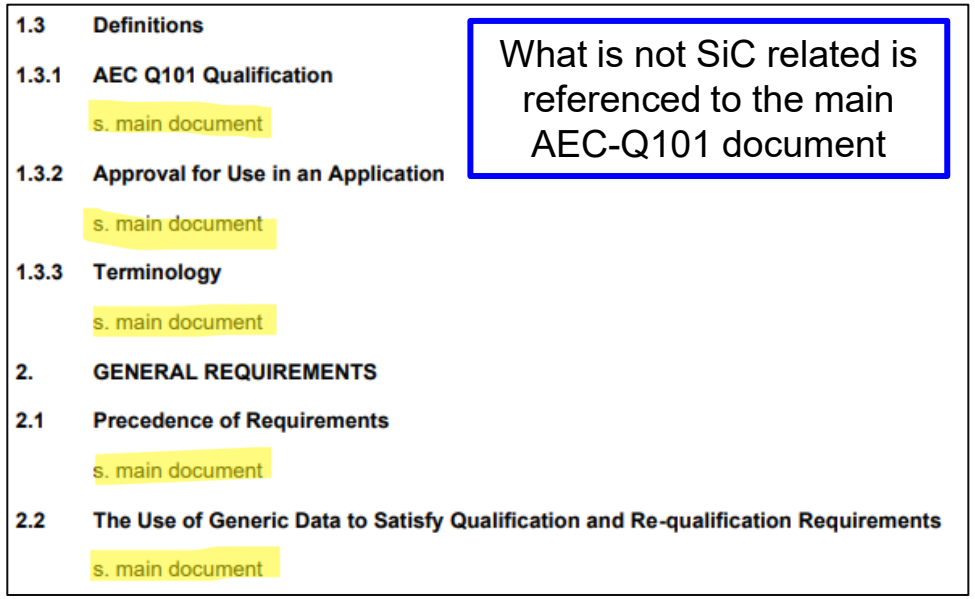
Scope and introduction of SiC Appendix

SCOPE of Appendix 8

The appendix 8 defines minimum stress test driven qualification requirements and references test conditions for qualification of **discrete** semiconductors (e.g. transistors, diodes, etc.) and **bare dies** based on **SiC technology**. A SiC-based discrete semiconductor is defined by having at least one SiC based semiconductor in the device (e.g. SiC-MOSFET or SiC-diode).

General remarks for the qualification of SiC-based bare die products

For the qualification of a bare die product an **appropriate test package** shall be used, based on **mutual agreement between user and supplier**. The supplier shall provide a general recommendation for the assembly method, i.e. if the die and metallization were developed for soldering, sintering, etc..



What is not SiC related is referenced to the main AEC-Q101 document

The Appendix receives and applies the **JEDEC-JC70** documents into the Automotive context under the scope of AEC

JEP183A	Guidelines for Measuring the Threshold Voltage (VT) of SiC MOSFETs	2023-01
JEP192	Guidelines for Gate Charge (QG) Test Method for SiC MOSFET	2022-12
JEP194	Guideline for Gate Oxide Reliability and Robustness Evaluation Procedures for Silicon Carbide Power	2023-02
JEP197	Guideline for Evaluating Bipolar Degradation of Silicon Carbide Power Devices	2023-11
et al.	⋮	

Qualification of a part in a new technology

Technology relevant tests have to be performed one time on parts manufactured on a new or unproven technology

New or unproven technology = no qualification exists or no re-qualification results can be referenced or associated for the failure mechanisms in the test scope

Tab.2 SiC indicates which tests are technology relevant and defines the conditions under which they have to be **repeated** in the case of a change

HTRB 2 (with neg Vgs) shall be performed in the case of:
- a new process with changed technology design (e.g. new EPI), with a potential effect from negative VGS on the VDS or on breakdown voltage
- an increase or a change of the electric field affecting the GOX stability or the edge termination at negative gate biasing1000 hours at the maximum specified DC reverse voltage and specified $T_{J(max)}$.

Apply the typical off-state gate bias during stress the test. Bias should only be removed upon cool down to 55°C+/-5°C or lower in accordance to JESD22-A108G (paragraph 5). When the maximum DC Reverse Voltage is not used, report the DC Reverse Voltage used during qualification, and justify the reason for applying a lower DC Reverse Voltage.
TEST before and after HTRB 2 as a minimum.

- Technology relevant

ADDITIONAL REQUIREMENTS

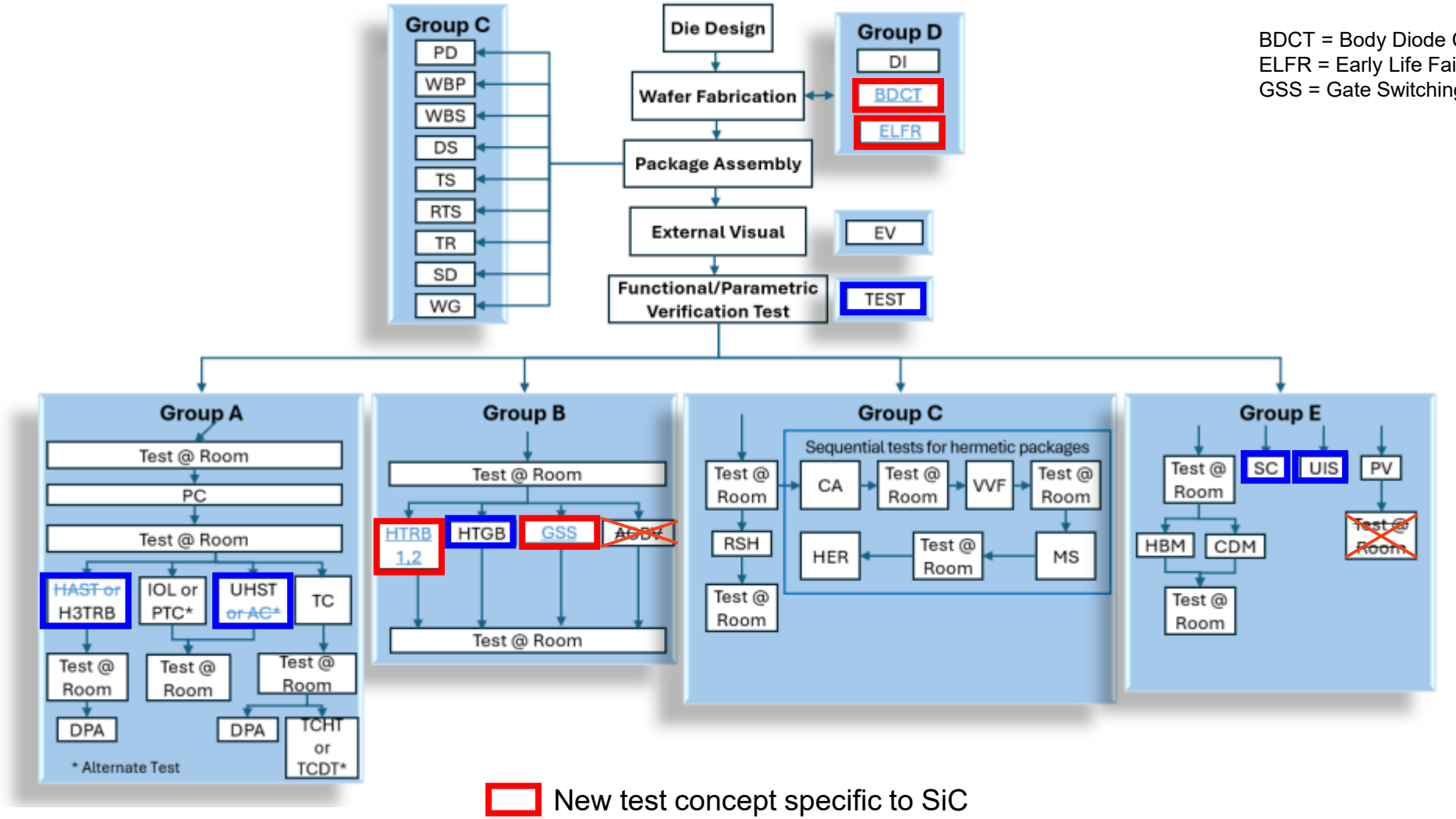
GSS shall be performed to assure the long-term reliability of the gate and gate-oxide of the device under VGS switching conditions. For example, it can be used to address (1) gate-oxide breakdown, (2) threshold voltage instability, (3) the migration of ionic contaminants in the gate oxide and/or interface, due to gate oxide electric field under repetitive switching condition.
Test per duration set to cover the total number of switching cycles until end of application profile (EoAP), as described in chapter GSS
The test shall be performed at the worst case application temperature, further details in AEC-Q101-007.
Switching from $V_{GS,min}$ to $V_{GS,max}$ (absolute max/min ratings as per datasheet, including transients). The slope of the switching curve should not be slower than in the applications. If the application slope is not known then 0.5 V/ns shall be used. A frequency of 500kHz is recommended, switching frequency ≤ 2Mhz are allowed, as long as the VGS static state has been reached and over- and undershoots are minimized

- Technology relevant

Early life failure rate (ELFR) testing for SiC MOS power devices, according to chapter ELFR.
The test is to demonstrate MOS gate reliability and Vds reverse-bias MOSFET reliability, ensuring that the failure rate lies below an accepted confidence level.
Test is to be performed at Tj,max, for a) 24hrs under HTRB conditions, and b) 24hrs under positive HTGB conditions.
When the test conditions in Chapter ELFR are not used, report the test conditions used during ELFR test .
Devices shall remain within datasheet specs to pass the ELFR test.
Both ELFR tests are needed for new devices or processes, although for a process change only one of these tests may be needed.

- Technology relevant

AEC-Q101 Stress Test Flowchart for SiC



BDCT = Body Diode Conduction Test
ELFR = Early Life Failure Rate
GSS = Gate Switching Stress

New test concept specific to SiC

Revised test conditions or test approach for SiC

Definition of Test Failure after Stressing only for SiC devices

1. Same baseline definition of test failure and drift criteria as per AEC-Q101
2. Exception for $V_{GS(th)}$ and R_{DSON} for SiC specific tests
3. Introduction of the part to part range of shift, mainly for bare die

2.4 Definition of Test Failure after Stressing

Test failures are defined as devices exhibiting any of the following criteria:

a. Parts not meeting the electrical test limits defined in the first user's part specification or appropriate supplier part specification. Minimum test parametric requirements shall be as specified in Appendix 5.

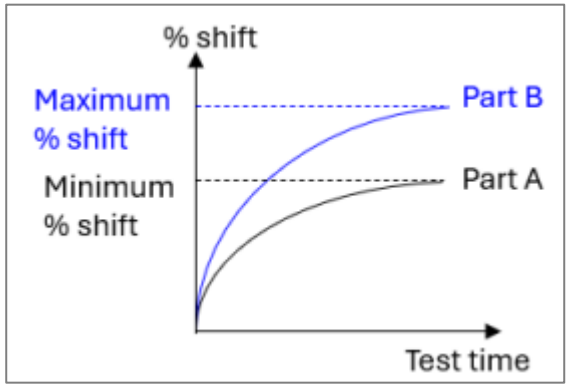
b. Parts not remaining within ± 20% of the initial reading of each test after completion of *all tests* ~~environmental testing.~~ ~~For leakages below 100nA, tester accuracy may prevent a post stress analysis to initial reading.~~

- For IOL, PTC and TC tests on products with RDSon ≤ 2.5 mOhm max, the allowed value for the shift of RDSon is ≤0.5 mOhm.
- ~~For breakdown voltage only, a shift of >20% of the initial measured value is a failure only if the final reading is within 20% of the datasheet maximum value.~~

Specific to SiC

- For $V_{GS(th)}$ and R_{DSON}, part to part variation of shift within each qualification lot for selected stress tests (HTGB positive, HTGB negative, GSS) is critical and must be monitored.
- Part to part range of shift = maximum % shift – minimum % shift.
- Part to part range of shift must be reported to user including all part by part variations

Example of part to part range of shift



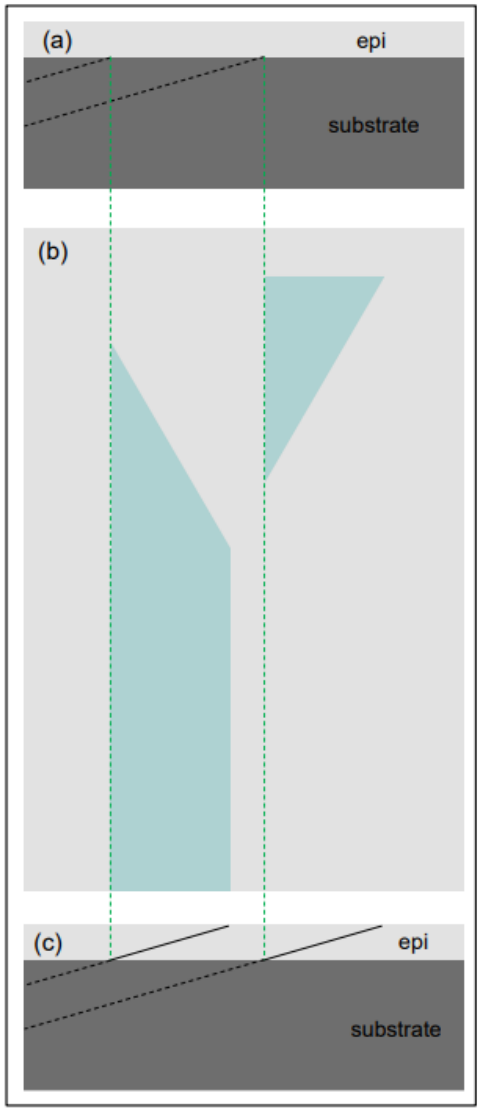
Body diode degradation

What is the body diode degradation

- SiC body diode degradation is a form of bipolar degradation in SiC MOSFETs caused by basal plane dislocations (BPDs) and resulting stacking faults (SSFs) in the drift region
- The SSF are activated by forward-bias current stress.
- The recombination energy from electron-hole pairs during the forward-bias operation creates and expands these stacking faults.
- BPDs are inherent defects in the SiC material, and under current stress, they act as nucleation sites for stacking faults.
- It is a defect related to raw material

How does the body diode degradation manifest

- Increased Forward Voltage (VF): A key indicator is an upward trend in the body diode's forward voltage drop (V_{SD}).
- Increased On-Resistance (R_{DSon}): BPDs and SSFs can affect carrier lifetime and mobility, leading to higher on-resistance.



SSF formation mechanism *

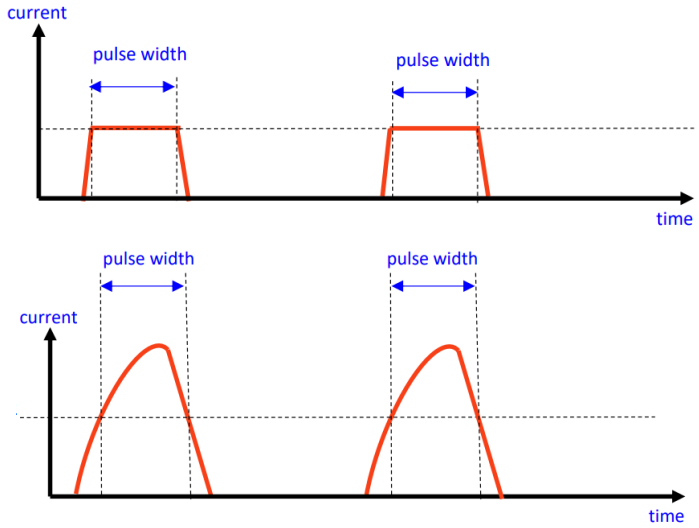
Before SSF form, there are 2 BPDs near the surface (a).
In (b) and (c) the SSFs have formed, grown and reached the epi surface

Before body diode current stressing, the BPDs are confined to the substrate just below the epitaxial layer as shown in the cross-sectional drawing in (a).
(b) and (c) show the SSF expansion reaching the top of the epitaxial layer

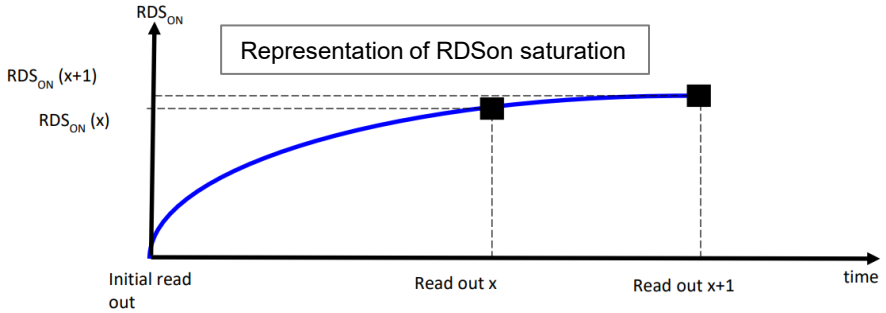
* Source: JEDEC JEP197 - Guideline for Evaluating Bipolar Degradation of Silicon Carbide Power Devices

Body Diode Conduction Test

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Body-Diode-Conduction test	BDCT	D2	3	D, G	77	3	RDSon drift saturation	AEC Q101-007	SiC MOSFET and diode Required for new technology release. Required for new substrate supplier and new epitaxy supplier. Not required if supplier can prove that quality (BPD density) of new substrate supplier and new epitaxy supplier is improved. Evidence shall be provided upon request. Required to evaluate process/ design changes related to substrate and epitaxy which will increase plasma density. • Technology relevant



- The dominant driver in bipolar degradation failure mechanism is the current, therefore the target is to set this stressing current as high as possible. The **maximum repetitive body diode pulsed current** for a given technology must be applied
- Recommended **current pulse shape** is a square shape, but triangular current pulse shapes are allowed for this test
- **Minimum pulse width must be 500ns** and recommended pulse width is above 1µs, otherwise according to maximum pulse width defined in datasheet.
- Minimum test duration is **10 hours of cumulative body diode conduction time**



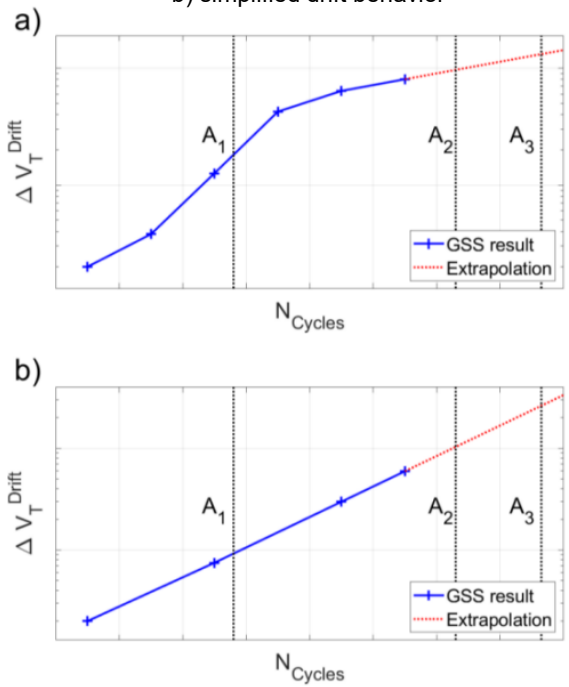
Test stops when R_{DSon} shift has reached a saturation:

$$\text{Saturation} = \frac{RDSon\ (x+1) - RDSon\ (x)}{RDSon\ (x)}$$

Gate Switching Stress

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS (continued)									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Gate switching stress	GSS	B3				3 Note B	0 Fails	AEC Q101-007 JEDEC JEP195	GSS shall be performed to assure the long-term reliability of the gate and gate-oxide of the device under VGS switching conditions. For example, it can be used to address (1) gate-oxide breakdown, (2) threshold voltage instability, (3) the migration of ionic contaminants in the gate oxide and/or interface, due to gate oxide electric field under repetitive switching condition. Test per duration set to cover the total number of switching cycles until end of application profile (EoAP), as described in chapter GSS The test shall be performed at the worst case application temperature, further details in AEC-Q101-007. Switching from $V_{GS,min}$ to $V_{GS,max}$ (absolute max/min ratings as per datasheet, including transients). The slope of the switching curve should not be slower than in the applications. If the application slope is not known then 0.5 V/ns shall be used. A frequency of 500kHz is recommended, switching frequency ≤ 2Mhz are allowed, as long as the VGS static state has been reached and over- and undershoots are minimized • Technology relevant

Extrapolation with a) multiple power laws or
b) simplified drift behavior



- This test is used to assure the **long-term reliability of the gate and gate-oxide** of the device under test, while switching the device between different gate-source voltage levels
- Switch from V_{GSmin} to V_{GSmax} (absolute max/min ratings as per datasheet, including transients)
- Any **switching frequency** ≤ 2Mhz, with a typical of 500kHz, as long as the V_{GS} static state has been reached and over- and undershoots are minimized.
- Test to cover the total number of switching cycles until end of application profile (EoAP). Extrapolation is allowed if power law has settled

HTRB with different V_{GS} applied

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS						
STRESS	**ABV**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
High Temperature Reverse Bias (Vgs = 0V)	HTRB 1	77	3	0 fails	MIL-STD-750-1 M1038 condition A (for diodes, rectifiers and Zeners) M1039 condition A (for transistors)	• 1000 hours at the maximum specified DC Reverse Voltage and specified $T_{J(max)}$. • Apply a gate bias (V_{GS}) of 0V during the stress test.
High Temperature Reverse Bias (Vgs negative)	HTRB 2	77	3	0 fails		• 1000 hours at the maximum specified DC reverse voltage and specified $T_{J(max)}$. • Apply the typical off-state gate bias during the stress test • Technology relevant

V_{GS} = 0V

1. Considers channel leakage (channel not completely off)
2. Offers a design comparison
3. Not preferred by Customers but still applied by many (easy to have)

V_{GS} negative

1. Switch off channel completely
2. Worst case for the Gox shielding (design comparison), especially for trench design
3. Preferred by Customers, used in most applications, but often needs a gate driver (extra implementation)

Insulation and environmental tests

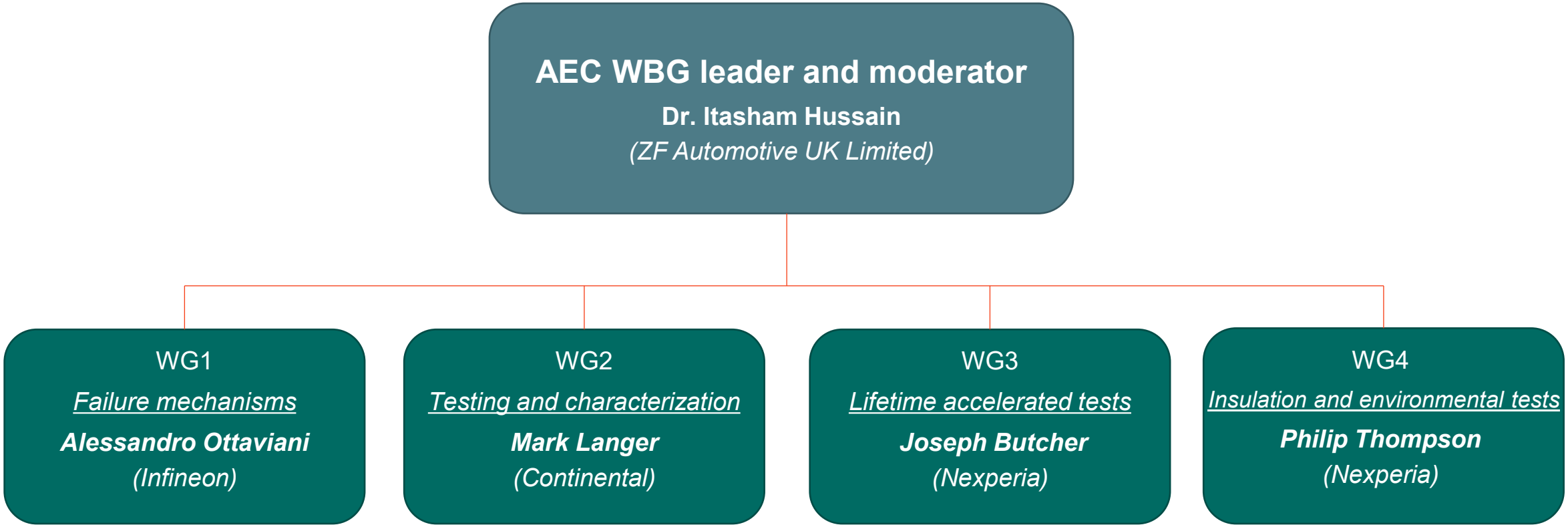
Test	Abbr.	#	Discrete	Bare die
Pre-conditioning	**PC**	**A1**	• No changes to AEC-Q101	• Test not required for bare die
~~Highly accelerated stress test~~	~~HAST~~	~~A2~~	~~• For SiC: use H3TRB instead of HAST, due to risk of arcing~~	
High humidity, high temperature reverse bias	**H3TRB**	**A2**	• **Remove limit of max. 100V in AEC-Q101**	• **Test according to updated SiC conditions** • Test package based on mutual agreement between user and supplier • Supplier has to give a general recommendation for the assembly method
Unbiased Highly accelerated stress test	**UHAST**	**A3**	• No changes to AEC-Q101	• Test not required for bare die
~~Autoclave~~	~~AC~~	~~A3 alt~~	~~• Jedec document no longer valid~~	
Temperature cycling	**TC**	**A4**	• No changes to AEC-Q101	• **Test according to AEC-Q101** • This test is relevant for bare die and focusses on the robustness of the interconnects within the metallization and passivation • Test package based on mutual agreement between user and supplier • Supplier gives a general recommendation for the assembly method
Temperature cycling hot test	**TCHT**	**A4a**	• **Minimum 125°C**, no further change to AEC-Q101	• Test not required for bare die
TC delamination test	**TCDT**	**A4a Alt**	• No changes to AEC-Q101	• Test not required for bare die
Intermittent Operational Life	**IOL**	**A5**	• No changes to AEC-Q101	• Test not required for bare die
Power Temperature Cycling	**PTC**	**A5 Alt**	• No changes to AEC-Q101, IOL is preferred	• Test not required for bare die

GaN standardization

- Technical discussion and the consolidation of deliverables on GaN standardization has kicked off in Q3 2025.
- GaN standardization will follow the same goal and modus operandi as for SiC.
- Same organizational structure and working groups.
- The list of experts and participants is still under consolidation
- *Challenge*: limited participants, unbalanced attendees in WG4

Experts are welcome. If you want to actively contribute please contact:
Dr. Itasham Hussain <Itasham.Hussain@zf.com>

AEC WBG GaN organization



Time for your questions

Thank you.