# New ESD Contact-Based Charged Device Models (CDM) Are Needed to Keep Up with ESD Roadmap

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# Automotive: memory and storage are everywhere

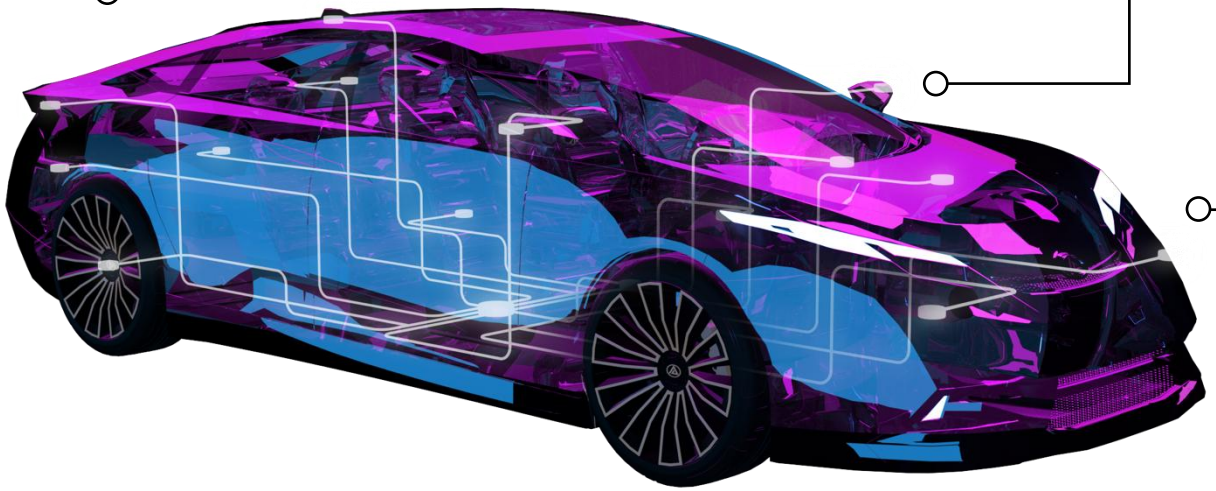
**Centralized storage**
- NAND (ultra-endurance SSD)
- DRAM
- MCP

**Powertrain**
- NOR
- DRAM
- NAND (SLC NAND)

**Enriched cabin**
- DRAM
- NAND (e.MMC/UFS/SSD)
- NOR
- MCP

**Connected**
- e.MMC
- NOR
- MCP

**ADAS L2-L5**
- DRAM
- NAND (e.MMC/UFS/ultra-endurance SSD)
- NOR
- MCP



# Topics

1. Introduction
2. ESDA 2024 roadmap - ESD trends
3. CDM Test model overview (JS-002)
4. CDM Variance factors + controls
5. Variance Issue #1: Waveform variation gets worse at lower stress levels.
   - Review Contact CDM options and progress
6. Variance Issue #2:  Fail level variation due 3Zap wear out
   - Review key 1vs3Zap AEC 2024 Presentation Slides (Waki-san, et al)
   - Review highlights from NXP 2024 paper
7. AEC ESD Specifications – Current Status + Opportunities for Improvement
8. Proposal
9. Questions

# ESD Technology Roadmap – 2024*

- Both HBM and CDM fail levels of devices are decreasing, as pin speed increases, pkg area increases.
- 2.5 + 3D pkg interfaces are especially vulnerable as minimal to zero ESD design protection is possible.
- AEC ESD specs need overhaul to keep up with fast changing ESD roadmaps on high performance ICs.
- **Low voltage CDM testing has big variance issues; we will explore these today.**

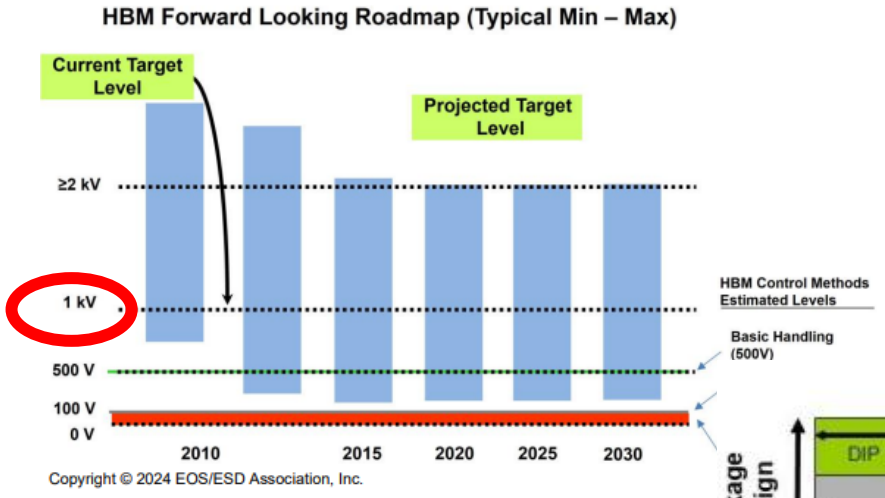



*Figure 1: 2010 to 2030 Human Body Model Sensitivity Limits Projec*
*NOTE: The current target level is 1 kilovolt.*


*Figure 4: 2010 to 2030 Charged Device Model Sensitivity Limits Projections*
*NOTE: The current target level is 250 Volts.*

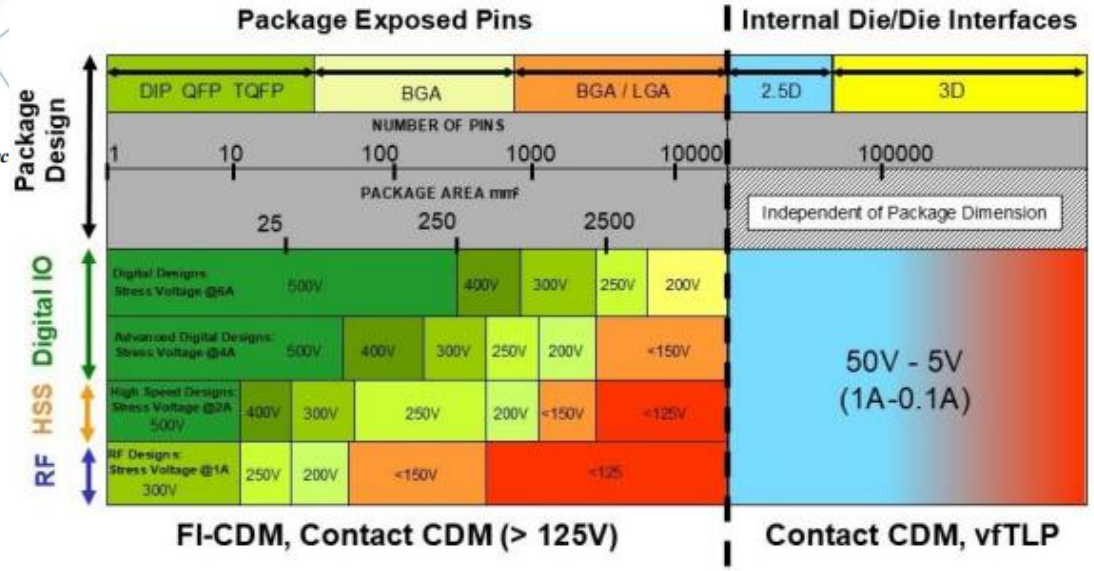



*Figure 2: Combined Projected Effects of IO Design and IC Package Size on CDM*

* Ref: ESD Technology Roadmap – 2024.

# HBM4 qual levels per JESD238A Spec. as an Example

## 7.4 Electrostatic Discharge Characteristics

**Table 88 — Electrostatic Discharge Characteristics**

| Parameter | Symbol | Values min. | Unit | Notes |
|---|---|---|---|---|
| PHY Human Body Model (HBM PHY) | $ESD_{HBM\_PHY}$ | - | V | 1 |
| PHY Charged Device Model (CDM PHY) | $ESD_{CDM\_PHY}$ | 30 | V | 2 |
| DA Human Body Model (HBM DA) | $ESD_{HBM\_DA}$ | 1000 | V | 3 |
| DA Charged Device Model (CDM DA) | $ESD_{CDM\_DA}$ | 250 | V | 4 |

NOTE 1 PHY Human Body Model (HBM PHY), or $ESD_{HBM\_PHY}$, is not applicable for HBM DRAM.
NOTE 2 Refer to JEP157A or later for more details.
NOTE 3 Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures.
NOTE 4 Refer to ESDA/JEDEC Joint Standard JS-002 for measurement procedures.

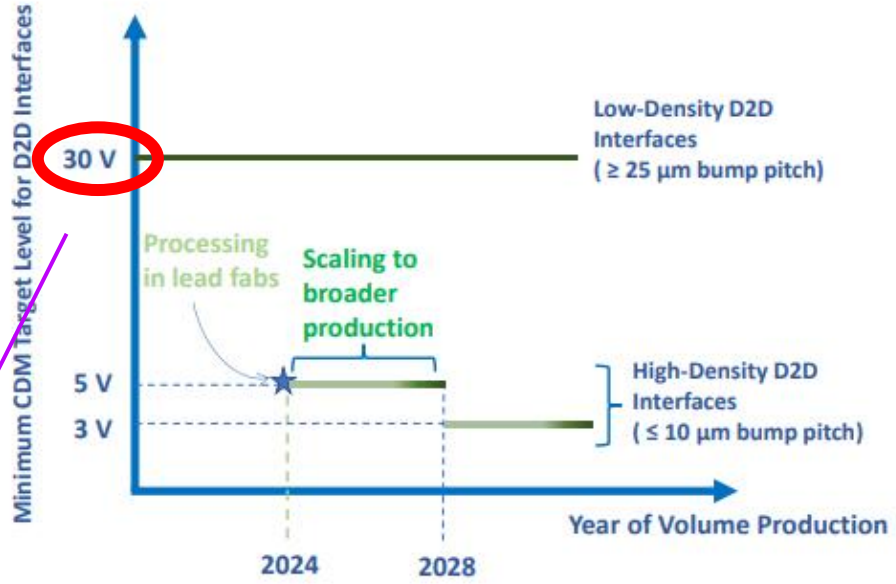



*Figure 12: Roadmap of CDM Targets of Die-to-Die Interfaces [27]*

Per JEDEC-238A, CDM PHY voltage = 30V (min) for newer node High Bandwidth Module vs 250V (min) per AEC Q100-011

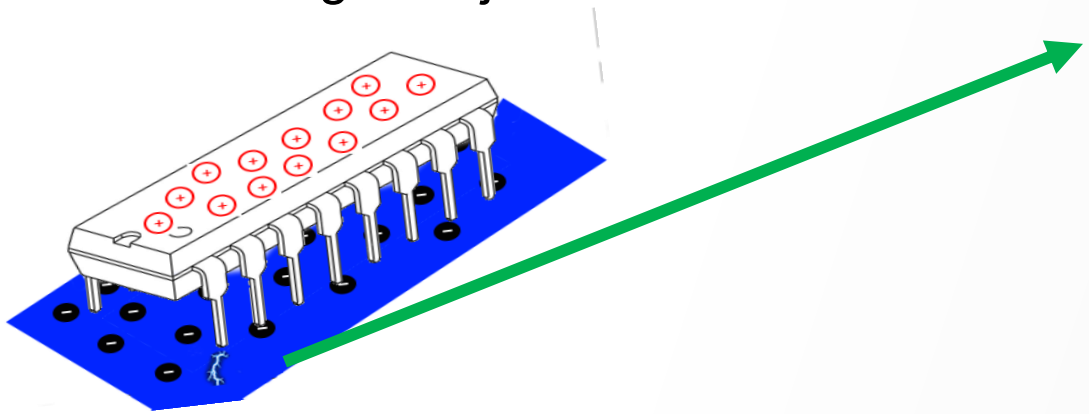
* Ref: ESD Technology Roadmap – 2024.

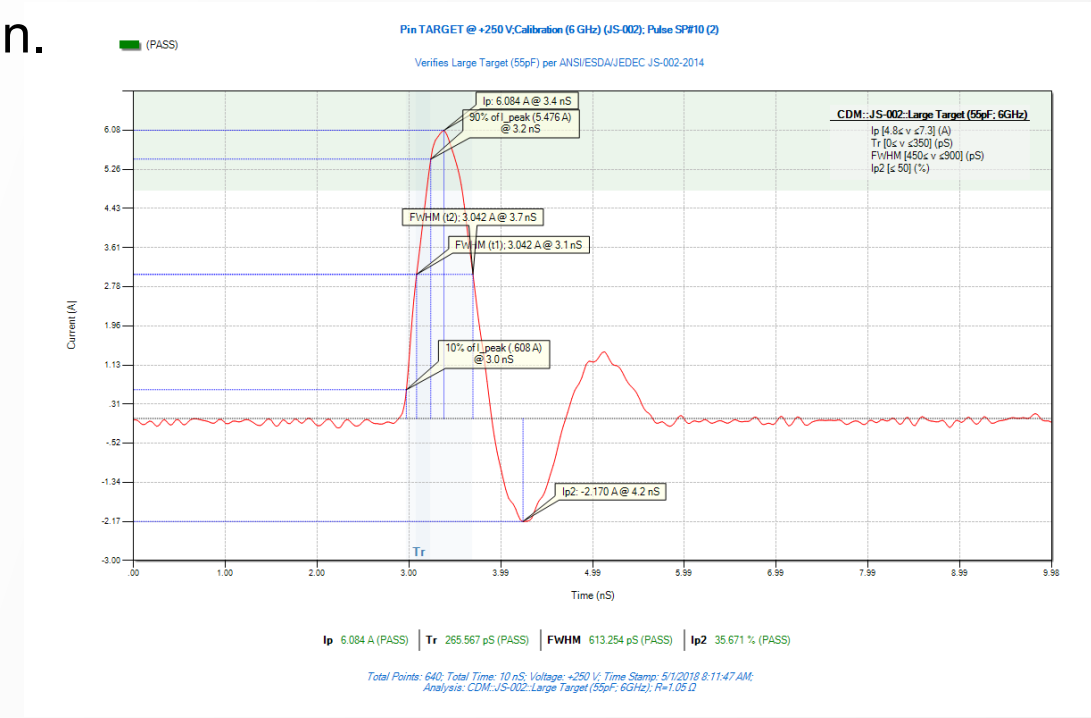
# Charge Device Model

The Charge Device Model (CDM) describes a stress on a semiconductor device that replicates a real-world event in which a semiconductor device acquires charge that can transfer to a conductive surface that has a different voltage potential.

A semiconductor device can acquire charge by different methods:

- Triboelectric charging, or production of charge by friction.
- Charge induced by electric fields.
- Charge induced by varying magnetic fields.
- By contact with a charged object

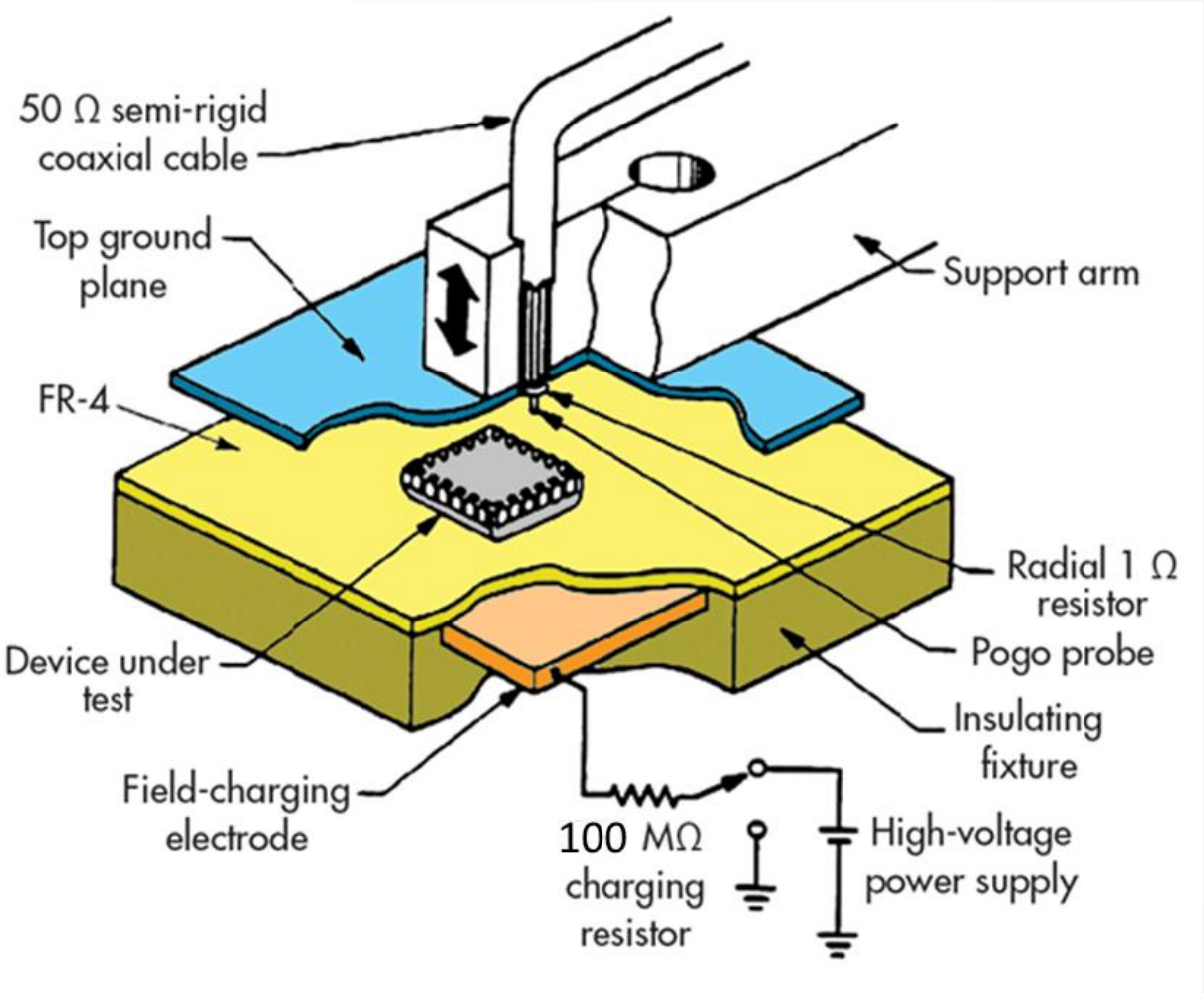





Ref: ThermoFisher Scientific. Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM). Marcos Hernandez. Presented at ESDINDIA forum, 2025.

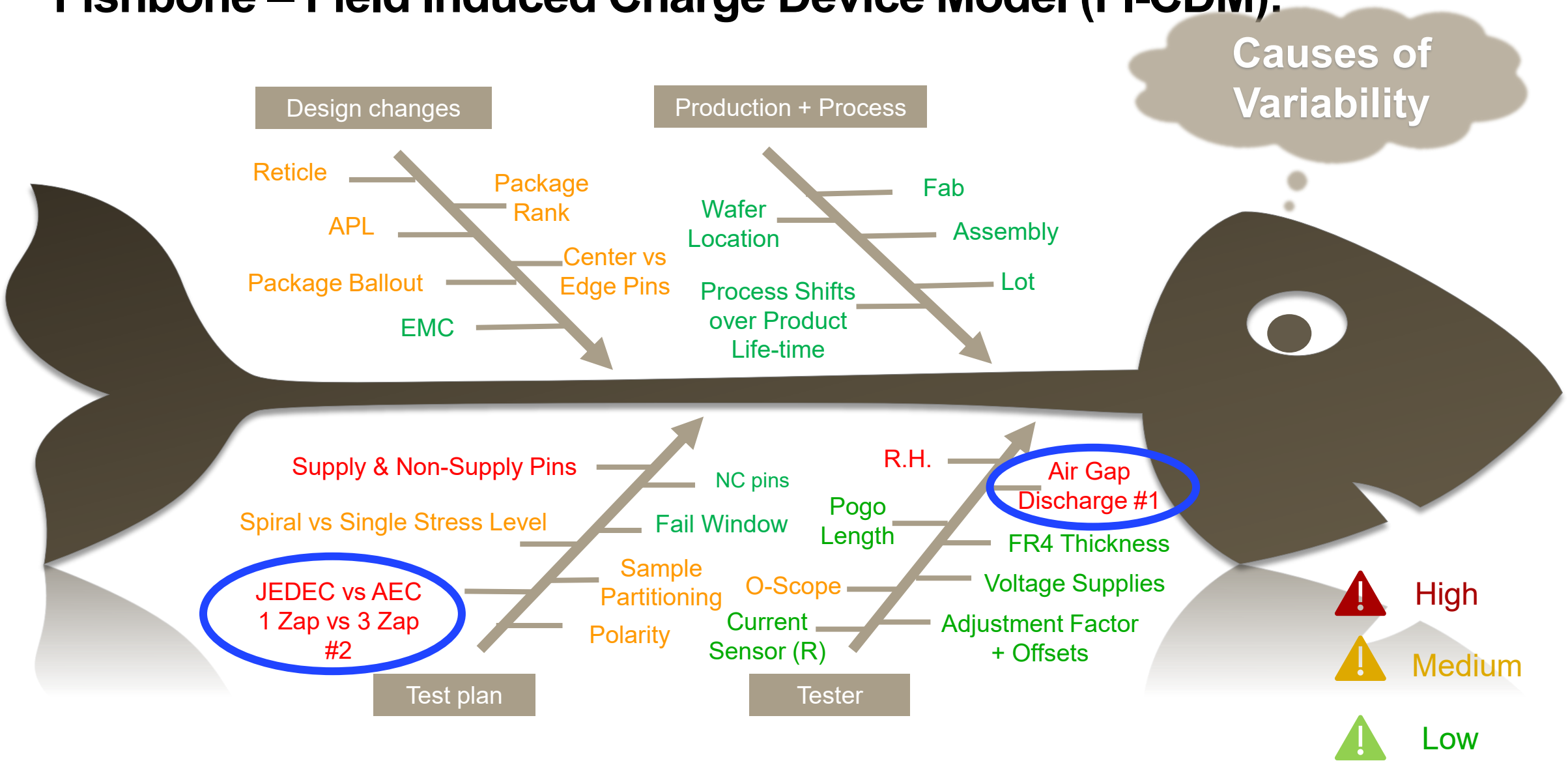
# Charge Device Model Simulator*

- The simulator applies an electric field between the Field-charging electrode and the top ground plane.
- The device sits “dead bug” with the pins or pads facing up
- Each pin is contacted by a pogo pin connected to the top ground plate through a radial resistor
- The radial resistor is then connected to a coaxial cable to capture waveform via oscilloscope
- **CDM is a one terminal test** (the device is capacitively coupled on the other end)
- Several organizations developed test standards for CDM
  - ESDA, JEDEC, AEC, JEITA
  - Harmonized into JS-002 (2015)


* Ref: ThermoFisher Scientific. Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM). Marcos Hernandez. Presented at ESDINDIA forum, 2025.

# Fishbone – Field Induced Charge Device Model (FI-CDM):




* R.H. and supply / non supply pins are N/A for this forum; focus on air gap and Zap

# Strategy for Variance: Control, Minimize, Sample

- **Tester Variance = Control**
  - Control with calibration (Adjustment factor + offset) to ensure WF's in spec range
  - FR4, Cal coins, current sensor, pogo length, voltage supplies.
  - R.H. controls. (CDA, N2 easily keeps R.H. < 5%)
  - Cleaning.
  - O-Scope (6 GHZ+)
  - **Air Discharge zap-zap variance gets worse with lower TC (lower voltage stress).**
    - **Consider Contact CDM Test Methods. (LI-CCDM, CC-TLP, RP-CDM, CCDM …)**


- **Test Plan Variance = Minimize**
  - Variance associated with 1st pin pulse, and pins stressed after non-connect pins can be mitigated (9)
  - Spiral / stair step stressing will often result in lower fail levels
  - Qual samples should only see one TC stress level to avoid risk of early failure due to wear-out.
  - Minimum step size for FI-CDM ~ 50V.
  - **3Zap testing should be avoided in favor of 1Zap testing**


- **Device Variance = Sample**
  - If risk is large enough, sample to ensure variation is within passing range.

    Ex: Package size. Reticle + APL design changes. Some process changes.
  - Pin group variance is unavoidable. VSS + Supply pins have higher Ipeak than signal pins.

# Variance # 1:  Air Discharge

- Review the Variance issue
- 4 Contact options
  - Standards in - progress
    - LI-CCD
    - CC-TLP

# Variance issue… WHY?

- Large Target (55pF) is ok to ~100V
- Small Target (6.6pF) is OK to 250V
- Most IC's pkg C_DUT is closer to ST
- 80% variance at 50V, ST
- Contact CDM does not have this issue

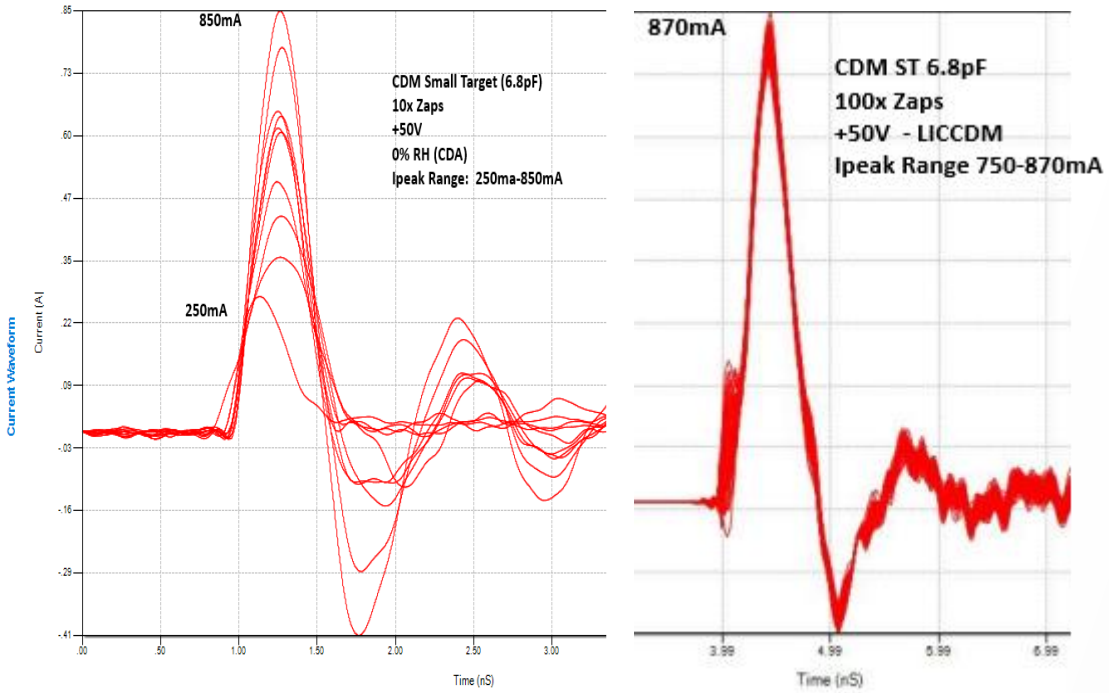



Fig 1: CDM (left ) and LICCDM (Right) Wave Form variance @ TC=50V, 8 GHz O-scope (Micron, ThermoFisher)

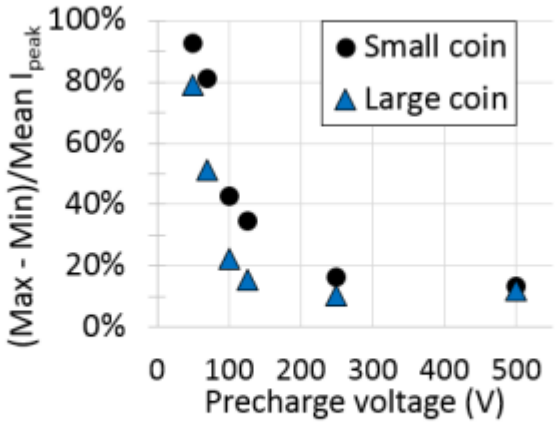



Figure 2: $I_{peak}$ maximum - minimum (top) and the standard deviation (bottom) of 50 zaps to JEDEC calibration coins as a percentage of the mean; 26% relative humidity. Data taken using an 8 GHz oscilloscope.

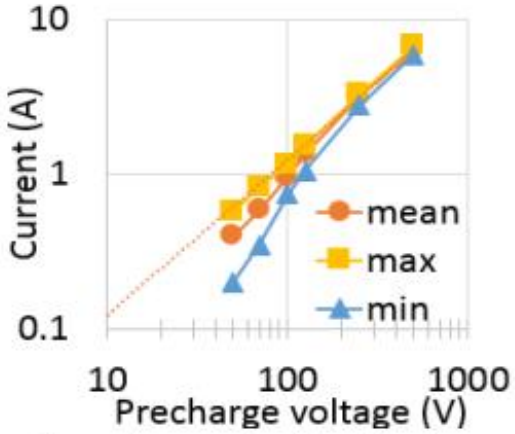
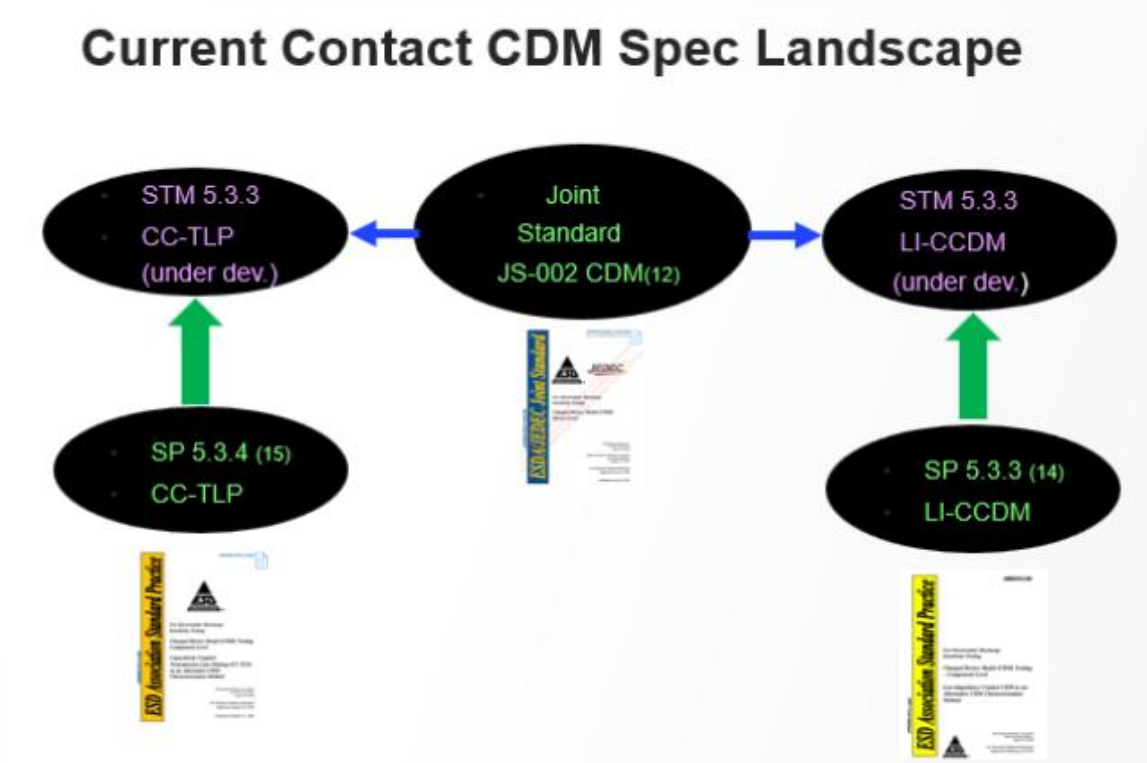



Figure 3: Maximum, minimum, and mean $I_{peak}$ as a function of precharge voltage when stressing the small JEDEC coin.

Ref: *Next Generation Charged Device Model ESD Testing*, Nathan Jack. 2016. www.ESDA.org, Fig 2, 3.

# Available options: CDM models for improved pulse repeatability @ low TC / V

- ❑ **CCDM***
  - ❑ Contact CDM (CDM2)
  - ❑ Peer reviewed papers + JS-002 Standards group work let to TR5.3.1-2018
- ❑ **RP-CDM***
  - ❑ Relay Pogo-CDM.
- ✓ **LI-CCDM**
  - ❑ Peer reviewed papers + JS-002 standards group work led to SP 5.3.3-2018
  - ❑ 2nd Round Robin Industry Testing starting 2026
  - ❑ Path: SP (Standard Practice) publishes to STM (Standard Test Method)
- ✓ **CC-TLP**
  - ❑ Peer reviewed papers + JS-002 standards group work led to SP 5.3.4-2022
  - ❑ 2nd Round Robin Industry Testing starting 2025 (**7 companies participating**)
  - ❑ Path: SP (Standard Practice) publishes to STM (Standard Test Method)

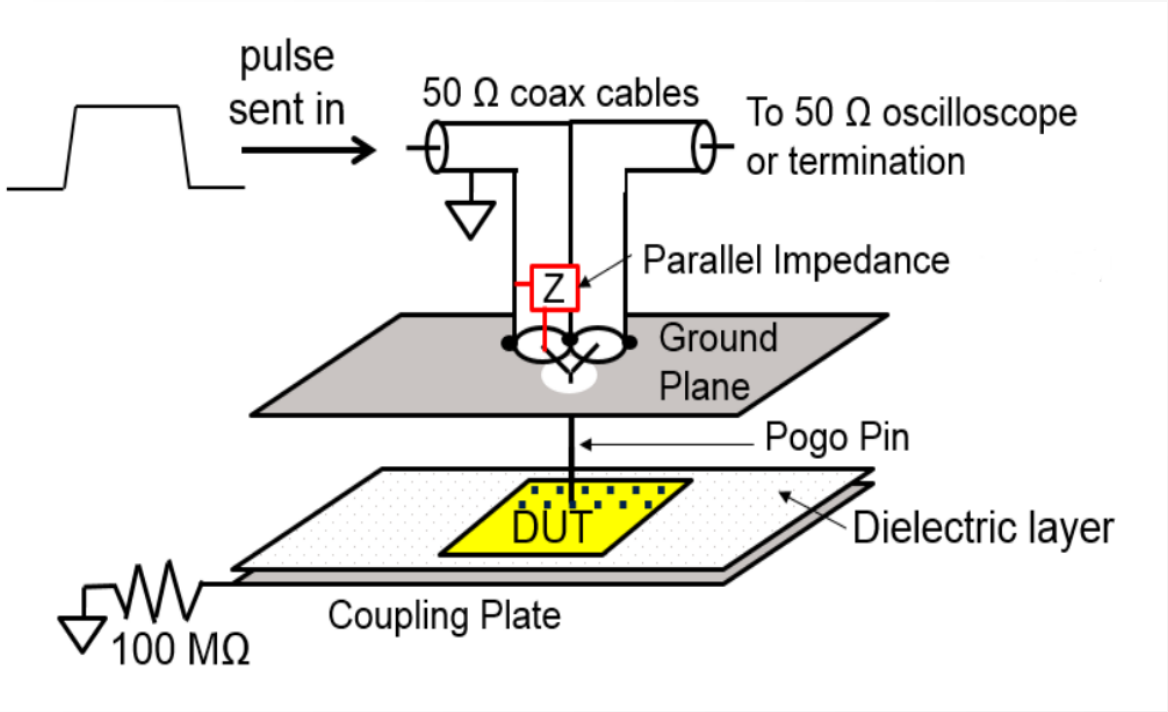



* CCDM and RP-CDM are outdated test techniques; Focus on LI-CCDM and CC-TLP that are industry accepted

Ref: www.ESDA.com

# Low Impedance Contact Charge Device Model (LI-CCDM)

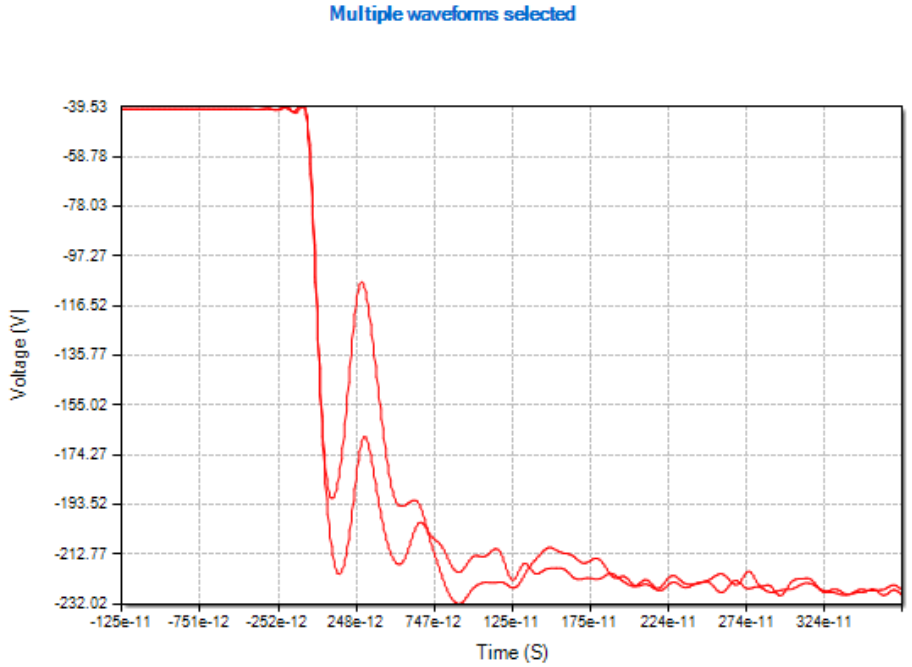
- Pogo contacts pin under test
- A modified TLP pulse is sent to the device through a 50Ω coaxial cable
- A second 50Ω coaxial cable also attached to the pin under test connects to an oscilloscope
- A third element, a 50Ω RF resistor is also attached to the pin under test
- All three parallel element resistance = 16.67 Ω
- This new test head and TLP pulser is added to JS-002 equipped tool



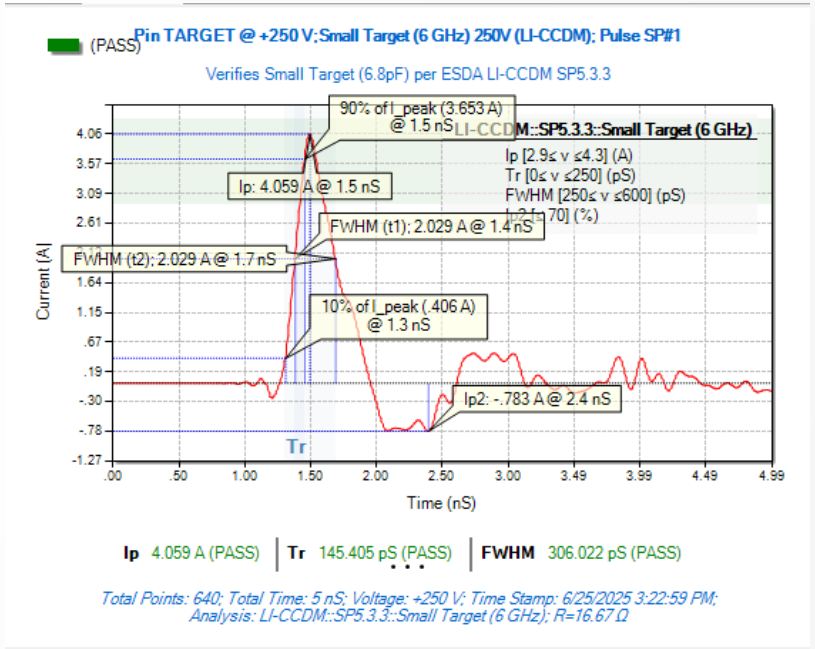

Ref: ThermoFisher Scientific. Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM). Marcos Hernandez. Presented at ESDINDIA forum, 2025

# Low Impedance Contact Charge Device Model (LI-CCDM)

- Stress pulse sent without touching the device (base waveform)
- The ground probe is moved and the pin under test (PUT) is contacted by pogo pin
- Second stress is sent while the PUT is in contact with the probe's pogo pin
- Difference between the base and the stress waveforms gives injected pin current
- No arcing – waveform very repeatable




**Base + Stress**

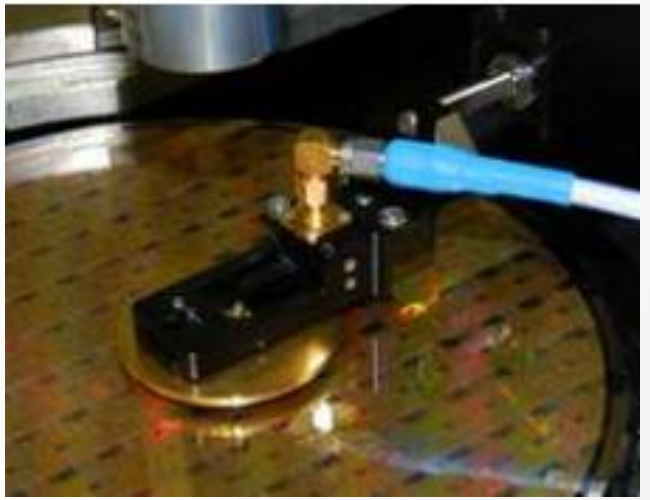


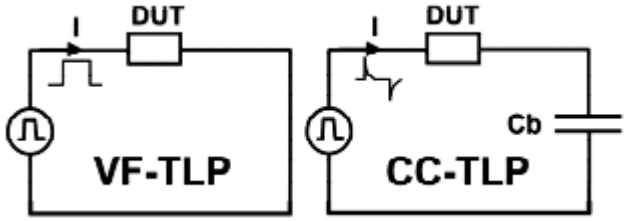

**LICCDM WF = Base - Stress**

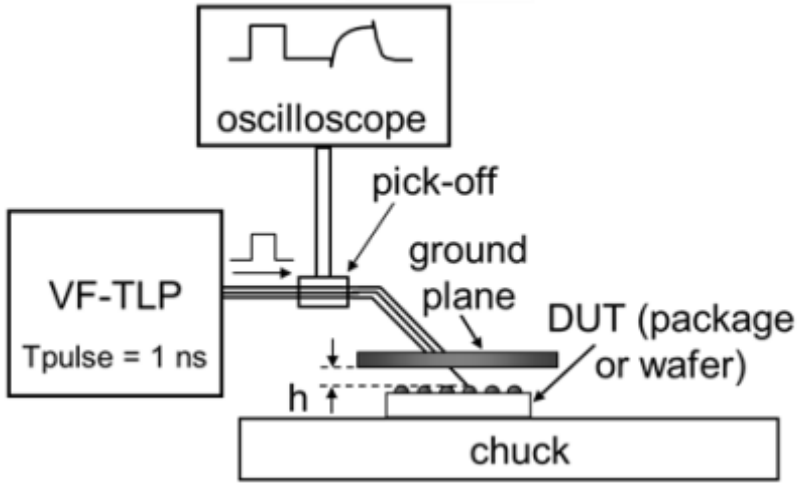
Ref: ThermoFisher Scientific. Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM). Marcos Hernandez. Presented at ESDINDIA forum, 2025

# Capacitively Coupled - Transmission Line Pulsing (CC-TLP)

- Evolved from VF-TLP, which is very widely used for ESD test structure characterization.
- Added a capacitively coupled ground path.
- Adjustable pulse width (1-5ns typical)
- Tunable rise time (~100ps typical)
- No air arcing – waveform very repeatable





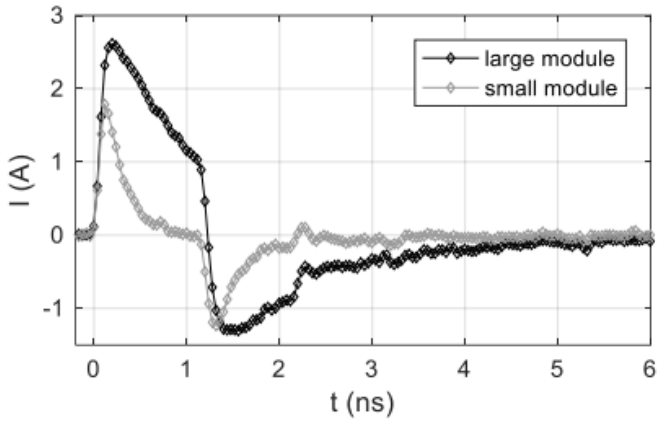




*Figure 8: Current Waveforms for the Small and Large CDM Verification Module*
*NOTE: The distance between the module and the GND disc of the CC-TLP probe is 0.3 mm.*


Ref 1: Using CC-TLP to get a CDM Robustness value. Kai Esmark, Reinhold Gaertner, Stefan Seidl, Friedrich zur Nieden, Heinrich Wolf, Horst Gieser
Ref 2: Capacitively Coupled Transmission Line Pulsing CC-TLP – A Traceable and Reproducible Stress Method in the CDM-Domain. Heinrich Wolf, et al. 2003.

# Variance # 2:  3Zap vs 1Zap

- Revisit AEC 2024 Rel Workshop presentation key slides
- NXP 2024 paper
- Conclusion

# Prior Work – Presented 2024 AEC Workshop – Detroit

## Harmonization to / Justification for a Common Industry / Automotive CDM Stress Procedure of Single Zap Per Pin Per Polarity


Nobuyuki Wakai (Toshiba Electronic Devices and Storage)
Teruo Suzuki (Socionext)
Masanori Sawada (Hanwa electronics)
Greg O'Sullivan (Micron)
Brett Carn (Intel)
Theo Smedes (NXP)
Alan Righter (*Analog Devices**)

**former affiliation*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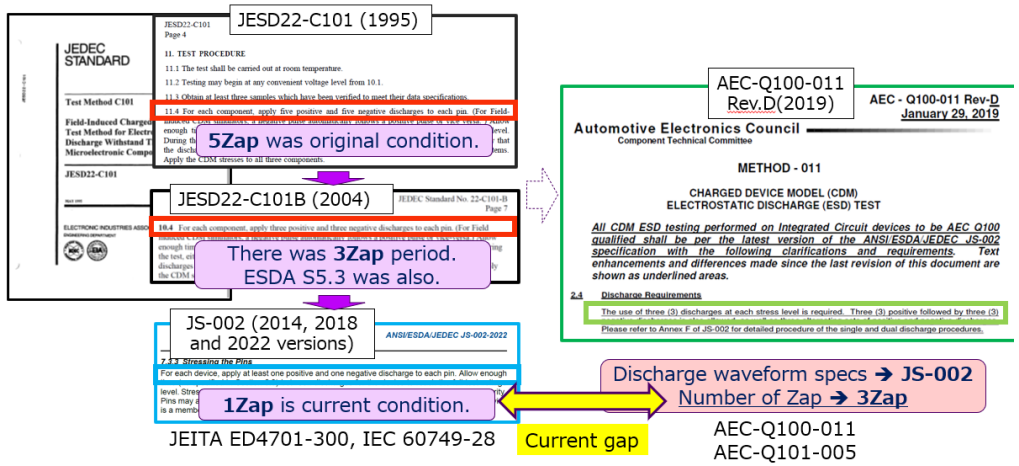
## 1. Motivation [1]~[6]

a recognition for contents difference in each CDM test standard

| | AEC-Q100*, Q104, Q101 | | Other standards |
|---|---|---|---|
| Target voltage | 250V* (<28nm)<br>500V** (current rev.)<br>250V** (In-progress rev.) | ⇔ | Classification (JEDEC / IEC)<br>250V (ESD council)<br>500V (JEITA) |
| Zap times | **3Zap** (both polarities) | ⇔ | **1Zap** (both polarities) |

**This matter is today's discussion with referring to**
**-relevant test standard**
**-ESD control and probability**
**-actual comparison data**

## 2. A brief history of CDM test developments [1]~[4],[8]~[11]




## 3. Reality and possibility [4]

Waveform observed by 8GHz (JS002)

8 GHz TC 500, Small Verification Module (oscilloscope adjusts for attenuation)

**Past understanding**

- Discharge waveform variation was also one of topics of reproducibility as standard test.

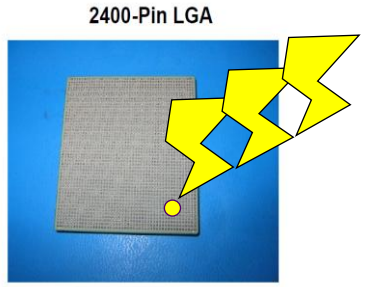
3Zap or 5Zap was solution to make it higher.

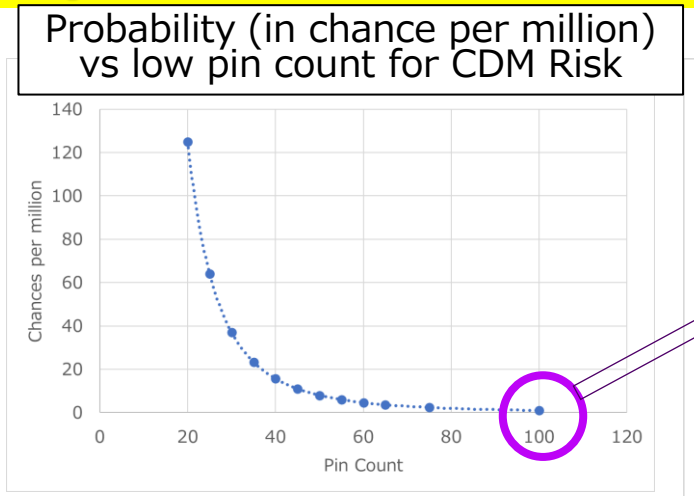
**Present understanding**

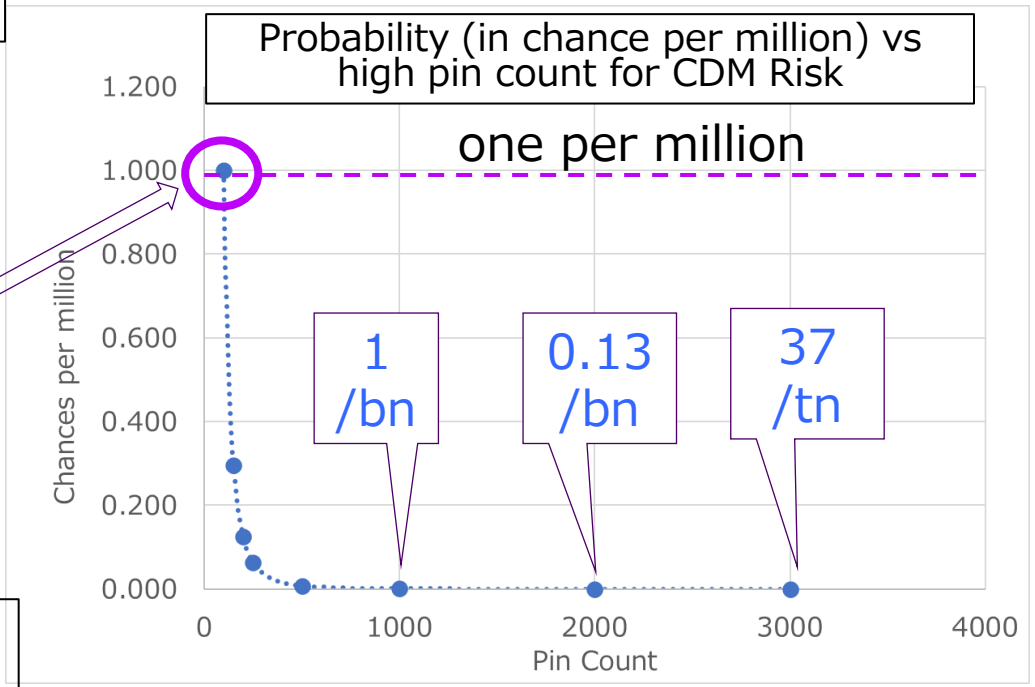
- 1st peak of CDM discharge waveform is highly related CDM breakdown.
  (Rise time and Peak current of 1st peak.)
- Variation of 1st peak is acceptable in the point of test reproducibility.
- Discharge waveform observation technology has improved to catch realistic CDM phenomenon.
  1GHz ➔ 6GHz ➔ 6GHz or more

## Prior Work – Presented 2024 AEC Workshop – Detroit (cont…)

# Q:How much is the probability of 3 consecutive discharge (3Zap) to the same 1-pin ?



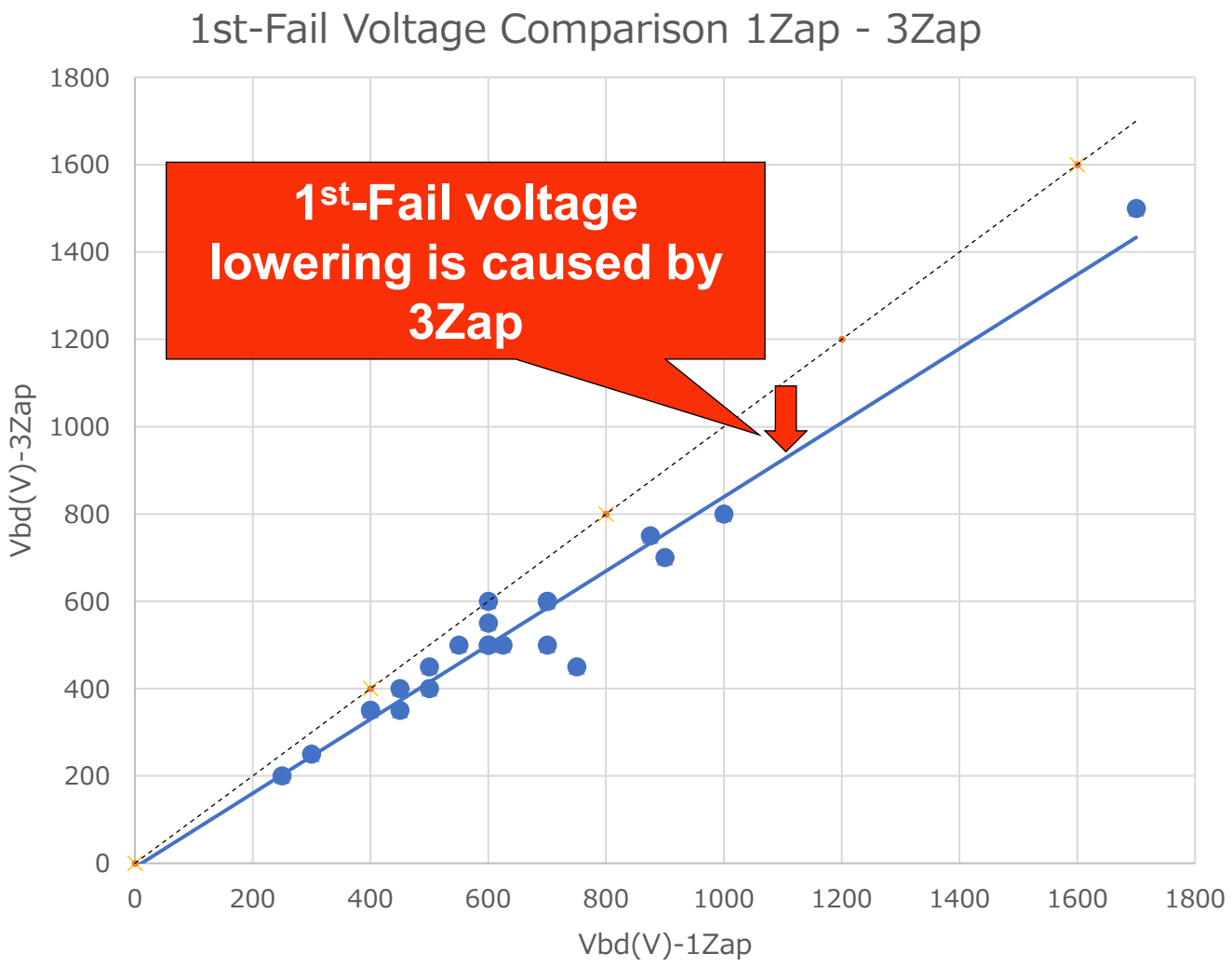

Probability that the same pin can be zapped 3 times in a manufacturing environment assuming a random event

A: CDM tester ➔ Possible

**Real World ➔ Impossible(almost)**

**In automotive environment, even 1 ZAP should be prevented**

# Prior Work – Presented 2024 AEC Workshop – Detroit (cont…)




23 products data from 7* companies

**50 ~ 300V lowering is observed by increasing from 1Zap to 3Zap**

* Micron, NXP, Toshiba, Socionext, Hanwa Electronics, Analog Devices, Intel

# A Statistical Explanation of CDM Qualification Variability*

**Theo Smedes** (1), Wolfgang Scheucher (2), Sheela Verwoerd (1), Joop Verwijst (1)NXP. EOS/ESD.2024

**Paper investigates the various contributors to FI-CDM qualification fail variance**

- •1 Pulse / 3 Pulse
- • Pulse to Pulse
- • Wear-out (Gate Oxide)
- • DUT to DUT

Samples ran, and Monte Carlo modeling used for generating higher samples to investigate variation.

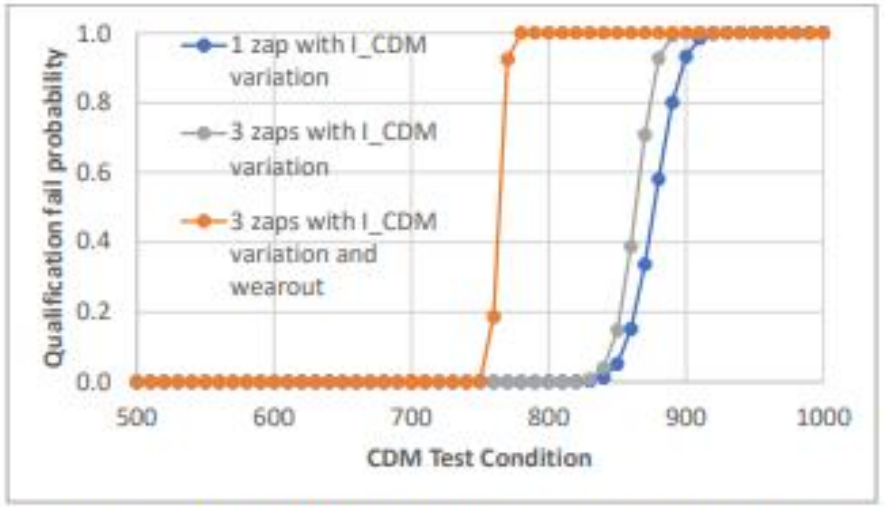



Figure 11: Qualification fail probability as function of the CDM stress level for a 0/3 qualification requirement.

**Key Takeaway**:

*"Since repeated stress close to the fail level is very unlikely in an EPA (ESD Protected Area) the 15-20% fail level degradation caused by gate oxide **wear-out** is too pessimistic. This failure mode is not relevant in an EPA . Therefore, it is recommended to eliminate the use of multiple pulses from all CDM qualification methods." :- Theo Smedes et al..)*

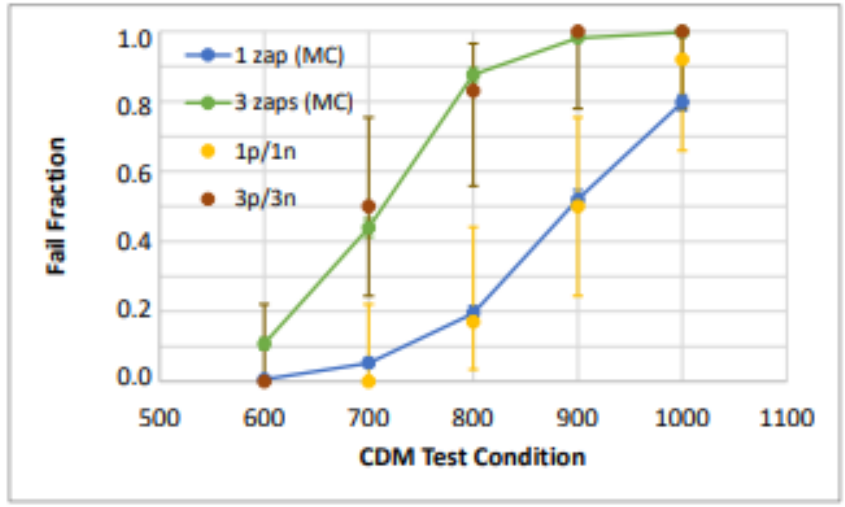



Figure 14: Fail fraction for MC run with 1000 samples per level compared to product results with 12 samples per level. Error bars indicate the 90% confidence interval for observations and MC.

*Ref: Theo Smedes, Wolfgang Scheucher, Sheela Verwoerd, Joop Verwijst, "A Statistical Explanation of CDM Qualification Variability", *2024 46th Annual EOS/ESD Symposium (EOS/ESD)*, vol.46, pp.1-10, 2024.

# Review: AEC ESD Specifications – Status + Opportunities for Improvement

- AEC Q100-rev J / 2023 Base Doc – Integrated Circuits
  - HBM + CDM + Qual targets updated to align with ESD Technology Roadmap.
- AEC Q104-rev A / 2025??? Base Doc – Multichip Modules (**Passed vote, pending publication**)
  - HBM + CDM + Qual targets updated to align with ESD Technology Roadmap.
- AEC Q100-011 Rev D / 2019 **CDM** - IC Semiconductors
  - Rev D aligned to JS-002 method, with various exceptions / additions detailed (Corner balls, 3 zaps, …)
  - Contact CDM test method accommodation roadmap for <200V T.C. sensitive devices.
  - 1 Zap vs 3 Zap harmonization.
  - Opportunities to further align, simplify, and adapt to keep up with ESD roadmap, including align on report format improvements (JEP178).
- AEC Q101-005 Rev A / 2019 **CDM** - Discrete Semiconductors
  - Rev A is aligned to JS-002 method various exceptions / additions detailed.
  - Opportunities to further align, simplify exist as some exceptions / additions are now covered in latest JS-002 revision.
- AEC Q100-002-rev E / 2013 **HBM** - IC Semiconductors
  - Rev E aligned to JS-001 test method, with various exceptions / additions detailed.
  - JS-001 has had the following revisions: 2014, 2017, 2022, 2023, 2024 after rev E.
  - Opportunities to further align, simplify, and adapt to keep up with ESD roadmap, including align on report format improvements (JEP178).
- AEC Q101-001 Rev A / 2005 **HBM** - Discrete Semiconductors
  - Rev A is aligned to obsoleted test specs STM5.1 / JESD22-A114


- AEC Q200-002 Rev B / 2010 **HBM per IEC 61000-4-2** : Passive Components
  - Rev B is aligned with IEC 61000-4-2, Ed 2: 2008.
  - Latest edition is Ed 3.0: 2024, and includes changes to calibration requirements, adding second peak current Ip2, and other improvements.

# Proposal – Let's Review and Update AEC ESD Specs

Goals:

- Maintain overall quality and relevance of the ESD sub-standards.
- Benefit from industry research and collaboration.

- Open the following working groups to review, align, optimize, and update as appropriate:
  - Q100-011 (CDM IC)
  - Q101-001 (CDM Discrete)
  - Q100-002 (HBM IC)
  - Q101-005 (HBM Discrete)
  - Q200-002 (HBM ESD Gun – Passives)
- AEC volunteers with ESD testing experience are willing to help initiate and lead this effort, including:
  - Greg OSullivan, Sumit Tayal Micron Technology – interested in CDM Specs.
  - Scott Ward, Texas Instruments, previous 2019 Q100-011D and Q101-005A sub-committee co-chair. Interested in HBM + CDM Specs.
  - Theo Smedes, NXP Interested in HBM + CDM Specs.

# Next steps:

- **Let's start!**
- **Request(s) to AEC committee members to open the ESD sub-spec working groups. Priority, CDM -> HBM -> ESD Gun.**

# QUESTIONS?