

功能安全暨資通安全服務中心

Functional Safety and Cybersecurity Service Center

Advancing Zero-Defect Through Process-Oriented Reliability and Soft Error Risk Integration

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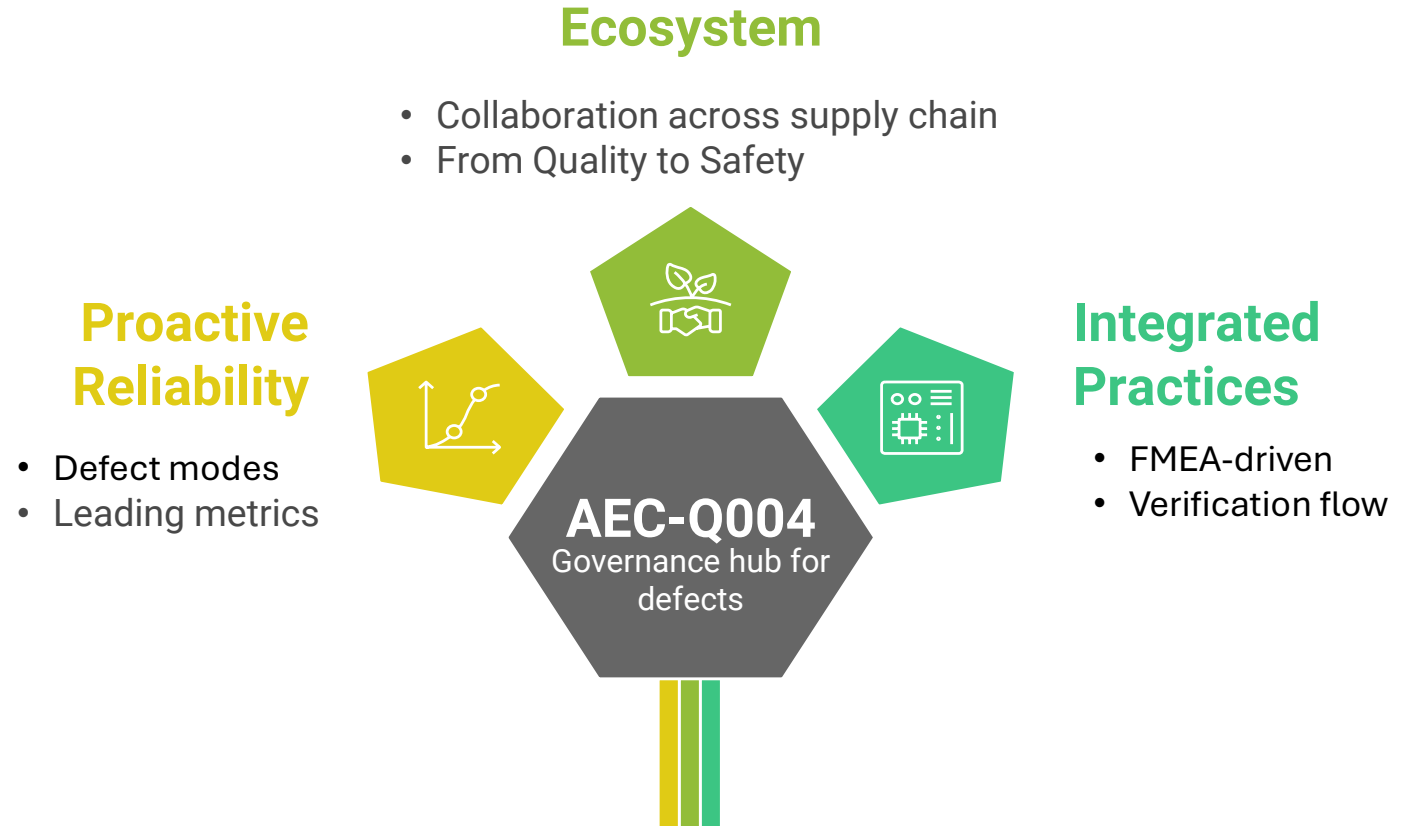
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OUTLINE

- **Introduction & Objective**
- **Frameworks and Standards Landscape**
- **Proactive Reliability through FMEA**
- **Expanding Reliability Scope: Soft Error Risk (SER)**
- **Building a Zero-Defect Ecosystem**

AEC-Q004 Drives Zero Defect

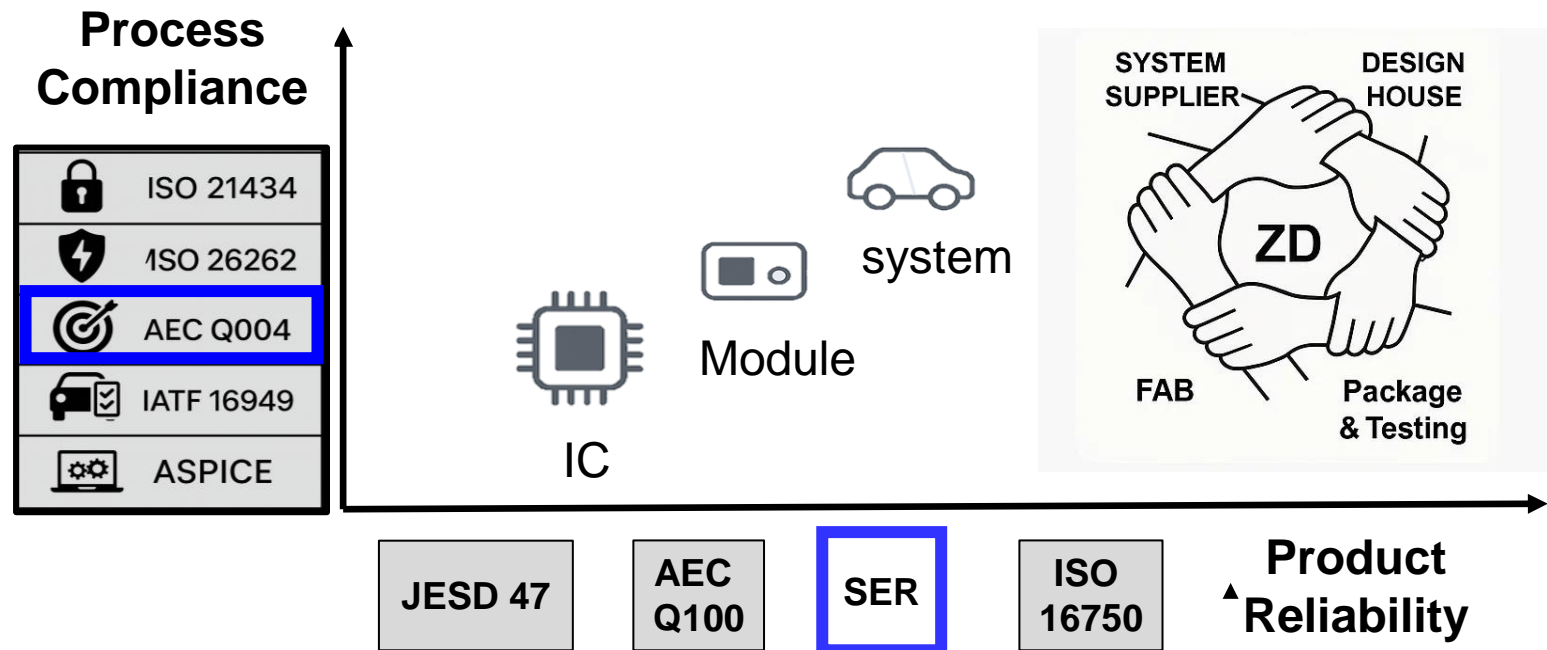
- Zero Defect Approach:
 - Any condition (hard/soft) that threatens zero-defect assurance in automotive electronics
- Supply Chain Collaboration:
 - Integrated with safety and reliability frameworks



Frameworks and Standards Landscape

Automotive electronics: increasing complexity & safety-critical role

- AEC-Q004 Zero Defect framework
- Position: **Zero Defect = governance hub**

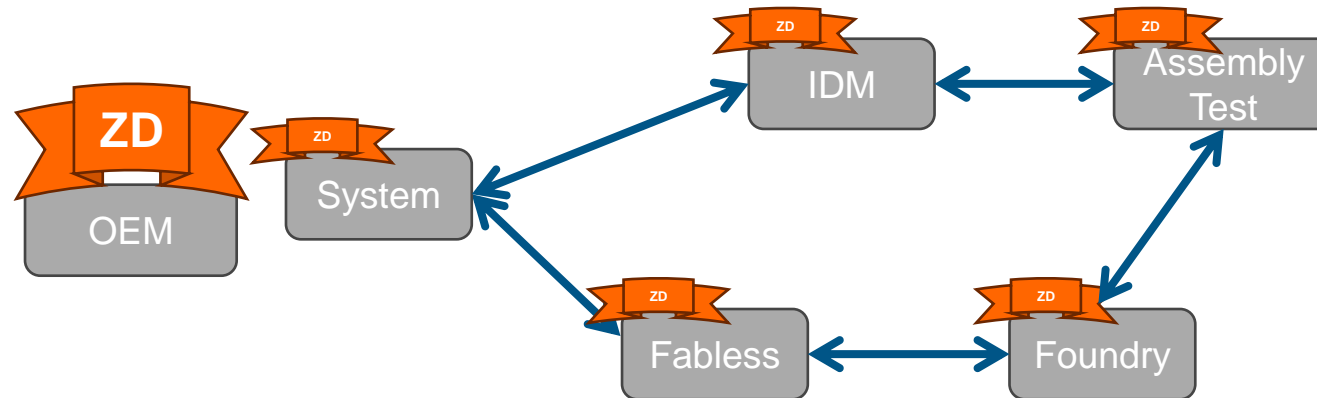


1. ASPICE: **A**utomotive **S**oftware **P**rocess **I**mprovement and **C**apability **D**etermination
2. **SER**: **S**oft **E**rror **R**isk

Collaboration Across the Value Chain

- Both upstream and downstream partners should collaborate to achieve Zero Defect across the supply chain
- In response to quality requirements, the upstream partners request ZD compliance, and the downstream partners deliver ZD-compliant parts

- AEC –Q004 Compliance
- Zero defect delivered across ecosystem

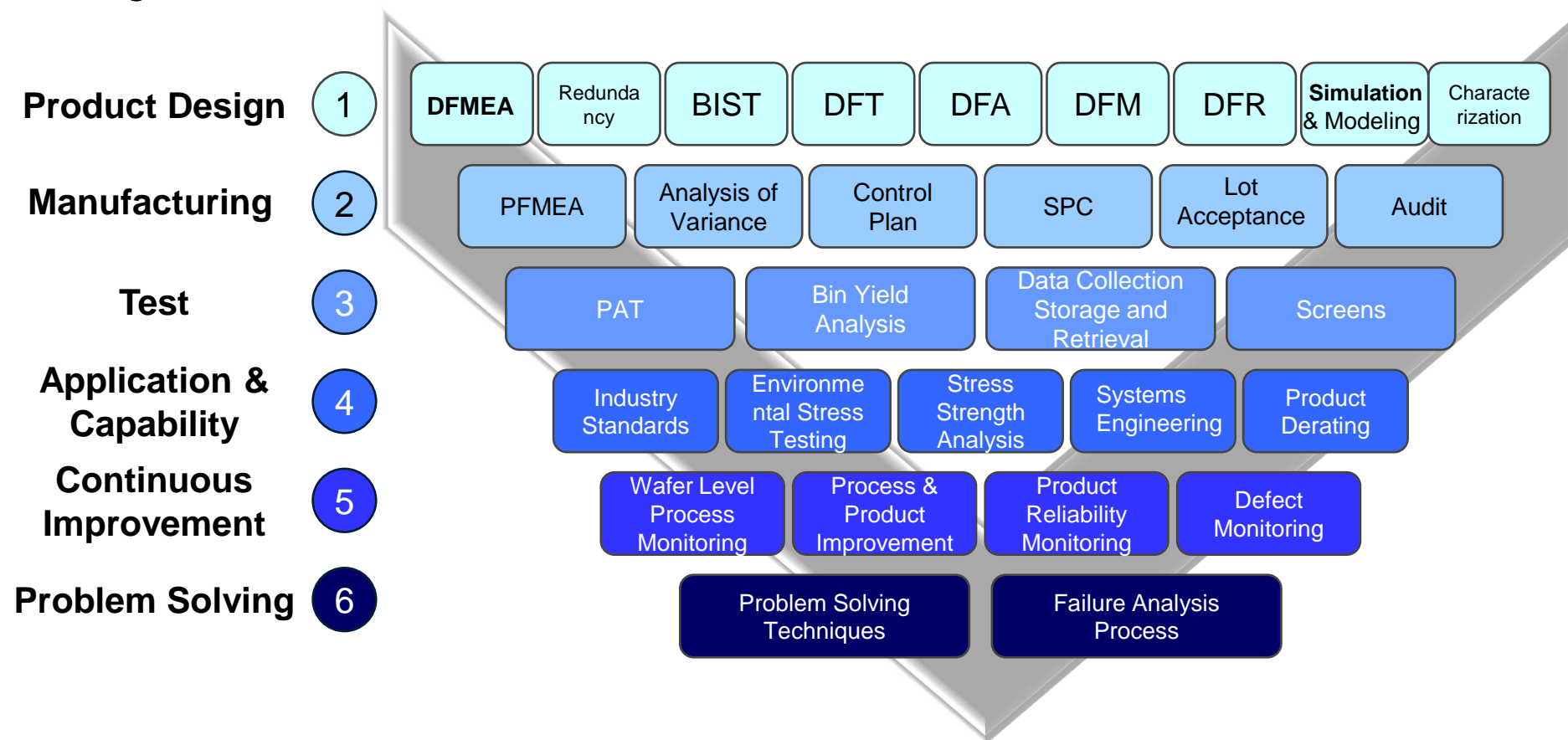


Objective

- Unified Zero-Defect Strategy
- Transparency and OEM Confidence
- Addressing Emerging Reliability Threats
- Process-Oriented Assurance Across the Value Chain

Zero Defect Framework

- The framework shows how applying these methods can enhance Zero-Defect (ZD) performance
- Leveraging systematic tools improves quality and reliability across design, manufacturing, and management



Building Value Through Connection

Connectivity

Reliability

Skill

- Each jewel demands state-of-the-art standards — connectivity, reliability, and skill woven into every strand.
- The Zero-Defect Dilemma in the Semiconductor Industry
 - A Single Company Cannot Achieve True Zero-Defect Alone
 - Checklist Expansion Creates a Resource Trap
 - Why the Ecosystem Fails Without Coordination
 - What's Needed for a Real Zero-Defect Ecosystem

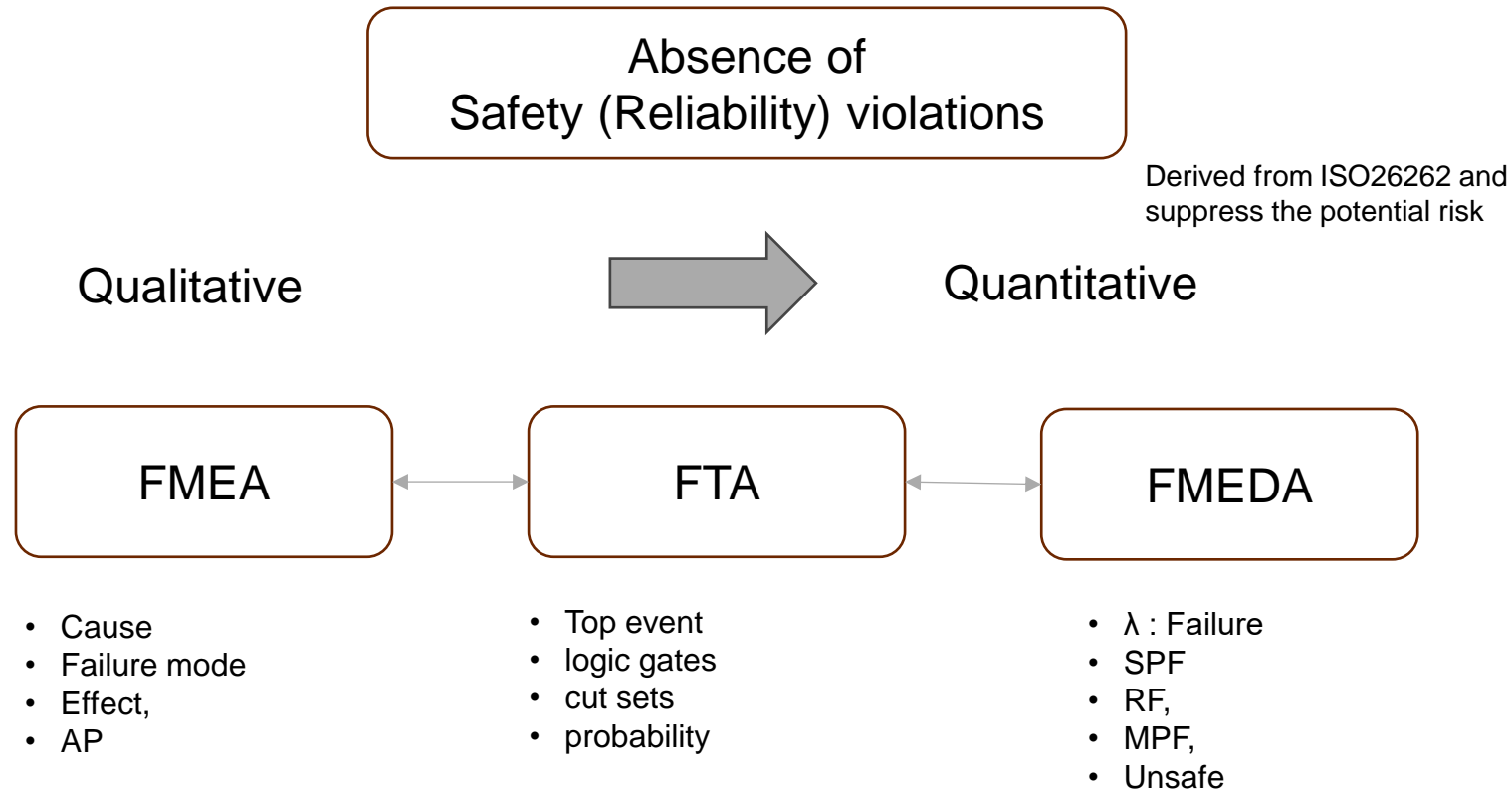


Reference

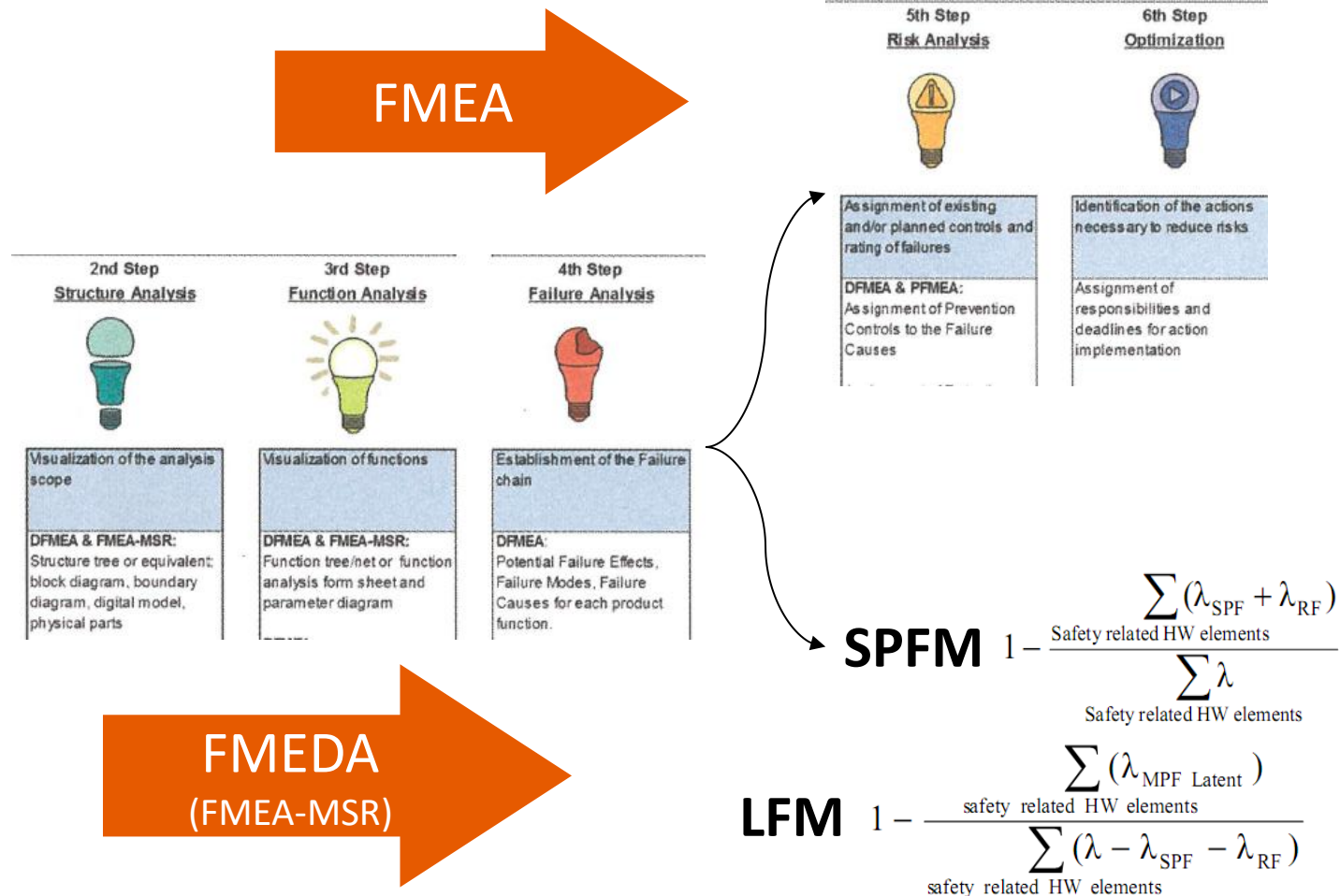
- Powell, Magnanini, Colledani, Myklebust, *Advancing Zero Defect Manufacturing*, 2022
- Psarommatis, May, Dreyfus, Kiritsis, *Zero-Defect Manufacturing & Sustainability*, 2020
- Kennedy & Alexandrescu, *Automotive Electronics Reliability In-Field Monitoring*, 2024
- AEC Council, *AEC-Q004 Standard*, 2020
- Gandhi & Gandhi, *Advanced Analytics for Yield Improvement*, 2015

From Failure Analysis to Leading Metrics for Manage Risk

- Systematic analysis: Use FMEA, FTA, and FMEDA to identify
- Quantitative linkage: provide the failure rate (λ) as a leading metric
- Design insight: the logical connection from item/system faults down to individual failures



FMEA vs. FMEDA



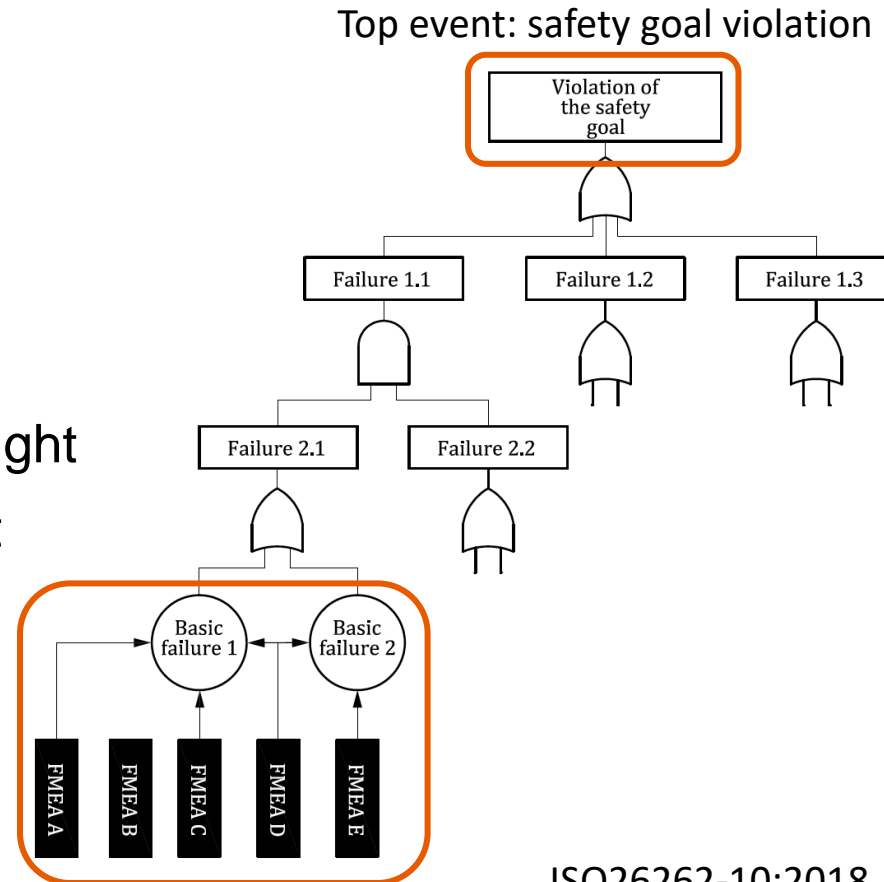
Make sure systematic fault is sufficiently low by preventive and detective control measures

Make sure random hardware fault could be controlled by safety mechanisms

Insight Through Skill: Combining FTA and FMEA

- FTA
 - Top-down logic to trace risks
- FMEA
 - Bottom-up discipline to capture weaknesses.
- Together
 - Reflect engineering skill and insight
 - Connecting system faults to root causes

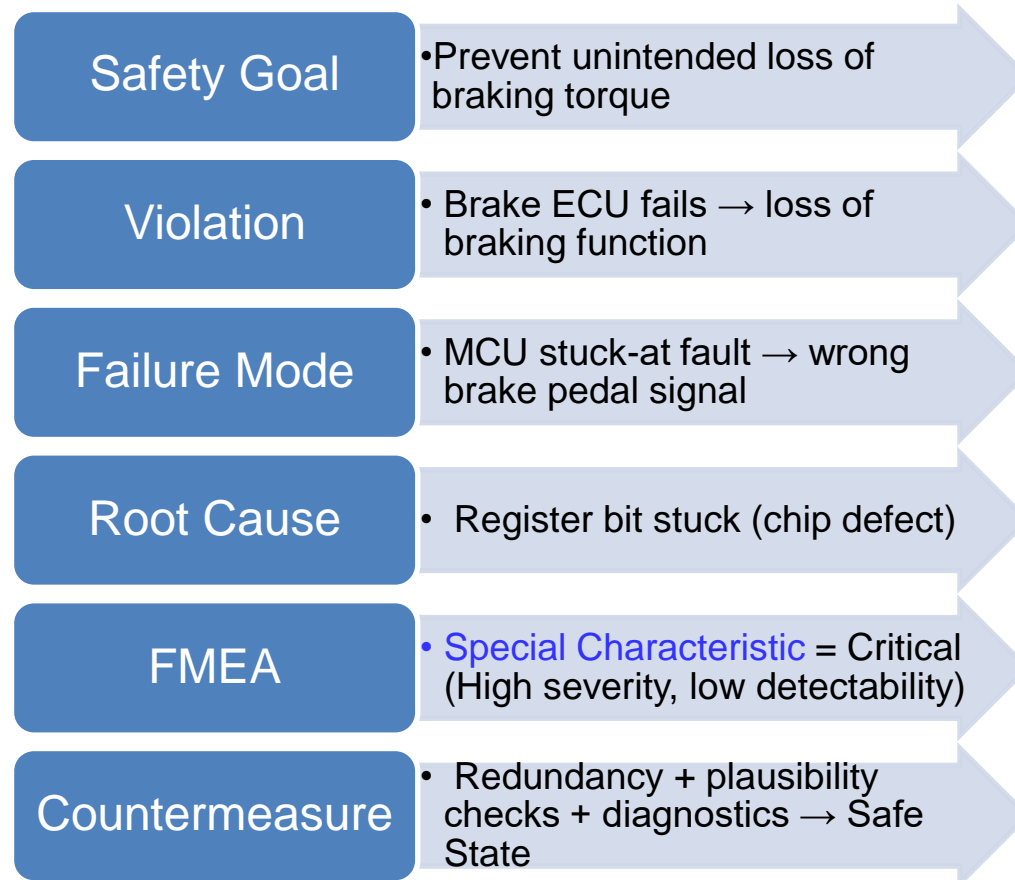
Bottom event: failure of elements



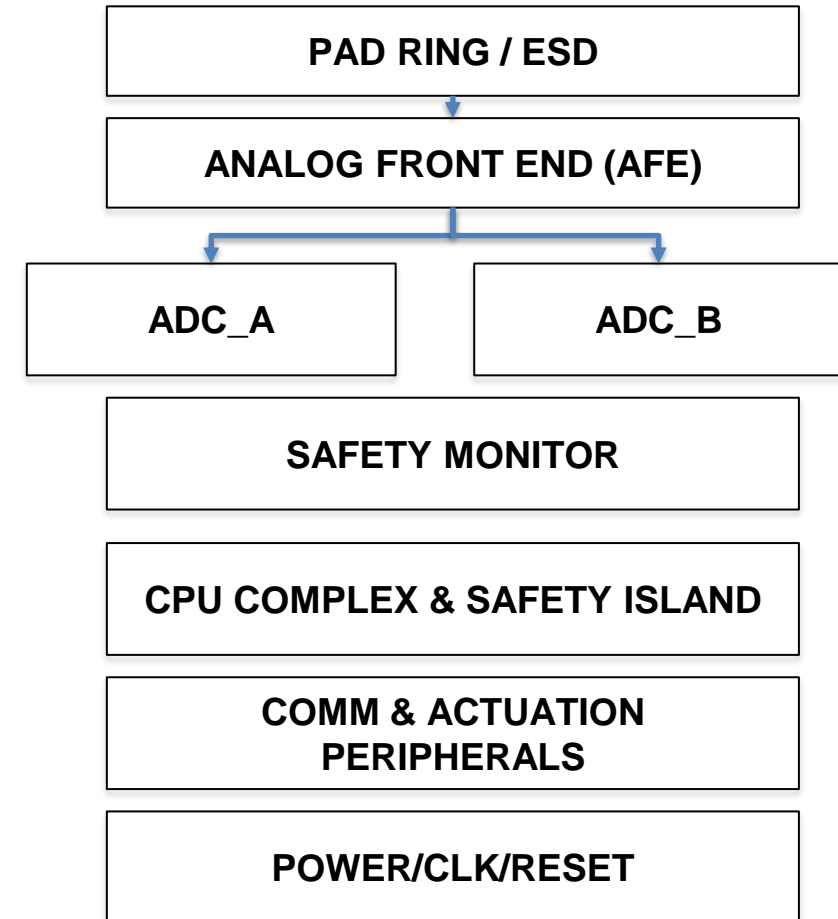
ISO26262-10:2018 Annex A

Visible Failures Anchored in FMEA

■ Automotive ECU Example, Brake-by-Wire System

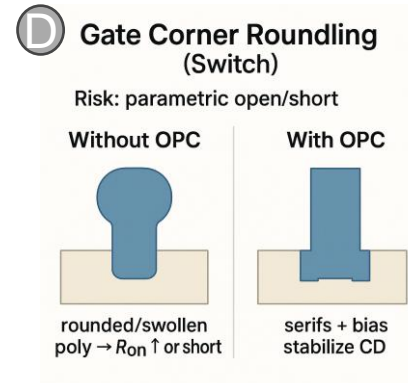
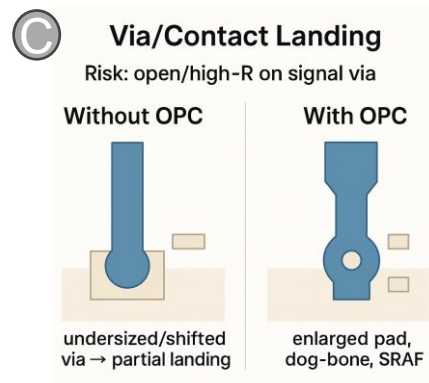
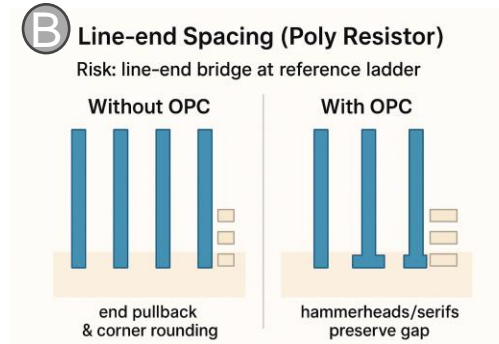
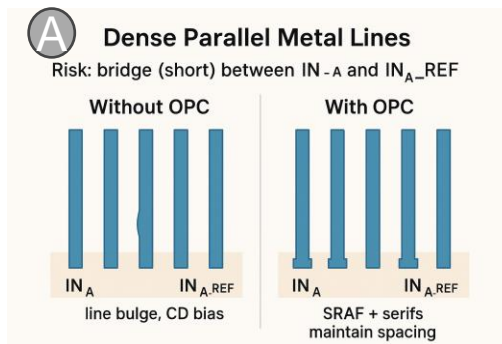


• MCU Block Diagram



OPC-Driven Risk Mitigation for Reliability

- Applying OPC reduces critical manufacturing risks—such as shorts, opens, and signal distortions—ensuring that the circuit, marked as a Special Characteristic, remains reliable.
- Linking risks to FMEA ensures proactive quality control, with checks built into the process to safeguard product integrity and yield



FMEA Linkage with Special Characteristic

A: Input nets integrity (Metal spacing)
OPC/LFD check

B: Reference ladder accuracy (Poly ends)
End-gap OPC check

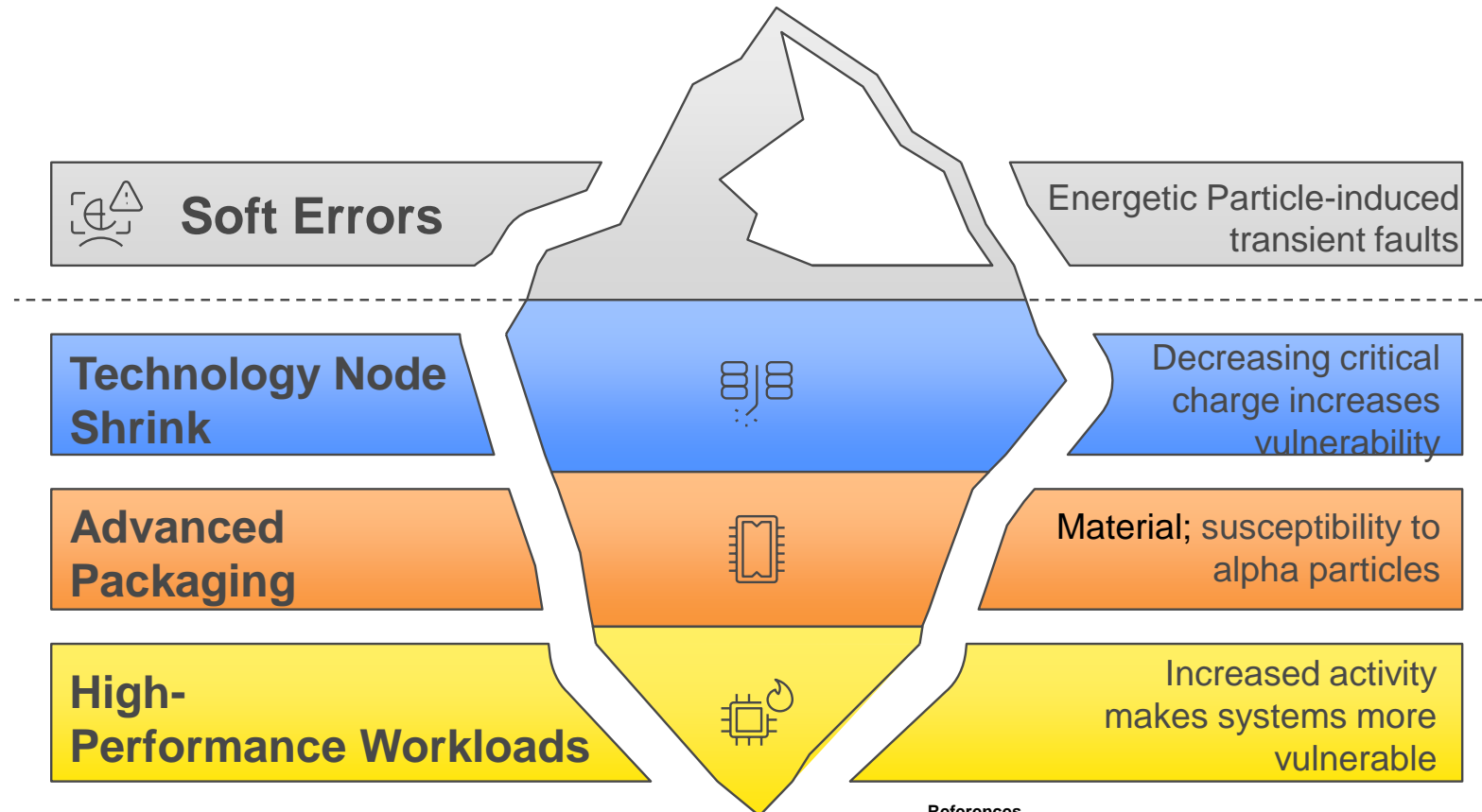
C: Signal continuity (Via stack)
Redundant via, OPC bias

D: Switch linearity (Poly gate)
Gate CD OPC sign-off

OPC : Optical Proximity Correction
LFD : Lithography Friendly Design
SRAF : Sub-Resolution Assist Feature
Serifs : Tiny layout extensions at corners

Soft Errors: A Hidden Threat to System Reliability

- Node shrink, packaging, and workloads drive hidden soft-error risks
- Zero defect needs proactive SER modeling and mitigation

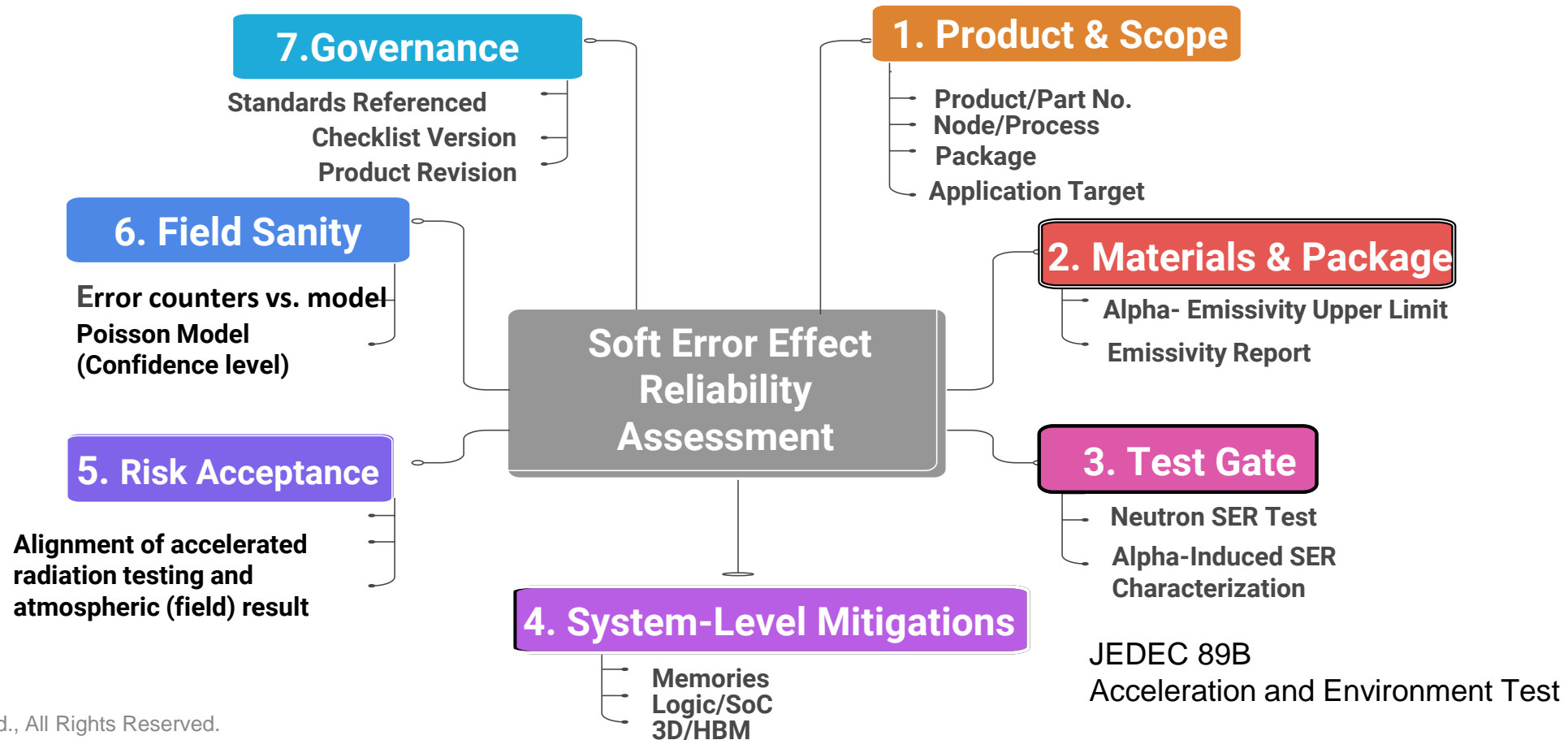


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- Slayman, Soft Error Trends & Mitigation in Memory Devices, IRPS, 2015
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- MacDermid Alpha, Mitigating Soft Errors in Advanced Packaging, 2025.
- 3D InCites, New Ultra-Low Alpha Tin Plating Solutions for Reliability, 2025

Semiconductor Reliability Assessment Process

- SER assessment connects design, package, test, and system
- Zero defect needs proof at every gate



Failure Classification and Management Strategies

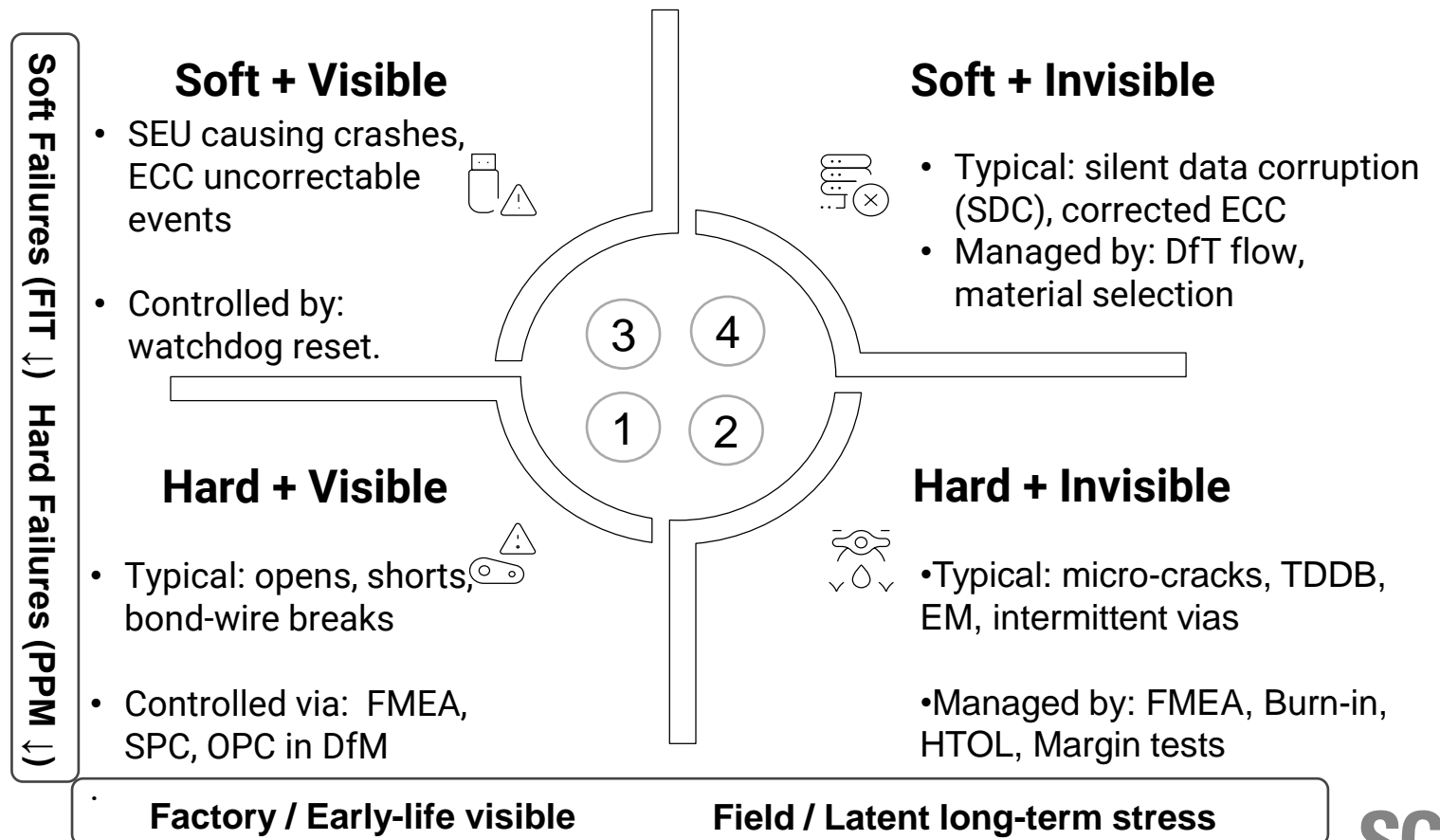
- Hard and soft failures demand dual metrics: lagging (PPM) & leading (FIT)

•Hard Failures (PPM focus)

- Factory*: visible at ATE/outgoing tests.
- Field*: latent, invisible w/o stress tests.
- Traceability via DfM (e.g., OPC).






•Soft Failures (FIT focus)

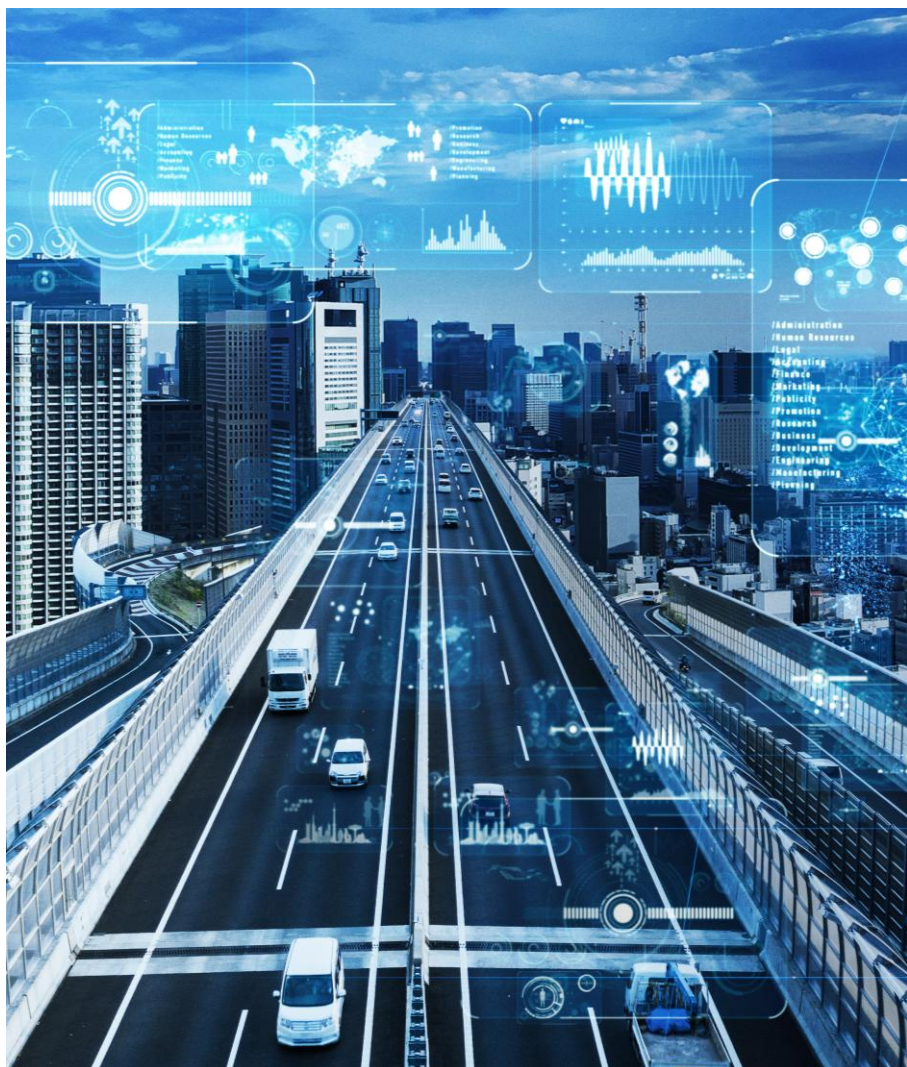
- Field errors*: visible if reported (ECC/system), invisible if silent (SDC)
- AEC-Q004 DfT + verification flows build systematic detection & ecosystem.



AEC-Q004 as the Linkage between IATF 16949 & ISO 26262

- Bridges quality and safety through FMEA, gating logic, and dual metrics (PPM & FIT)
- Drives continuous improvement, evolving from defect reduction to functional safety assurance

Characteristic	IATF 16949	AEC-Q004	ISO 26262
 Focus	Quality Management System & PPM Reduction	Core framework bridging quality and safety	Functional Safety (ASIL, SGV, PMHF)
 Hard Failure Handling	Handled via FMEA/PFMEA	DfM flow ensures OPC correction traced from FMEA	May cause Safety Goal Violation if not mitigated
 Soft Failure Handling	Latent defects managed via audits, SPC, PAT	DfT + Verification flow for Soft Failures (SER, transient)	Addressed by safety mechanisms (ECC, lockstep, diagnostics)
 Metrics	PPM, Cp/Cpk, audit scores	Dual governance: Quality (DPPM) × Safety (FIT/DC)	SPFM, LFM, PMHF, DC
 Improvement Driver	Customer requirements and audits	Extendable ecosystem: quality ↔ safety, unified under ZD	Ensures end-to-end safety compliance



Thank you!

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