HVM “Golden Recipe” Methodology for SiC Substrate Qualification Across Suppliers

Part 1

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2025 European Automotive Electronics Council Reliability Workshop (Bordeaux, France - October 2025)

Agenda

Part 1: VWC Intro and Problem Statement (VWG)

Part 2: Toward a Si-like solution for SiC (KLA)

Part 3: Data Results and Discussion (KLA)

Part 4: Conclusions and Next Steps (VWG & KLA)

Part 1: VWC Introduction and Problem Statement

VOLKSWAGEN GROUP
TECHNOLOGY

Group Technology

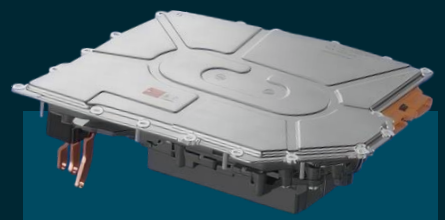
Volkswagen Group Power Electronics Strategy

Dr Michael Schmalz– Volkswagen AG, Group Technology
Key Expert Semiconductor Technology | 08.09.2025

VOLKSWAGEN GROUP
TECHNOLOGY

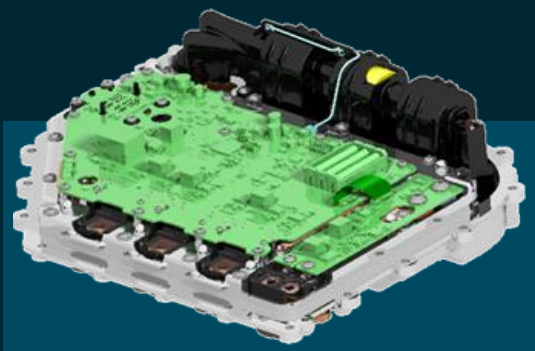
International Semiconductor Industry Group

VW Group- Evolution of E-drive power electronics



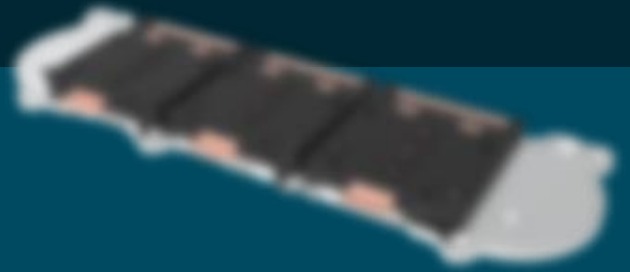
Step 1

Specification



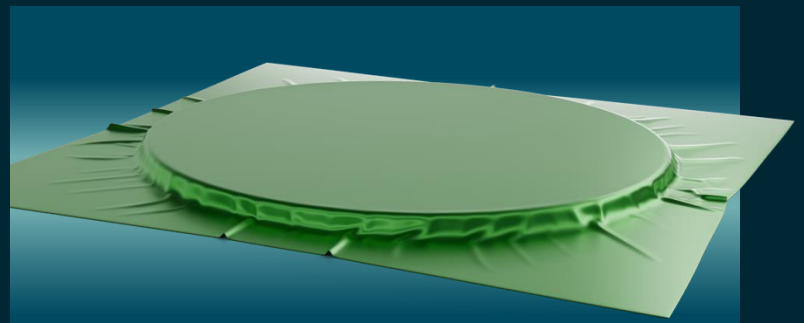
Step 2

In-house development



Step 3

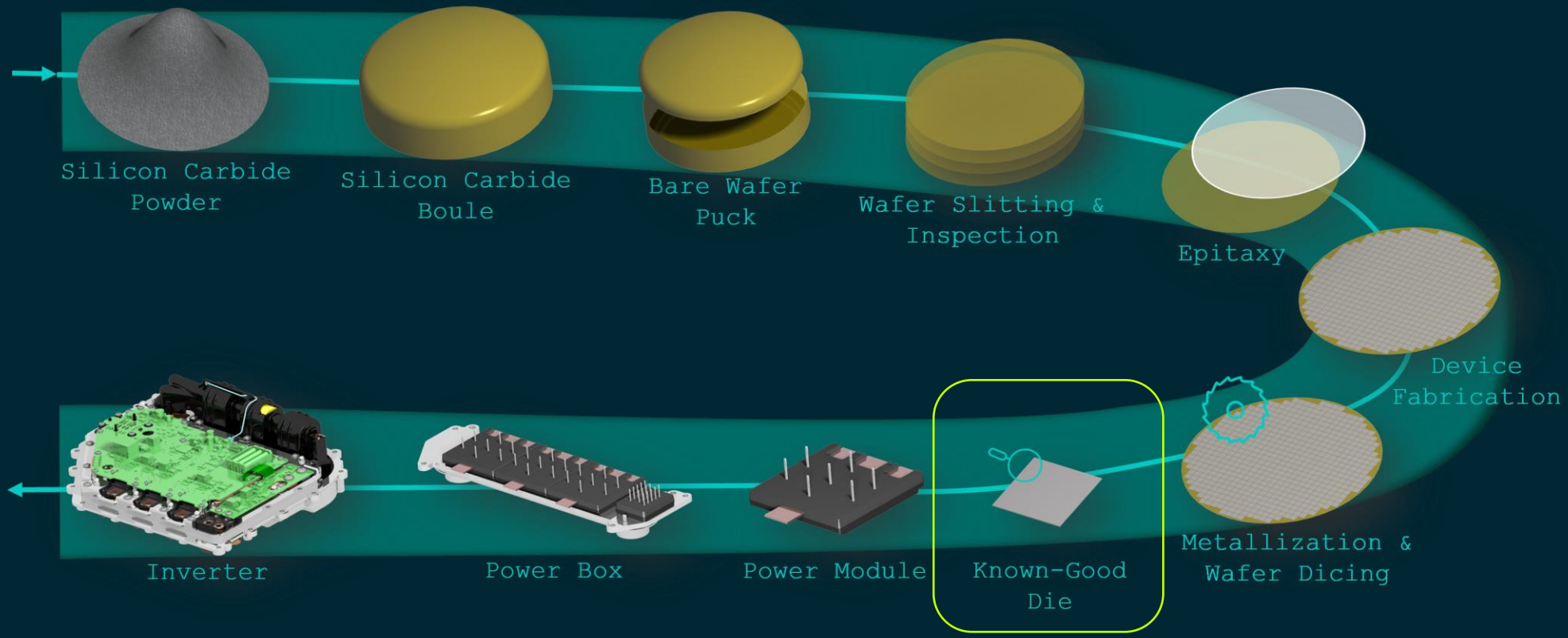
In-house development of sub-components



Step 4

In-house semiconductor design

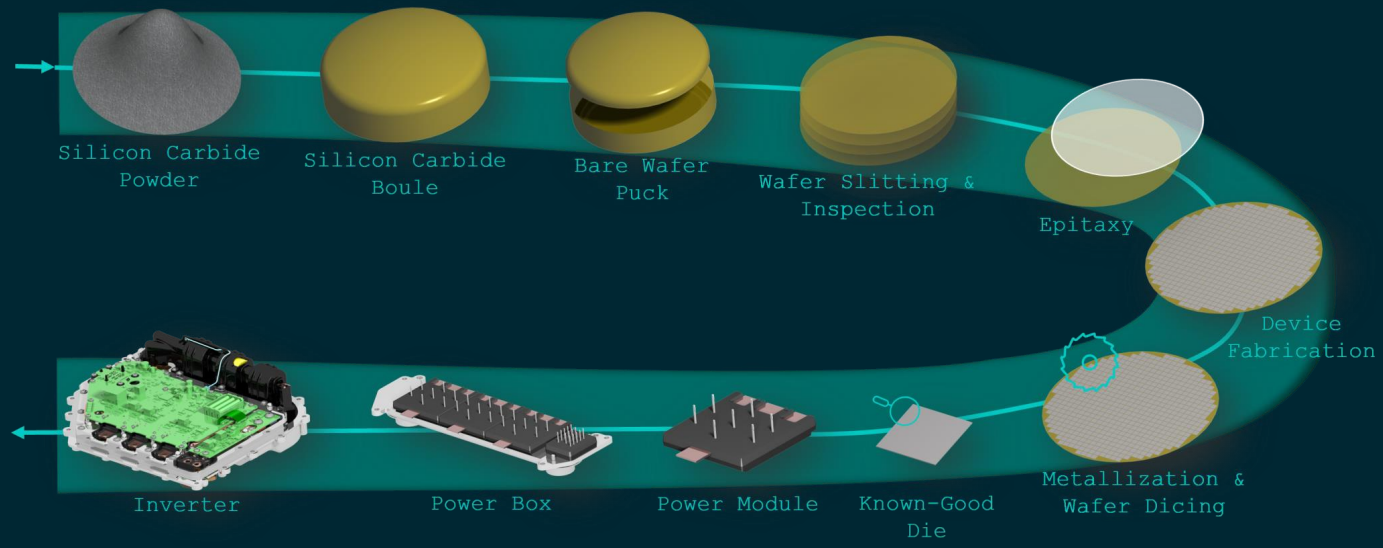
SiC MOSFET main production flow



Requirements landscape

VW customized SiC MOSFET chip:

- Performance conformity (electrical)
- Robustness & reliability
- Interface conformity to backend processes
- Cost-effectiveness
- Supply chain resilience



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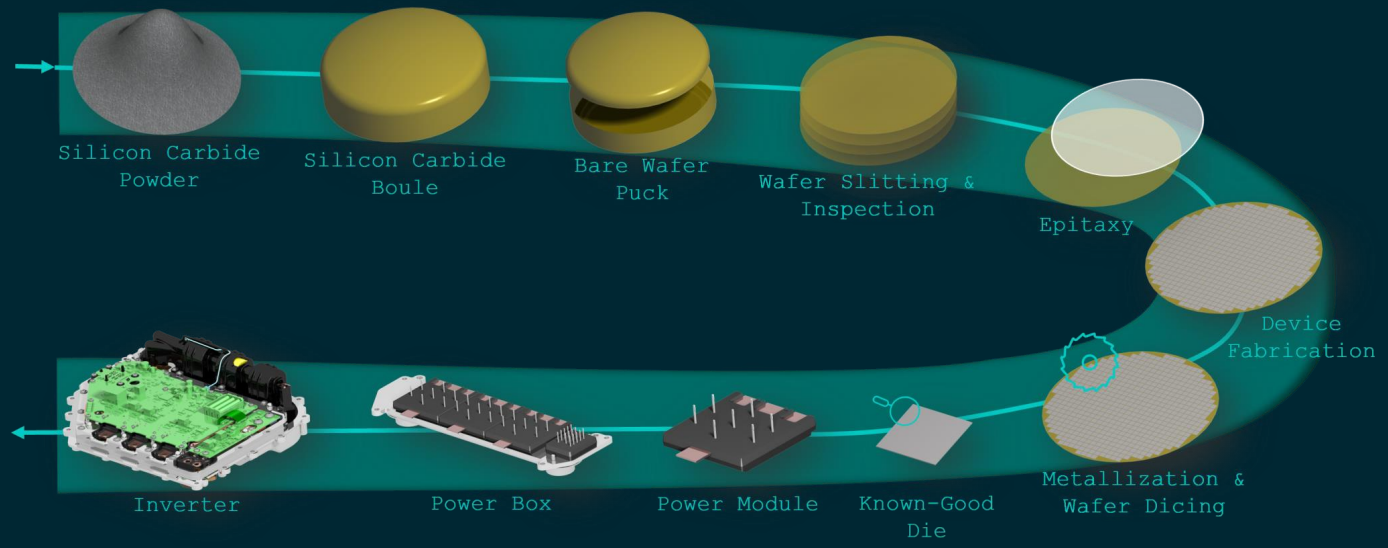
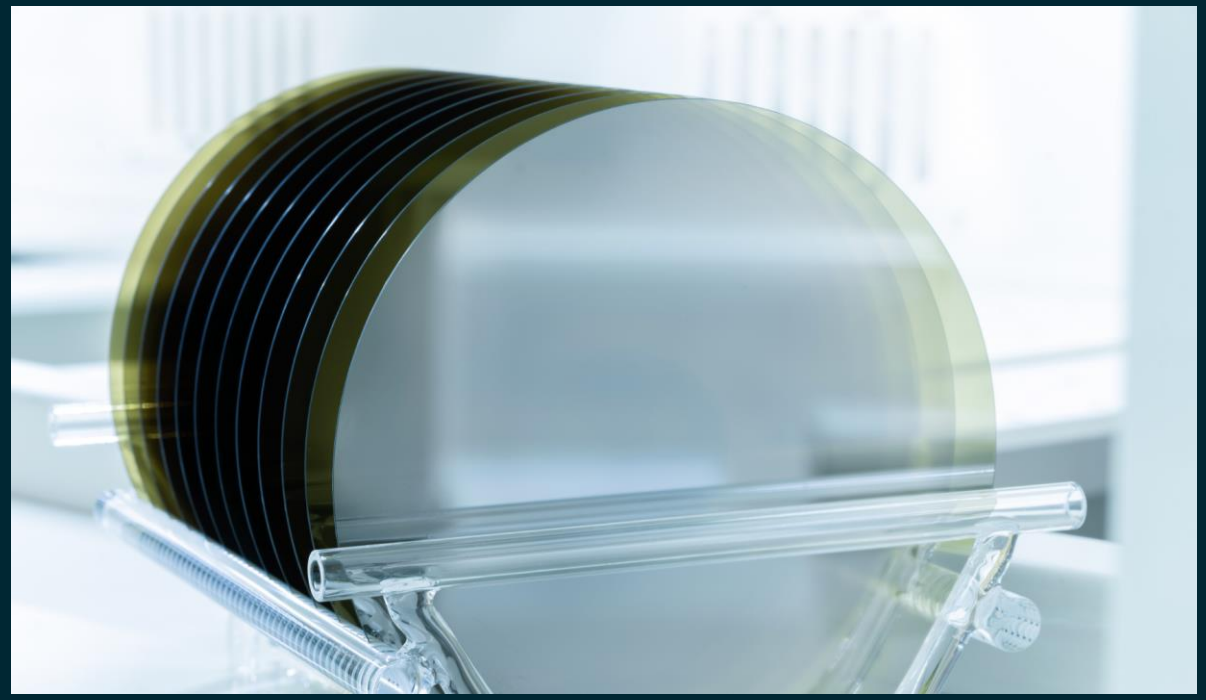


Impact of SiC raw wafer material on SiC Chip

- Performance conformity (electrical)
- Robustness & reliability
- Interface conformity to backend processes
- Cost-effectiveness
- Supply chain resilience



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Impact of SiC raw wafer material on SiC Chip

- Robustness & reliability
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Impact of SiC raw wafer material on SiC Chip

- Robustness & reliability
- Cost-effectiveness
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- Crystal defect metrology
- Epitaxy defect metrology
- Defect classification
- Defectivity map integration into SPC concepts
- Tool synchronization

Impact of SiC raw wafer material on SiC Chip

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Part 2: Toward a Si-like Solution for SiC

Collaborative goals

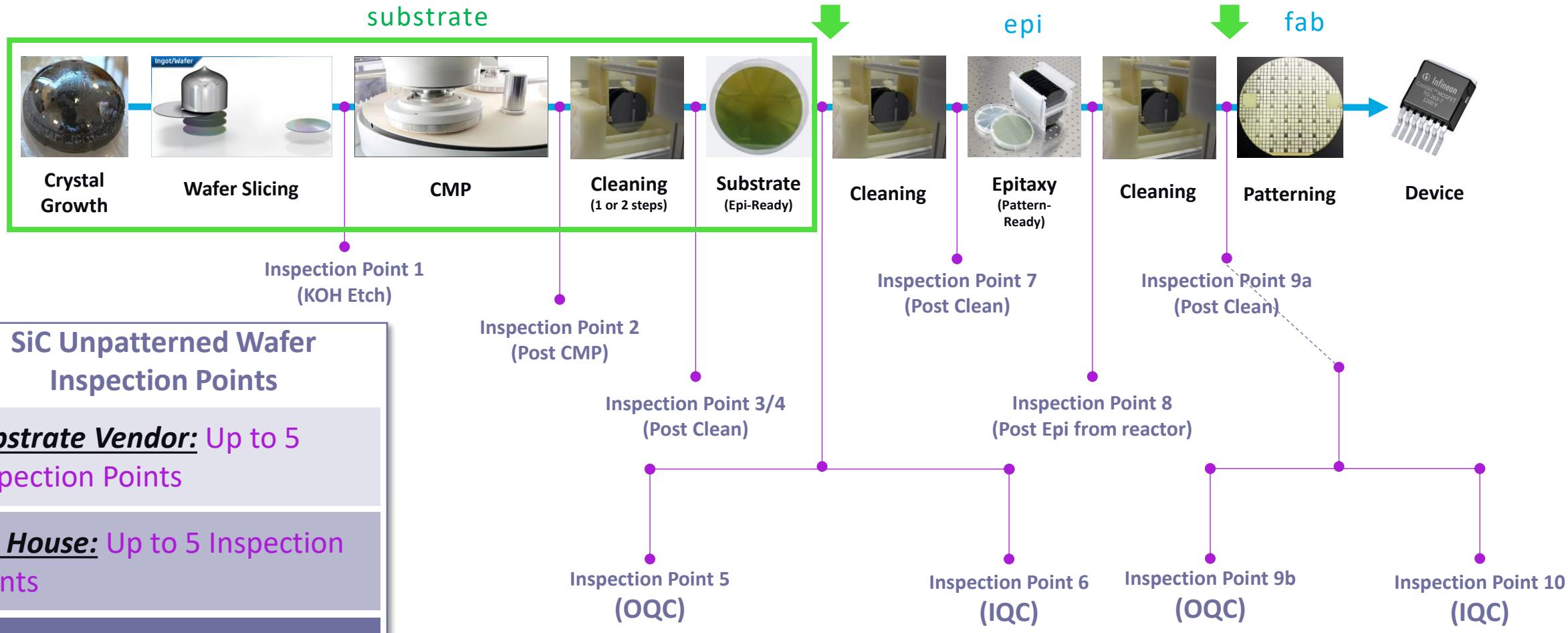
1. Help our partner succeed
2. Enable SiC substrate & Epi supplier advances in quality and reliability
3. Gain insight to develop the right tools and technology
   - Long time horizon engagement

SurfScan: 1st tool in the Si fab door

Better data. Better decisions. Faster Improvement

SiC Power Device:

Unpatterned Wafer Process Flow & Inspection Points



SiC Unpatterned Wafer Inspection Points

Substrate Vendor: Up to 5 Inspection Points

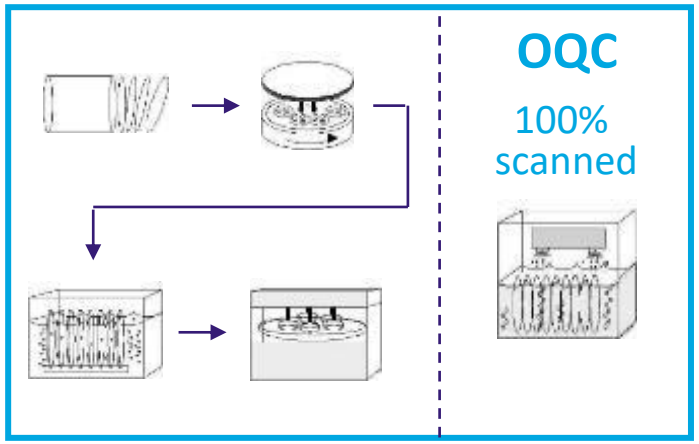
Epi House: Up to 5 Inspection Points

Device Maker: Up to 7 Inspection Points

OQC/IQC Methodologies

Silicon Supplier – Fab Handoff

Silicon Supplier



Surfscan

ITRS semi

Traceable data for each wafer

Specs

KLA

IC Fabs

IQC
- Sensitivity
- Defect Type
- Haze

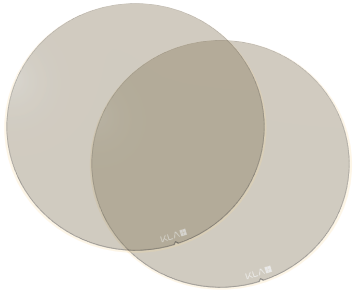
Process Modules
- Epitaxy
- Diffusion
- Lithography
- CMP
- Others

Surfscan

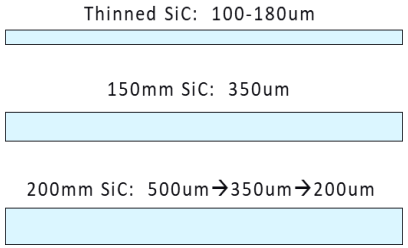
SEMI (industry) standard M59 mandates monitoring of killer defect types in Silicon. M81 controls Silicon Carbide

Requirements for HVM SiC success

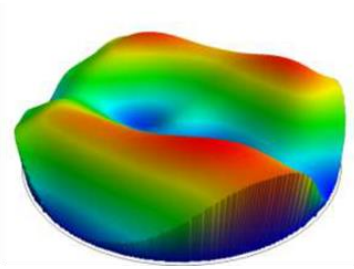
Handling



Transparent

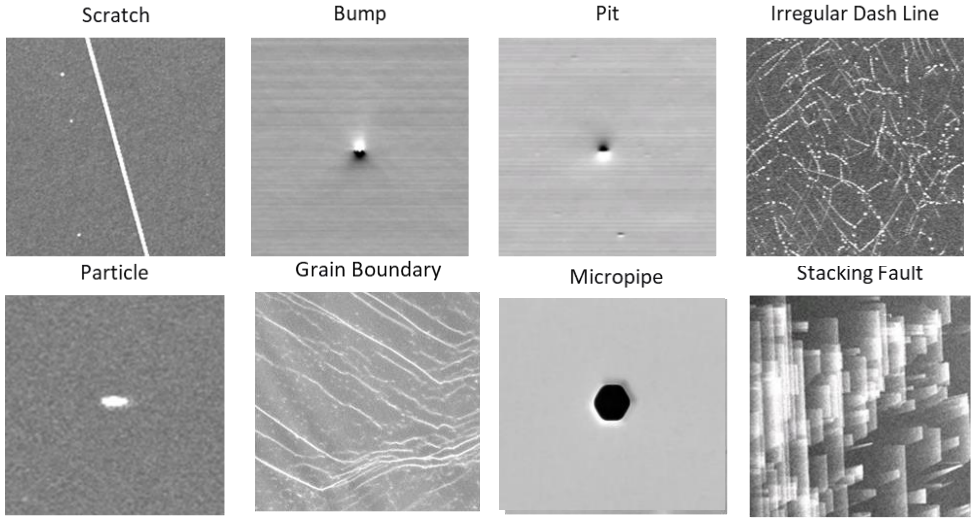


Varied thickness

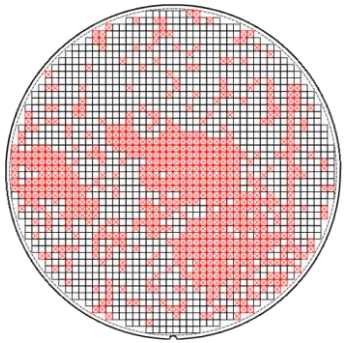


Bow & Warp

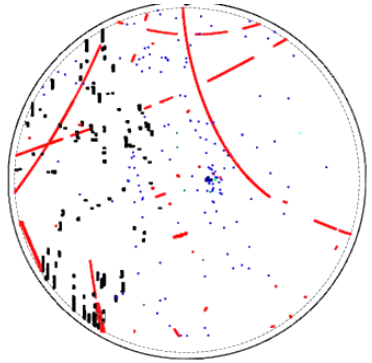
Sensitivity at HVM throughput



Actionable: SPC+



Pseudo-die



Binning

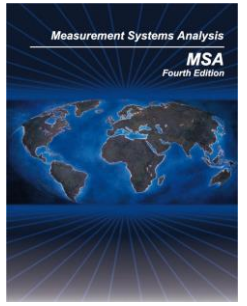
Defect Type	% Wafer Impact	Status
DOI 1	11.59420%	FAIL
DOI 2	17.39130%	FAIL
DOI 3	18.47826%	FAIL
DOI 4	0.36232%	PASS
DOI 5	70.65217%	FAIL
DOI 6	2.17391%	PASS
Total	80.79710%	FAIL

Disposition

Control Plan-ready

semi™

Standards & Automation



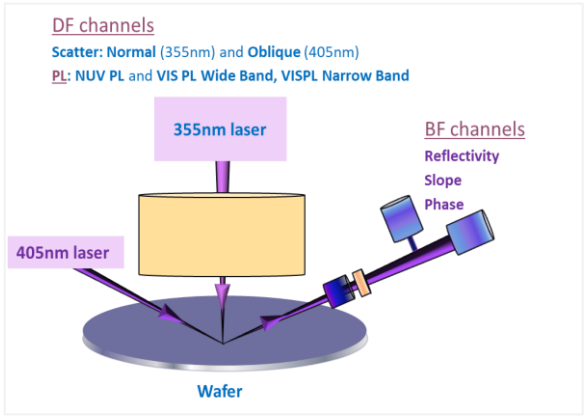
GR&R

Fleet management & matching

KLA's tools in this space

Candela 8520

405&355nm Laser

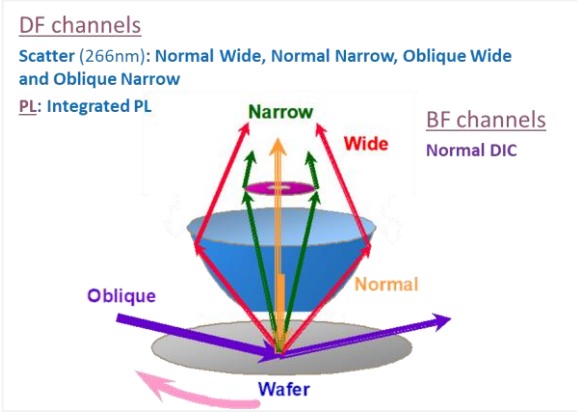


<1um sensitivity

~12WPH @8"

Surfscan SC1

266nm Laser



<100nm sensitivity

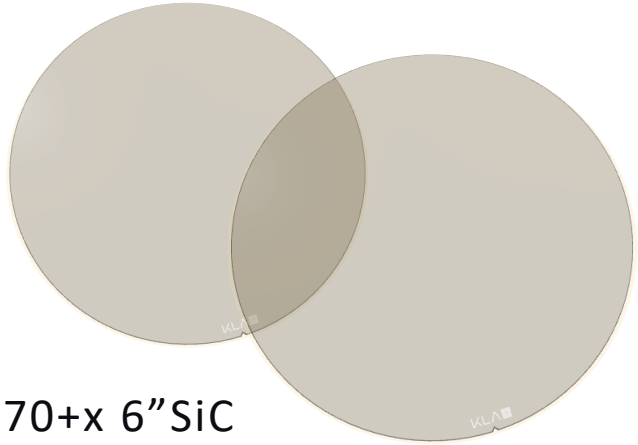
~32-110WPH @8"

- Original specialty substrate inspector
  - 25 year history. 300+ Candela 8520 field units
  - Engineering roots: agile/tunable multi-incidence, multi-detector, onboard analysis
- Extension of HVM Si industry standard
  - Built on SPx platform, 1000+ production units
    - Darkfield, Haze, PL. SiC and Si
  - Repeatable, matchable

Part 3: Results and Discussion

Data Set and Measurement System

Wafers



70+x 6”SiC substrates

36x 8” SiC substrates

13* Substrate Providers

- Sent to VW for supplier qualification

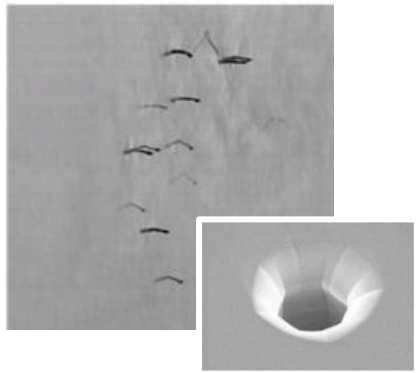
Equipment

- Common tool
  - KLA Candela 8520
  - SC1 defect inspection

“Golden Recipe”

Typical Defects of Interest*

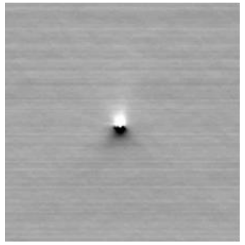
Micropipe



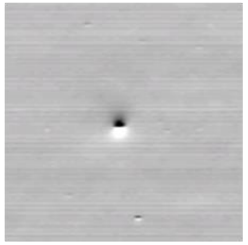
SEM Image

Stacking Fault

Bump



Pit

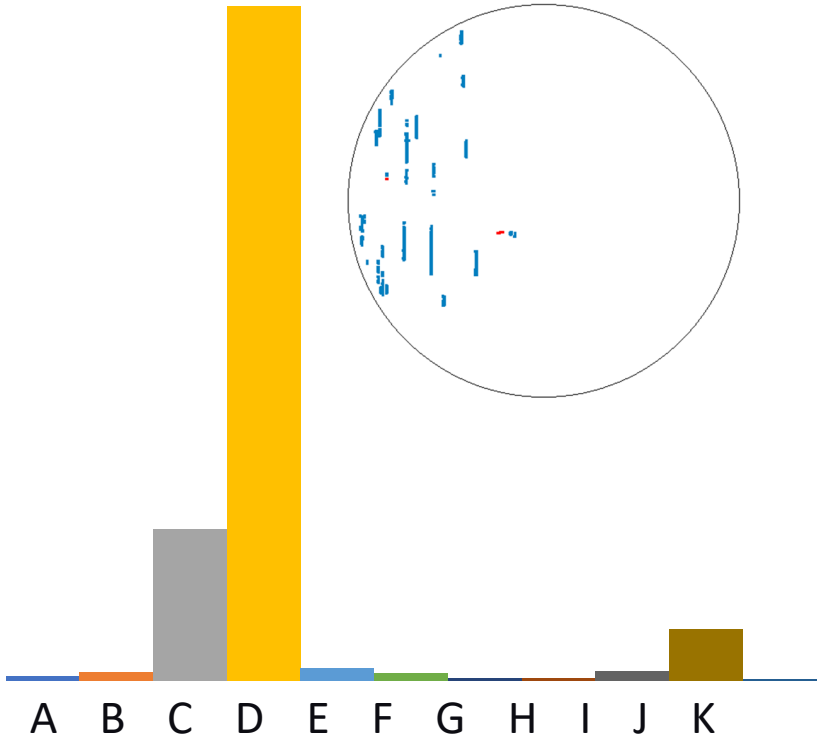


Scratch

*non-exhaustive

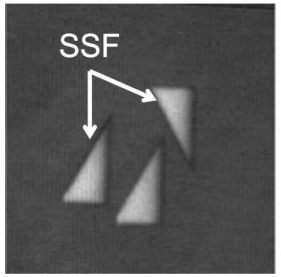
Supplier Qualification for Stacking Faults

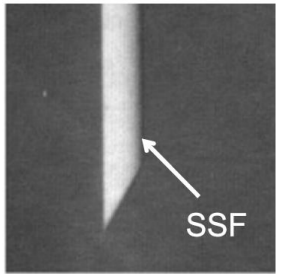
Avg. # of stacking faults per wafer from 11 SiC substrate providers



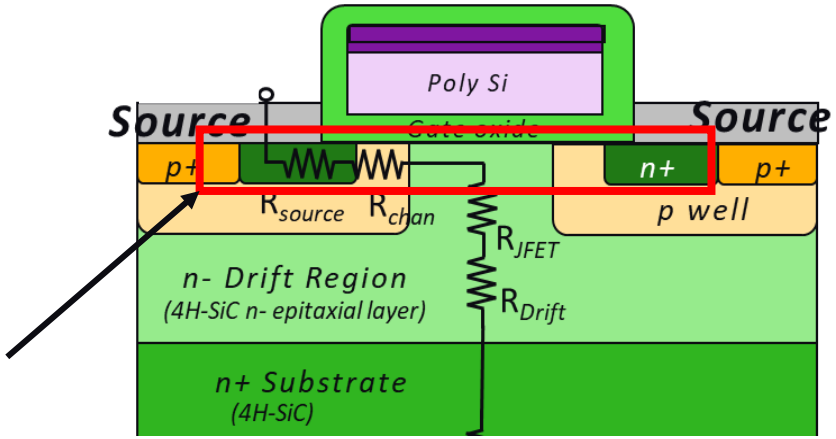
Substrate Supplier

Stacking faults can lead to reliability defect (Bipolar Degradation) through increased resistance in the area covered by the grown SSF



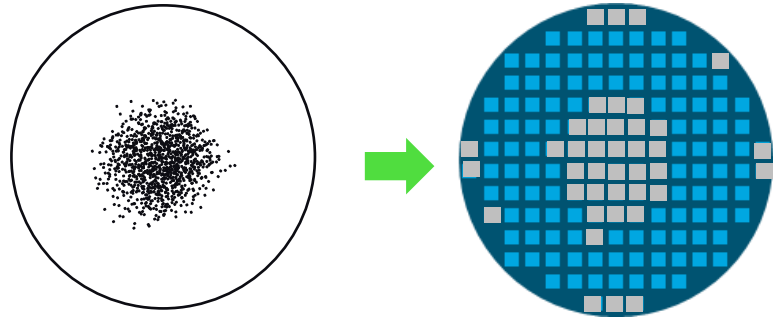


Defect images from: Kimoto, T. "Defect engr. in SiC technology for HV power devices" (2020 Appl. Phys. Exp 13 120201)



Mitigation:

1. Electrical verification measures
2. Defect screening- ink wafer areas with high defect density.

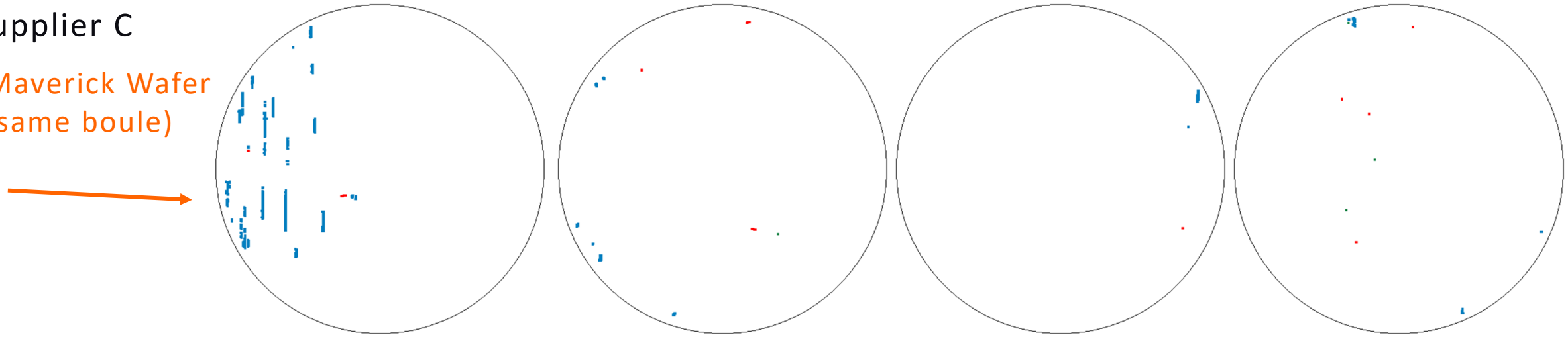


Sample Defect Maps: Stacking Faults

Variation drives 100% sampling

Supplier C

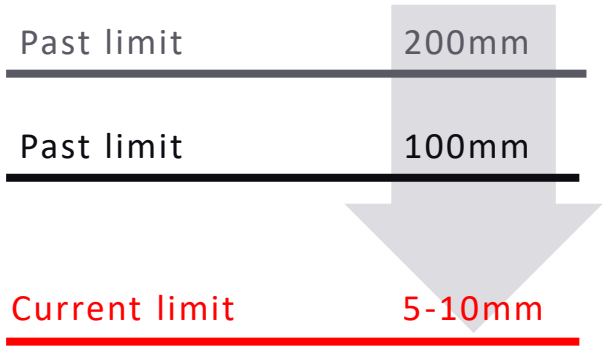
Maverick Wafer
(same boule)



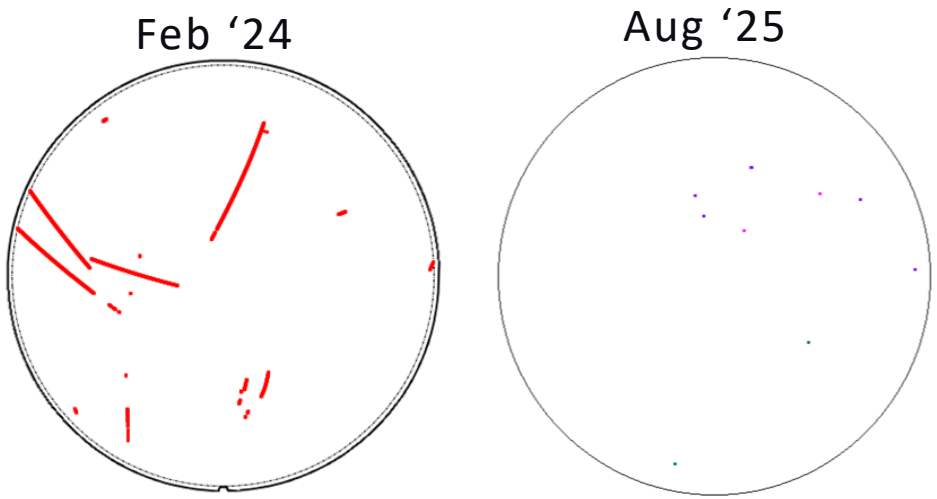
Scratch Stacking Fault Micropipe Bump Pit

Supplier Qualification for Scratches

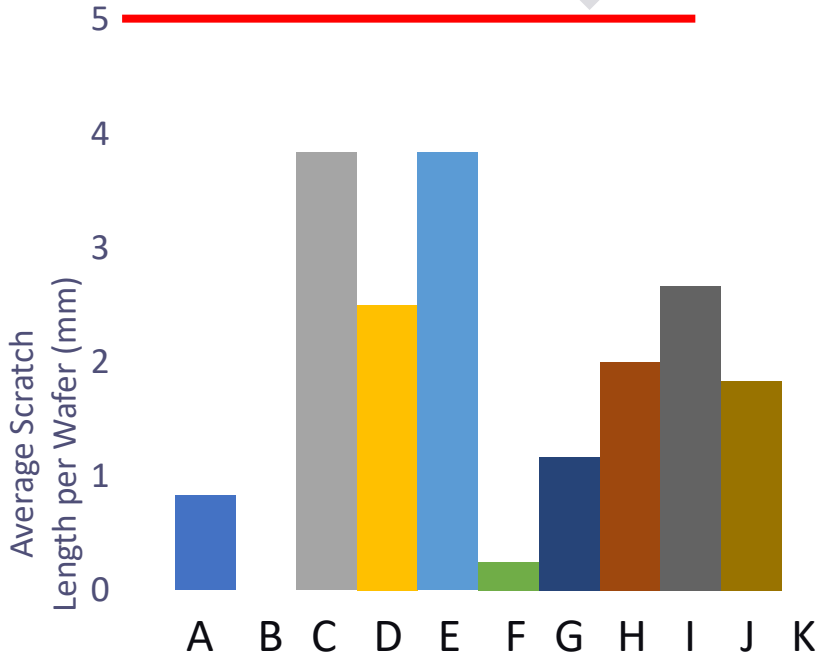
Industry-wide improvement



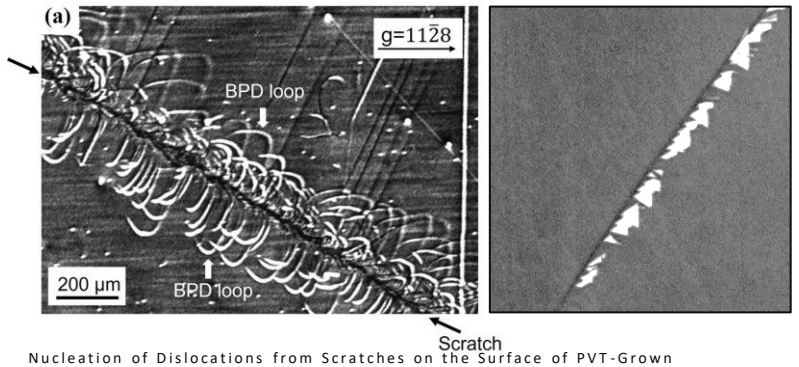
Supplier K



Total length~200mm



Scratches can be a nucleation site for defect growth



Nucleation of Dislocations from Scratches on the Surface of PVT-Grown 4H-SiC Wafers, S. Hu, et.al, *Journal of Electronic Materials, Jan 2025*

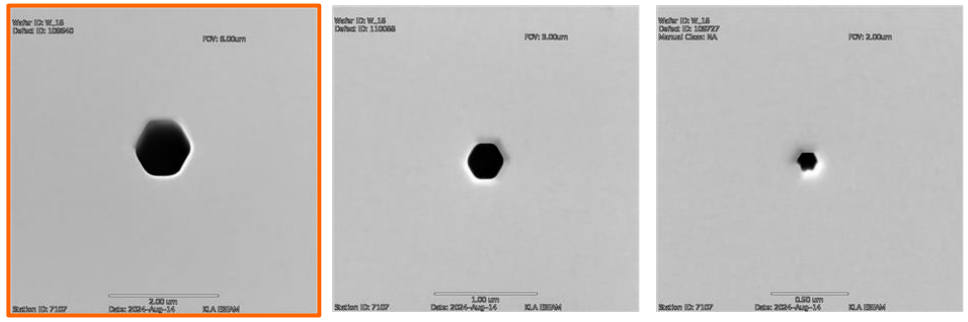
- BPD Loops
- TEDs (prismatic slip)
- Partial dislocation loop expansion
- Stacking faults, step bunching at EPI

Possible propagation/mitigation at Epitaxy

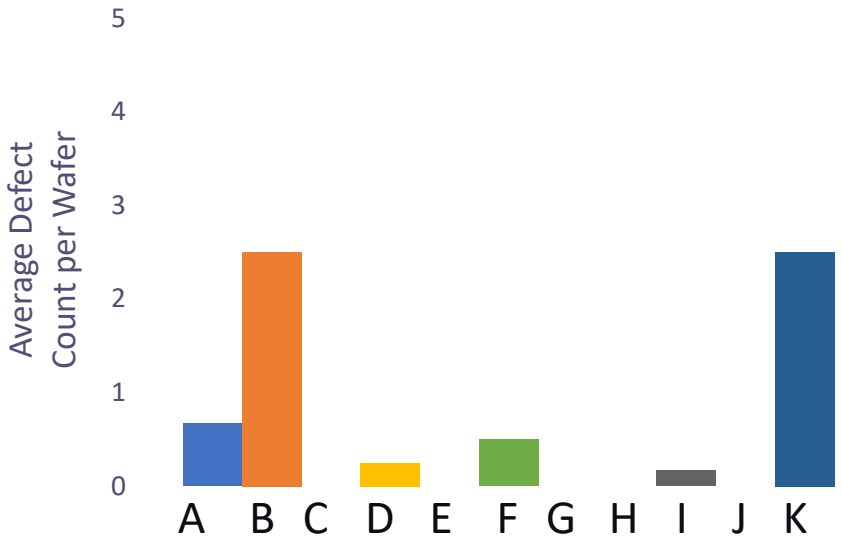
Supplier Qualification for Micropipes

Killer defect: varied sizes

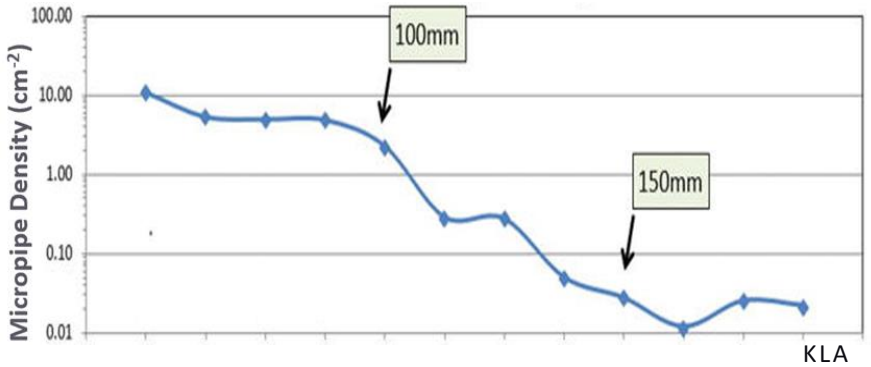
Current industry sensitivity



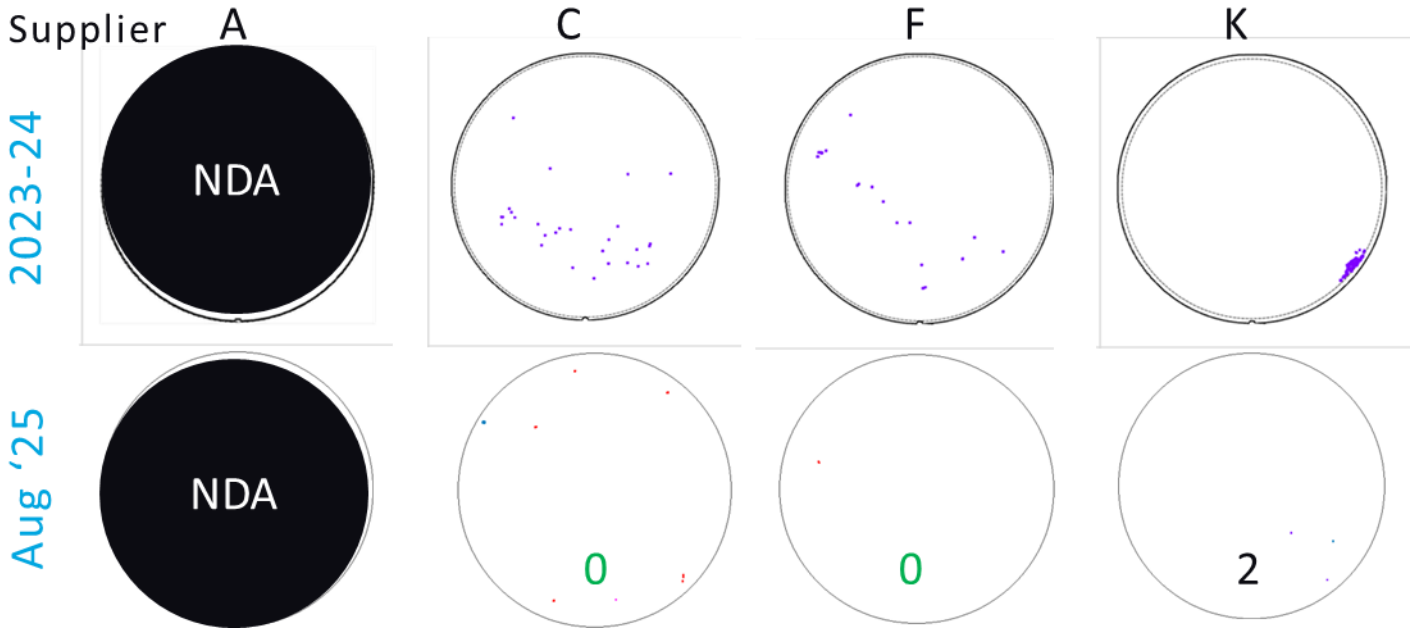
~800-1000nm ~300nm ~100nm



Micropipe density decreasing: < .1/cm^2

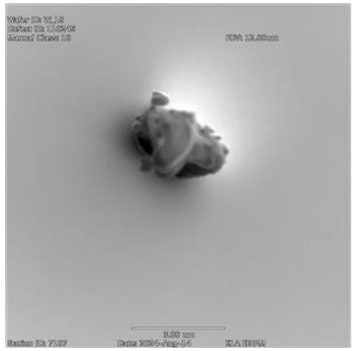


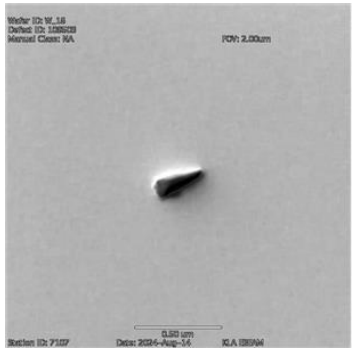
- Smaller diameter micropipes exist
- Characterizing ~100nm now on SC1
- SEM intensive

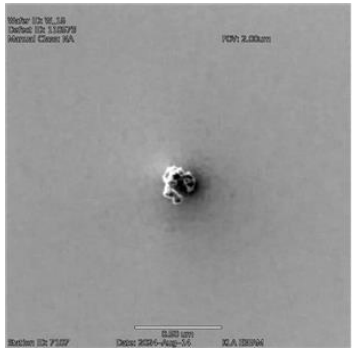


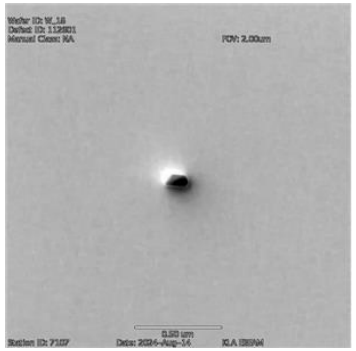
Supplier Qualification for Particles

Cleanable* and embedded


~5 um

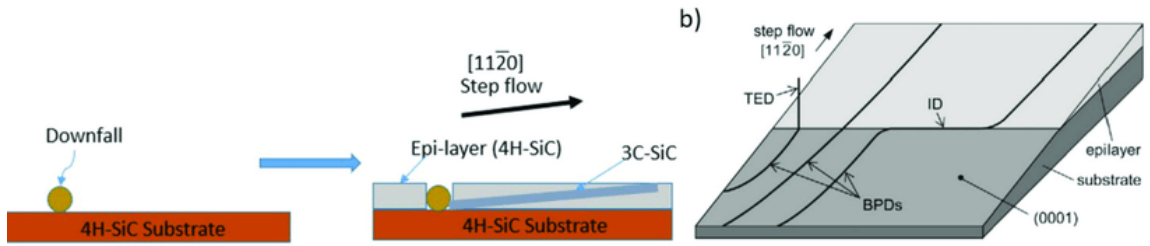

~300nm


~150nm


<100nm

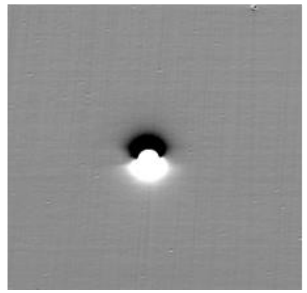
What size matters?

- Sources
  - 3C-SiC particles during crystal growth, Powder impurities, Furnace debris, slice, grind, CMP, Tools, Environment, Handling
- Effects: Yield and Reliability
  - Nucleation site for SF, dislocations and polytype inclusions
  - Can propagate through Epi. Growth variation, Thin GateOx, Doping disruption
  - Can cause failure, higher leakage currents, higher on-state resistance, premature breakdown, reduced carrier mobility.

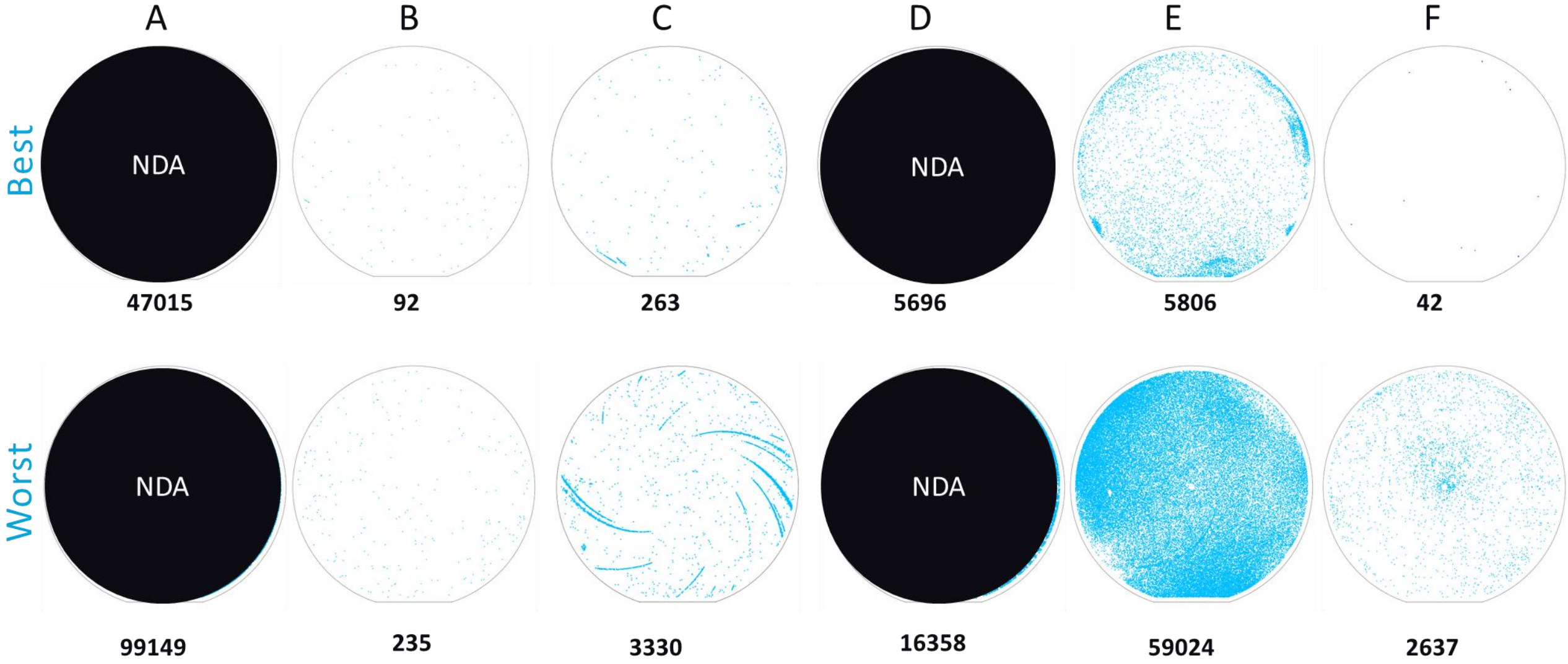


Review of Silicon Carbide Process for Power MOSFET, C. Langpoklakpam et.al, Crystals, 2022, www.mdpi.com/journal/crystals

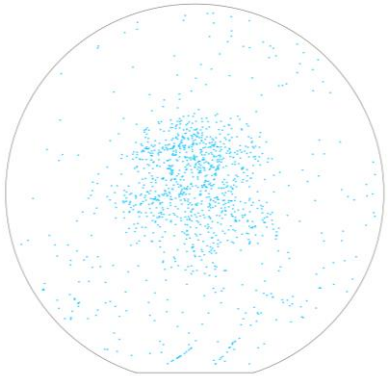
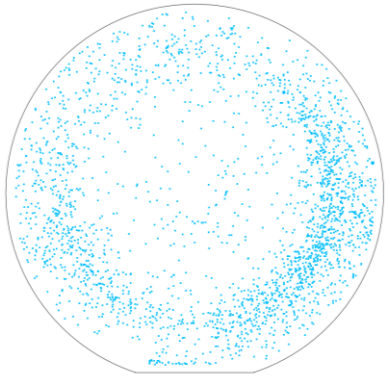
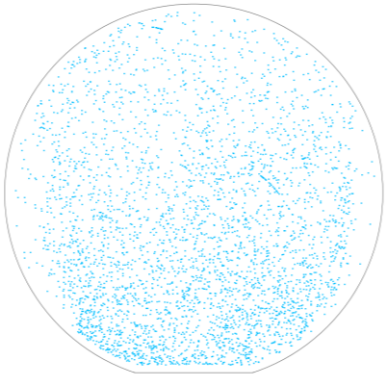
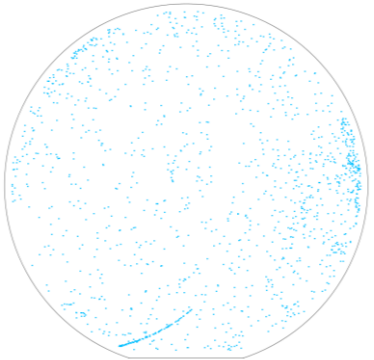
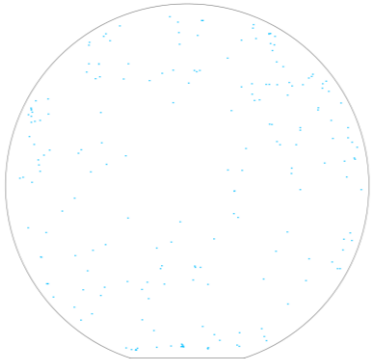
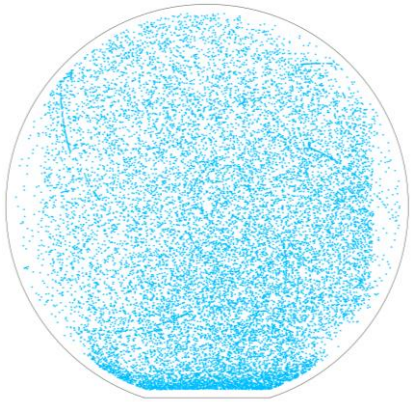
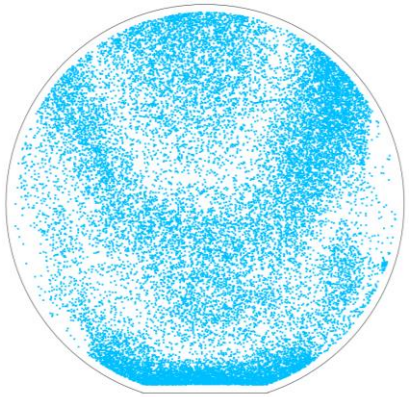
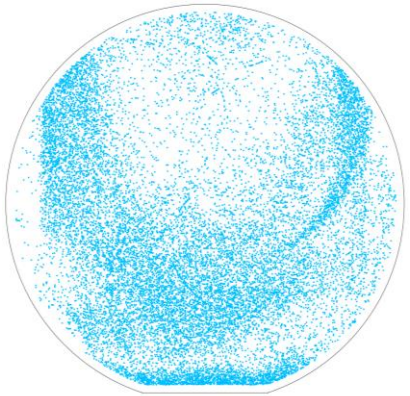
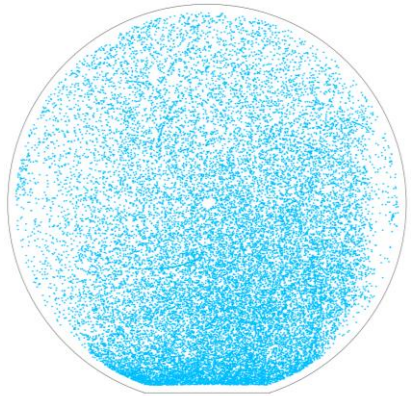
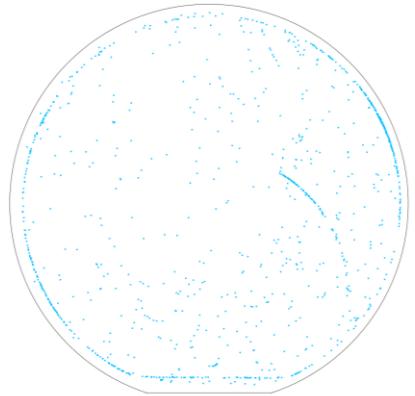
Downfall



Supplier particle comparisons at 110 WPH

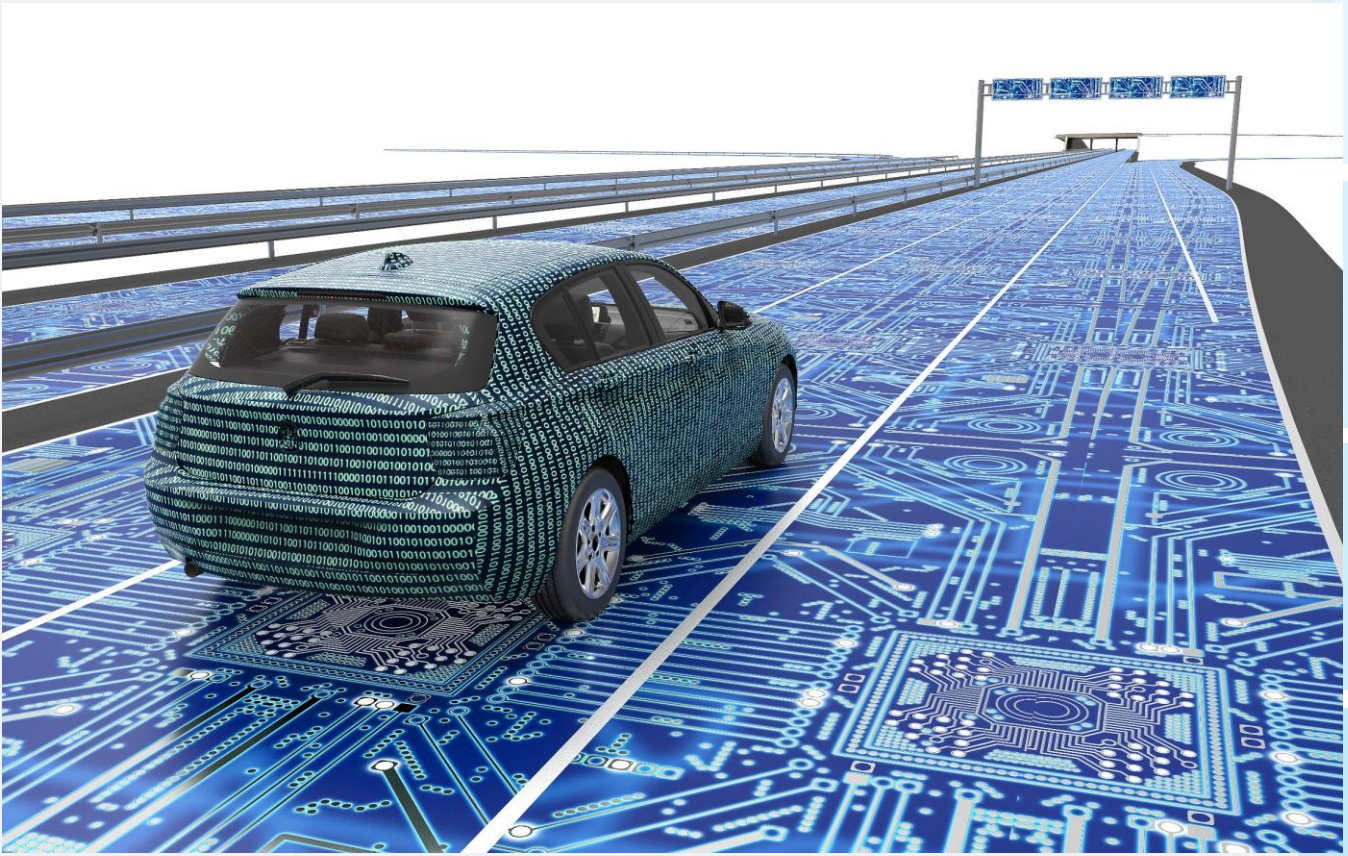


Supplier particle comparisons at 110 WPH

	G	H	I	J	K
Best					
	1231	**2504**	**3669**	**1370**	**204**
Worst					
	16702	**20742**	**18171**	**23124**	**1027**

Conclusions and Next Steps

Summary and next steps



Supplier selection is challenging in a rapidly changing marketplace. Partnership beneficial

Si-like tools and use-cases coming to SiC to drive improvement

Ongoing project to assess 6” and 8” substrates, continuing through Epi and beyond

6” baseline maturing for OM-detectable crystalline defects. Surface defect cleanliness varies widely with room for improvement. Variability drives high sampling

Thank You

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