4rthAEC-RW Europa 2025

Oct 8, 2025 – Introduction Session

Introduction

- AEC* Component Technical Committee, is the standardization body for establishing standards for reliable, high quality electronic components.
- Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing.
- The AEC website makes available the technical documents developed by the AEC Component Technical Committee (these documents can be downloaded directly).

- AEC is organizing Reliability Workshops on a yearly base since more than 20 years in the US!
  And since 2017, with a regular additional European edition

- This year, the European AEC Workshop is organized for the second time in close cooperation with ESREF 36th edition in Bordeaux

THANKS a lot for hosting us !!!!

* AEC : Automotive Electronics Council with 90 members across the automotive industry

AEC Membership Update

- **Current Membership:**
  - 90 Active Member companies
  - Tier-1 (21), Tier-2 (49), Tier-3 (21), Guest (5)

- **Key Members Lost:**
  - Sustaining (Tier 1): Aptiv (founding member), Denso, and Lear
  - Technical (Tier 2): Intel, pSemi, Schurter
  - Associate (Tier 3): None
  - Guest: None

- **New Member Applications**
  - Working on creating new membership ballot for 2025. Will include applications from late 2024 through mid-2025
  - Confirming all information received (application, automotive focus, tech representative, and questionnaire)

AEC Membership Applications / Changes

- **Application Status / Updates**
  - If you have an outstanding application, you can contact Mike Buzinski for status

- **Organization Status Change**
  - If you need to change details of membership due to corporate changes (name change, merger, split, logo change, etc.) contact Mike Buzinski

- **Company Representation**
  - We would like to limit formal company representation to 1 primary and 2 alternates to limit size of email lists
  - Company representatives could then distribute within their company
  - Additional company representatives can participate in committees, workshops and other activities

AEC Documents / Standards

50 AEC Documents

- Charter (2)
- Main Standards (7)
- Methods (25)
- General Guidelines & Standards (7)
- Templates (9)

Published Main Documents

1. AEC - Q100: Failure Mechanism Based Stress Test Qualification For Integrated Circuits
2. AEC - Q101: Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors
3. AEC - Q102: Failure Mechanism Based Stress Test Qualification for Discrete Optoelectronic Semiconductors in Automotive Applications
4. AEC - Q103-002 Rev - (Initial Release): Failure Mechanism Based Stress Test Qualification for Micro Electro-Mechanical System (MEMS) Pressure Sensor Devices
5. AEC - Q103-003 Rev - (Initial Release): Failure Mechanism Based Stress Test Qualification for MEMS Microphone Devices
6. AEC - Q104: Failure Mechanism Based Stress Test Qualification For Multichip Modules (MCM) In Automotive Applications
7. AEC - Q200: Stress Test Qualification For Passive Components

- AEC - Q001 Rev - D: Guidelines for Part Average Testing
- AEC - Q002 Rev - B: Guidelines for Statistical Yield Analysis
- AEC - Q003 Rev - A : Guidelines for Characterizing the Electrical Performance of Integrated Circuit Products
- AEC - Q004 Rev- (Initial Release): Automotive Zero Defects Framework
- AEC - Q005 Rev - A: Pb-Free Test Requirements
- AEC - Q006 Rev - A: Qualification Requirements for Components using Copper (Cu) Wire Interconnects
- AEC – Q007 Rev- (Initial Release): Failure Mechanism Based Testing Guidelines for Components Mounted to a Printed Board

AEC Working Groups & Task Forces

AEC Document #	AEC Document Title	Leader	Email
Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits	Ulrich Abelein, Infineon	ulrich.abelein@infineon.com
Q101	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications	Andreas Pinkernelle, Nexperia	andreas.pinkernelle@nexperia.com
Q102	Failure Mechanism Based Stress Test Qualification for Discrete Optoelectronic Semiconductors in Automotive Applications	Uwe Berger, Hella	uwe.berger@hella.com
Q103-001	MEMS Inertial Sensors	Mike Aldrich, Analog Devices	mike.aldrich@analog.com
Q103-002	Failure Mechanism Based Stress Test Qualification for Micro Electro-Mechanical System (MEMS) Pressure Sensor Devices	Mikola Blyzniuk, Melexis	mbl@melexis.com
Q103-003	Failure Mechanism Based Stress Test Qualification for MEMS Microphones Devices	Bassel Atala, STMicroelectronics	bassel.atala@st.com
Q104	Failure Mechanism Based Stress Test Qualification for Multichip Modules (MCM) in Automotive Applications	Steve Sibrel, Harman Tom Lawler, Consultant/Retired	steven.sibrel@harman.com tomjlawler@alumni.caltech.edu
Q105	Touch Screen & Display Module Systems	Steve Sibrel, Harman	steven.sibrel@harman.com
Q200	Stress Test Qualification for Passive Components	Saad Lambaz, Littelfuse	slambaz@littelfuse.com
Q004	Zero Defects Guideline	Rene Rongen, NXP	rene.rongen@nxp.com
Q006	Qualification Requirements for Components Using Copper (Cu) Wire Interconnections	Ulrich Abelein, Infineon Rene Rongen, NXP	ulrich.abelein@infineon.com rene.rongen@nxp.com
Q007	Board Level Reliability	Romuald Roucou, NXP	romuald.roucou@nxp.com
Universal CoDC	Universal CoDC Template	Mike Buzinski, Microchip	mike.buzinski@microchip.com
WBG	Wide Band Gap Components (SiC-Based Power Products)	Itasham Hussain, ZF	itasham.hussain@zf.com
Re-Org	Organizational Committee	Mike Buzinski, Microchip	mike.buzinski@microchip.com

AEC – Recent Ballots / Updates

- **Q006 Rev B - 'Copper Wire Qualification'**
  - Posted to website
- **Q004-001 Rev – 'Zero Defects Casebook Examples'**
  - Ballot approved. Comments and final editing in process
- **Q100 CDC Template – 'Q100 CDC Template'**
  - Ballot complete. Will release after current Q100 Rev J1 ballot completed
- **Q200-006 – 'Terminal Strength Surface Mount / Shear Strength Test'**
  - Ballot complete. Will release after final edits complete

AEC – Organizational Changes

- **Leadership Changes**
  - Mike Buzinski takes over chairman position

- **Charter Updated (Rev H) to allow for incorporation of AEC**
  - Defines the role of the Executive Team
  - Will create a more lasting organization that can survive member instabilities
  - Will allow for financial assets and payments
  - Fees will allow:
    - Website enhancements
    - Payment of workshop from annual dues
    - Use of management company to assist with administrative activities

- **Organization committee has started**
  - Contact Mike Buzinski if interested in participating

AEC Executive Team

1. **Team Members**:
   - Mike Buzinski (Chair) — Microchip
   - Rene Rongen (Vice Chair) — NXP Semiconductors
   - Bassel Atala — STMicorelectronix
   - Carsten Ohlhoff — Auomovio (Conti)
   - Ulrich Abelein — Infineon Technologies
   - Ludger Kappius — Forvia (Hella)
   - Steven Sibrel — Harman
   - Zhongning Liang — NXP Semiconductors
   - Mark Kelly (Consultant)

2. **Objectives:**
   - Ongoing — Committee Meetings & Working Groups/ Workshops
   - Short Term — Re-organization (First Step : Charter Revision)
   - Mid Term — Website modernization
   - Long Term — Reliationships Mgmt: JEDEC/ ESDA/ Chinese Standards

AEC – Membership Responsibility

- **AEC is a volunteer organization to develop industry standards. To be successful, members need to volunteer and participate**

- **Volunteer Activities / Requirements**
  - Committee participation
  - Ballot voting consistency
    - Every ballot should be completed
    - Abstain is a valid response if the ballot does not apply to your organization
    - Companies that fall below 80% response will be contacted to improve
    - Companies that fail to reach 50% response will be suspended

- **Administrative Help Welcomed**
  - Anyone interested in assisting in reviewing membership applications or other general administration, contact Mike Buzinski

Agenda - Wednesday October 8, 2025

08:00 AM - 08:30 AM		**Registration**		
08:30 AM - 09:00 AM	**O**	**Welcome & AEC Updates**	Rene Rongen	NXP Semiconductors
09:00 AM - 10:30 AM		**Technical Session 1: Passives, LEDs, WBG**	Moderator: Uwe Berger	Hella (Forvia)
09:00 AM - 09:30 AM	**T1.1**	Tantalum Polymer Capacitors Trends and Challenges - Software Defined Vehicles (SDV)	Cristina MotaCaetano	Yageo
09:30 AM - 10:00 AM	**T1.2**	Need for speed? A Comparative Study of H2S-Corrosion Tests	Jennifer Rieder	amsOSRAM
10:00 AM - 10:30 AM	**T1.3**	HVM “Golden Recipe” Methodology for SiC Substrate Qualification Across Suppliers	Jay Rathert; Michael Schmalz	KLA / Volkswagen
10.30 AM - 11.00 AM		**Break**		
11:00 AM - 11:30 AM		**Technical Session 2: Invited Paper**	Moderator: René Rongen	NXP Semiconductors
11:00 AM - 11:30 AM	**T2.1**	SAFETY in cars	Franck Galtie	NXP Semiconductors
11:30 AM - 12:00 PM	**W1**	Q102 / Optoelectronics	Uwe Berger	Hella (Forvia)
12:00 PM - 12:30 PM	**W2**	Q200	Alan Cooper	Yageo
12:30 PM - 01:30 PM		**Lunch**		
01:30 PM - 02:00 PM	**W3**	Q101 / Discretes	Andreas Pinkernelle	Nexperia
02:00 PM - 02:45 PM	**W4**	Wide Band Gap	Massimiliano Regardi	Nexperia
02:45 PM - 03:45 PM		**Technical Session 3: Power Modules**	Moderator: Martin Geiger	Microchip
02:45 PM - 03:15 PM	**T3.1**	Advanced Estimation of Remaining Useful Lifetime for Power Modules	Horst Lewitschnig	Infineon Technologies Austria AG
03:15 PM - 03:45 PM	**T3.2**	Thermal Fatigue in Copper Wire Bonds under Power Cycling: Acceleration Model and Influence of Different Wire Types	Carlo Neva	STMicroelectronics
03:45 PM - 04:15 PM		**Break**		
04:15 PM - 4:45 PM		**Technical Session 3: Power Modules (cont'd)**	Moderator: Martin Geiger	Microchip
04:15 PM - 04:45 PM	**T3.3**	New HAST and non-destructive evaluation methods for Power Modules	Etienne Wortham	Zestron
04:45 PM - 05:00 PM	**W5**	Q007 / Board Level Reliability	Romuald Roucou	NXP Semiconductors
05:00 PM		**Wrap-up Day 1**		

Agenda - Thursday October 9, 2025

08:15 AM - 08:30 AM	**O**	Welcome	Rene Rongen	NXP Semiconductors
08:30 AM - 09:00 AM	**W6**	Extended Mission Profiles	Rene Rongen	NXP Semiconductors
09:00 AM - 10:30 AM		**Technical Session 5: Extended/ Severe Mission Profiles**	Moderator: Bassel Atala	STMicorelectronics
09:00 AM - 09:30 AM	**T4.1**	Extended Lifetime Evaluation – An OEM Point of View	Stefan Simon	Audi
09:30 AM - 10:00 AM	**T4.2**	Rethinking “Automotive”: How to Specify Components for Tomorrow’s Mobility	Francois Gouyou	Valeo
10:00 AM - 10:30 AM	**T4.3**	Considerations and Challenges in the Use of AEC-Q Components for Space Missions	Gonzalo Fernandez; Anastasia Pesce	Alter Technology / ESA
10.30 AM - 11.00 AM		**Break**		
11:00 AM - 11:30 AM	**W7**	Q004 / Zero Defects & Q006 / Cu-wire	Rene Rongen	NXP Semiconductors
11:30 AM - 12:30 PM		**Technical Session 6: Zero Defects**	Bassel Atala	STMicorelectronics
11:30 AM - 12:00 PM	**T5.1**	Advancing Zero Defect Through Process-Oriented Reliability and Soft Error Risk Integration	Calvin Yang	SGS
12:00 AM - 12:30 PM	**T5.2**	Technical cleanliness for electronic components	Uwe Berger	Hella (Forvia)
12:30 PM - 01:30 PM		**Lunch**		
01:30 PM - 02:00 PM	**W8**	Q100 IC & CDC Template	Moderator: Bassel Atala	STMicorelectronics
02:00 PM - 03:00 PM		**Technical Session 7: Zero Defects / Memory**	Moderator: Martin Geiger	Microchip
02:00 PM - 02:30 PM	**T6.1**	Outliers Detection for Zero Defect on Non-Normal and Highly Multivariate Data	Francois Bergeret; Francois Bourlon	Ippon Innovation / NXP Semiconductors
02:30 PM - 03:00 PM	**T6.2**	Reliability Assessment of Single-Ended PCM in Automotive Microcontrollers Compliant with AEC-Q100 Standards	Fabio Dell'Orto	STMicorelectronics
03:00 PM - 03:30 PM		**Break**		
03:30 PM - 04:00 PM		**Technical Session 8: ESD**	Moderator: René Rongen	NXP Semiconductors
03:30 PM - 04:00 PM	**T7.1**	New Contact-Based CDM Methods Needed to Align with ESD Roadmap	Greg O'Sullivan; Sumit Tayal	Micron
04:00 PM - 04:15 PM	**W9**	Q104 / MCMs	Rene Rongen	NXP Semiconductors
04:15 PM		**Wrap-up Day 2 and Closure**		

AEC-RW Europe 2025 – October 8 & 9

On behalf of ***AEC's General Chair, Mike Buzinski***, we want to thank the ESREF Organization for this excellent opportunity to have the AEC RW 2025 under the ESREF 2025 umbrella

With a special thanks to:

François Marc

Nicolas Nolhier

Laura Savarit

for their excellent support!

Organizing Committee of AEC-RW 2025

René Rongen	Claudia Palumbiny	Ludger Kappius	Martin Geiger	Zhongning Liang
NXP Semiconductors	Infineon Technologies	Forvia (Hella)	Microchip	NXP Semiconductors
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Future Workshops

- **2026 AEC US Workshop – Novi, MI**
  - 2026 Workshop to be held in early April @ Sheraton Novi Hotel
- **2026 AEC Asia Workshop – Hsinchu, Taiwan**
  - **FIRST** Asian workshop October 14-15 @ Ambassador Hotel
- **2027 AEC US Workshop – Location tbd**
  - Workshop planned for April.
  - Looking for feedback if members would be interested in alternate venue
- **2027 AEC EU Workshop**
  - In collaboration with ESREF

2026 AEC Reliability Workshop

Novi, Michigan – Sheraton Hotel

- **Date: April 2026 (Finalizing dates)**
- **Call for Presentations currently being finalized**
- **Format to follow previous Workshop events**
  - Monday evening TC meeting
  - Technical Sessions Tuesday, Wednesday, and Thursday
  - Workshop Panel Sessions reviewing AEC documents & activities

AEC-RW Asia 2026 in Hsinchu, Taiwan

Dave Chen, Rene Rogen

- **First AEC Workshop in Asia**
  - iST to host and cover facility costs
  - iST and AEC to coordinate on registration and organization
  - Attendee responsible for travel and accommodations
- **Format similar to European format**
  - Tuesday evening TC meeting
  - Technical Sessions Wednesday and Thursday
  - Both Technical presentations and working sessions on standards.

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Organized by the AEC Technical Committee

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