Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits

M. Kelly (1), L.G. Henry (2), J. Barth (3), G. Weiss (4), M. Chaine (5), H. Gieser (6), D. Bonfert (6), T. Meuse (7), V. Gross (8), C. Hatchard (9), I. Morgan (9)

(1) Delphi Delco Electronics Systems, P.O. Box 9005, M/S R117, Kokomo, IN 46904-9005, USA
Tel: 765-451-7084, Fax: 765-451-9647, e-mail: mark.a.kelly@delphiauto.com

(2) ORYX Instruments Corporation, 47341 Bayside Parkway, Fremont, CA 94538, USA
Tel: 510-249-6318, Fax: 510-249-1150, e-mail: lghenry@oryxinstruments.com

(3) Barth Electronics Inc., 1300 Wyoming St., Boulder City, NV 89005, USA

(4) Lucent Technologies, 555 Union Blvd., Room 23R-255ES, Allentown, PA 18103, USA

(5) Micron Technology Inc., 8000 South Federal Way, P.O. Box 6, Boise, ID 83707-0006, USA

(6) Fraunhofer-Institute Reliability and Microintegration (IZM), Hansastr.27d, D-80686 Muenchen, Germany

(7) KeyTek, One Lowell Research Center, Lowell, MA 01852-4345, USA

(8) IBM Microelectronics, 1000 River St., Dept. E71/ZIP967J, Essex Junction, VT 05452, USA

(9) Advanced Micro Devices, One AMD Place, P.O. Box 3453, M/S 66, Sunnyvale, CA 94088, USA

Abstract – This paper presents the results of a search for a more effective stimulus suitable for assessing the latch-up susceptibility of integrated circuits. Different transient stimuli and amplitudes were found to have varying effectiveness in creating a latch event. The investigation also identified the inadequate response and recovery of existing test system power supplies and need for appropriate isolation techniques.

Introduction

The phenomenon of latch-up (LU) has existed for many years. Identification of latch-up susceptible integrated circuit designs is critical in this era of increased reliability and reduced costs being driven by the electronics industry. The majority of latch-up characterization is performed using JEDEC Standard No.17 [1] and JEDEC Standard 78 [2]. Through the implementation of latch-up design rules (best practices developed over the years to reduce/eliminate latch-up susceptibility), devices failing to meet JEDEC latch-up requirements at room temperature are uncommon.

Static or dynamic stresses in various time domains may trigger latch-up. Several studies [3,4,5] have shown that static test methods with slowly applied voltage or current (millisecond timeframe) do not identify all weak devices. Although devices seem to be robust according to standard latch-up characterization, device latch-up failures were occurring during accelerated stress testing (burn-in) and in the field. These findings suggest that the static nature of the JEDEC latch-up test at room temperature may be a “less than ideal” method of determining latch-up susceptibility. Therefore, different trigger stimuli were investigated to help identify potentially sensitive circuit designs

This early work served as the foundation for the creation of the ESD Association (ESDA) Transient Induced Latch-Up (TLU) working group WG-5.4. The development of a new standard for latch-up testing not only builds upon previous test standards but also requires the collaborative efforts of many individuals from different companies. Each contributor brings a unique perspective derived from experience with a particular mixture of technologies, device applications, and test equipment. The present

ESDA WG-5.4 has members from ten different companies and includes representatives from three equipment manufacturers. Collection of data using new techniques is facilitated by the sharing of known problematic devices among the members in round-robin testing. Identification and removal of obstacles hindering the implementation of new automated equipment LU stress techniques is also a major objective for the working group.

In this paper, we first present a brief background on early latch-up work and then review the issues surrounding the power supply response. We then discuss the efforts on manual and automated RC TLU testing methodology. We also review the TLU test results for transmission line pulse (TLP) methodology. Finally, we discuss the results for Bi-polar stress trigger TLU methodology.

Background

The need to implement complementary (both N-type and P-type) transistors on an integrated circuit can often result in current paths parallel to a desired functional circuit. Latch-up (LU) occurs from the activation of four-layer pnpn structures (thyristors) that are parasitically inherent to certain integrated circuit (IC) technologies. This undesirable parasitic path is composed of bipolar transistors that operate as intended under normal conditions. During abnormal conditions, the bipolar transistors can be turned on by a trigger stimulus. Consequently, large amounts of current may be drawn from the power supply producing either circuit malfunction and/or irreversible damage. This reduction in circuit resistance is characteristic of latch-up.

Working group WG-5.4 attempted to improve the efficiency of latch-up screening in two different ways. Since LU is initiated by a collection of charge carriers at diffused layers (resistance) acting in combination with parasitic bipolar transistors, the goal was to maximize this charge density while minimizing the total transferred energy. Too much injected energy could result in thermal damage before useful measurements could be made. This consideration and the finite lifetime of injected carriers support the greater effectiveness of short transients for assessing latch-up immunity.

The collective experience within the working group indicates that a majority of device LU sensitivity can be triggered through power pin stressing. This is not surprising since designers have many years of experience in optimizing I/O buffer guard-ring layout and computer-aided checks for appropriate implementation. Whereas power connections must go to every sub-circuit on the chip, the opportunity exists to stimulate circuit structures that have not been given the benefit of more robust layout. Therefore, additional test efficiency can be achieved by improving the traditional over-voltage power supply latch-up stress.

Success was achieved on 1.5µm technology devices when robust output or power pins were stressed using a 100nF/20Ω discharge network (see Figure 1). Collaborative efforts within the newly established ESDA working group WG-5.4 resulted in the construction of the Model BEI-790 (± 200 volts) RC Pulse Generator [6]. The waveform produced is shown in Figure 2 and was measured using a 350MHz oscilloscope.

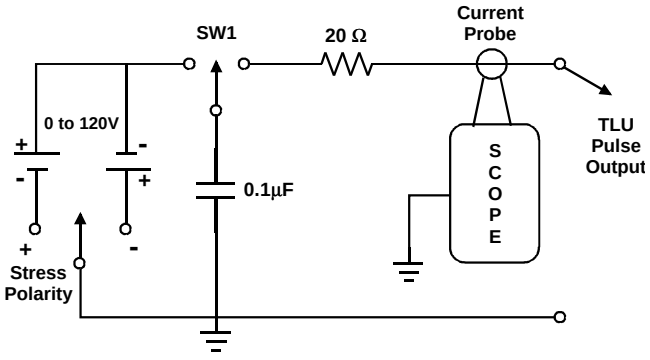

Figure 1: First generation dual-polarity TLU pulse generator

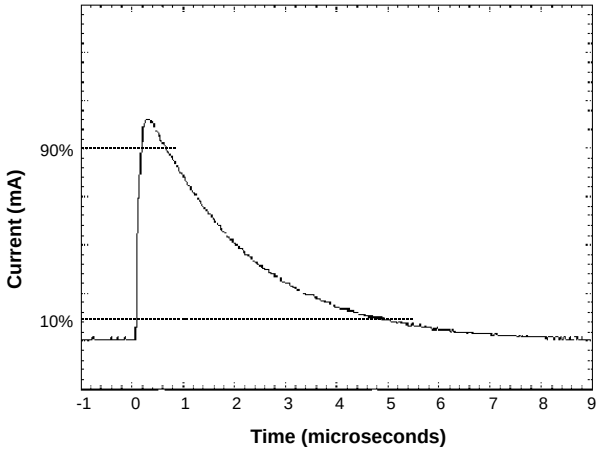

Figure 2: First generation TLU waveform

Figure 3 illustrates a typical TLU test configuration where a device-under-test (DUT) is appropriately biased while being stressed via the dual polarity TLU pulse generator. With several of the BEI-790 generators available to the working group,

specification issues such as pulse risetime, falltime, and peak current amplitude were explored. During the period from 12/95 to 9/97, these evaluations resulted in the establishment of a TLU test method [7]. It was quickly recognized that newer technologies (<1μm) were becoming less robust for pulses longer than 150ns in duration. On-chip ESD protection networks generally cannot protect against this long time-constant electrical overstress (EOS). Consequently, many devices would be thermally damaged before a latch-up threshold could be determined. The quest for a new, shorter duration transient stress was then initiated. This set-back came as a surprise to many within the working group; proving that constantly changing technology often results in the pursuit of a moving target.

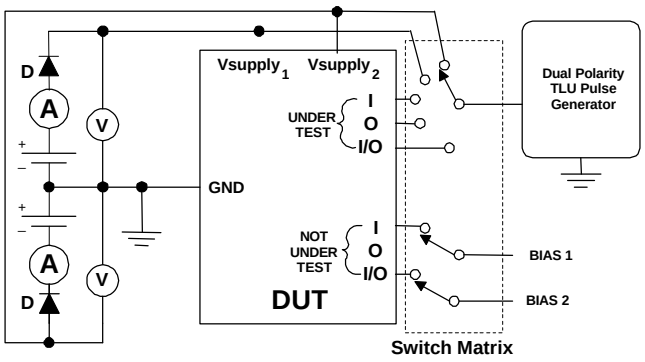

Figure 3: Typical TLU test configuration

Power Supply Response and Isolation

When latch-up occurs in integrated circuits, a low impedance path is created between the power supply and ground. Consequently, the power supply experiences an abrupt increase in device supply current and a sudden drop in voltage. Voltage supplied to the device under test (DUT) must quickly recover to near-original voltage levels to sustain the latch-up event. In addition, the voltage supply must limit the current to the DUT during latch-up to avoid excessive thermal damage.

To determine whether the power supply and connection network can meet the above requirements, a new test was developed. The Power Supply Response test (PSR) (Figure 4) allows for the measurement of recovery time due to an abrupt load change. Typical recoveries during a load change are shown in Figure 5. The acceptable power supply voltage response and recovery time (dark trace) is much faster than an unacceptable power supply response and recovery (light trace). The PSR test, performed by abruptly changing the power supply load from 510Ω to 10Ω, is accomplished by shorting out the 500Ω resistor with a very fast and bounce-free mercury (Hg) wetted relay. To measure the voltage recovery (Figure 5) and current risetime (Figure 6), a voltage probe, current transducer, and oscilloscope are used. Power supply test data shows that the voltage of an acceptable power supply must return to within 90% of its initial low current level within 500ns of the application of a load change (510Ω to 10Ω).

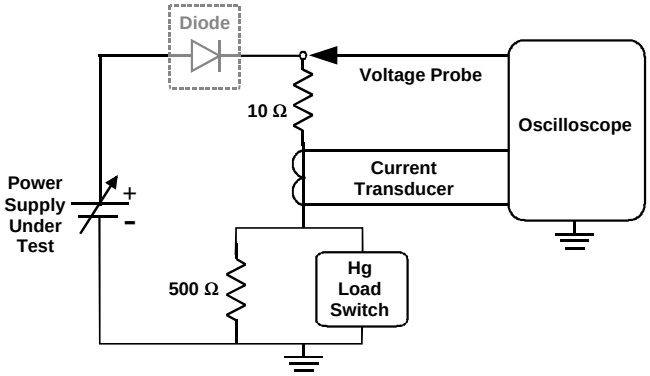

Figure 4: Power supply response test circuit

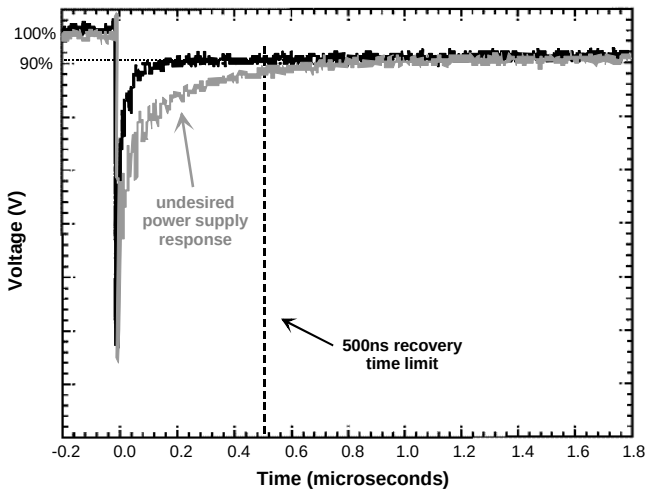

Figure 5: PSR test; desired (dark trace) and undesired (light trace) power supply voltage recovery

To ensure that most of the transient current stress is applied to the DUT and not the power supply, some isolation technique must be applied. To accomplish this isolation, a small inductor could be inserted between the power supply and the DUT; often, this could simply be the interconnect wiring. However, the use of too large an inductor would adversely affect the power supply response. A better choice for isolation is often a rectifier diode. The recovery time and reverse breakdown voltage of this diode must

match the application and may increase the time for the power supply voltage to recover. Different tests revealed that a number of available power supplies did not meet the required response to the rapid load change of 510Ω to 10Ω (see Figure 5, light trace). Test results from the ongoing PSR effort will define the requirements for a suitable TLU power supply.

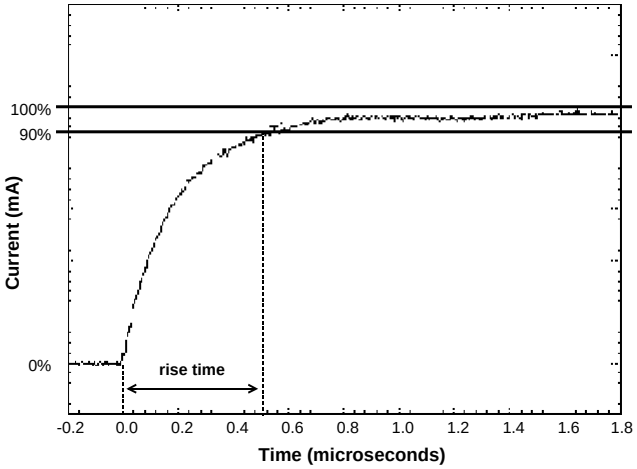

Figure 6: PSR test; power supply current response

A fast current limiting power supply was achieved by using a linear, current-limited voltage regulator. A type L200 IC was used to regulate the voltage and limit the current of an ordinary DC power supply. The power supply response test circuit configuration shown in Figure 4 was used to measure the Fast Response Power Supply (FRPS) current risetime. As shown with the dark trace in Figure 7, the change in loading produces a current step with a risetime of approximately 200ns. With the current limit of the L200 set to 300mA, the current was reduced to that level in approximately one microsecond, as shown with the light trace in Figure 7.

The best results for isolating the transient trigger source from the DUT power supply were obtained by using a type LL101 Schottky barrier diode. When this diode was measured in the reverse polarity with a transmission line pulse (TLP) test system, the diode could withstand a 65V pulse before avalanche breakdown occurs (see Figure 8). For higher stress voltages, two diodes connected in series were used. TLP testing a forward-biased LL101 diode in series with a 110Ω chip resistor produces similar results; the diode-resistor combination can be pulsed up to 70V (Figure 8). If diode D1 is reverse-bias pulsed above its breakdown level, significant current can flow into the power supply from the transient trigger source and lower the selected transient pulse amplitude. This will produce errors in TLU test susceptibility data.

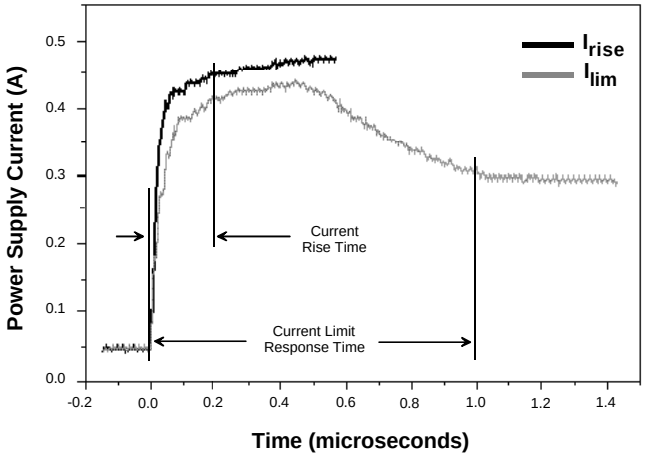

Figure 7: PSR test; transmission line (rectangular) pulse Fast Response Power Supply (FRPS)

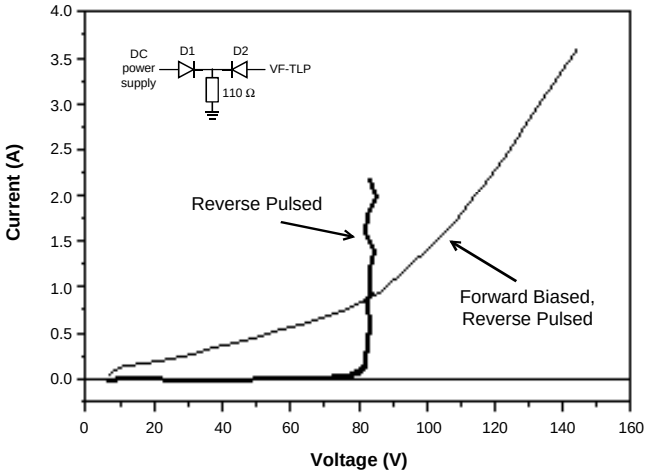

Figure 8: I-V reverse breakdown curve of a pulsed LL101 diode (D1)

Due to the short duration of the transient stimulus, a fast diode (D1) is required when using diode isolation during the TLU stress. A small signal diode, LL4148, and a power diode, 1N4005, were evaluated for this use. In both cases, sustained latch-up was not detected when transient voltages were applied to a latch-up sensitive device; even at amplitudes high enough to cause permanent EOS damage.

Manual RC Pulse TLU

After addressing the power supply response issues, the search for a more effective latch-up stimulus could resume. The first stimulus examined was a double exponential waveform. These pulses can be easily produced by charging a capacitor and subsequently

discharging that capacitor through a resistor. This RC combination dictates the falltime, or period, of the resulting pulse. With proper selection of components, a simplified waveform stress similar to those often encountered in "real-world" latch-up situations can be obtained. Since these RC pulses have a long history of use in ESD and EOS simulators, it is only natural that they be investigated for efficient latch-up initiators as well.

Latch-up susceptible devices were shared within the working group and led to the discovery that system-level HBM simulators could indeed be effectively used for latch-up stress initiation. A contract with KeyTek secured a hand-held zap gun [8] utilizing both the IEC 1000-4-2 [9] system-level HBM module and an experimental, externally selectable discharge module (limited to 1KV).

In addition to the system-level HBM pulse (see Figure 9), waveform variants resembling CDM and ferrite-suppressed HBM could be generated using the variable discharge module. The CDM-like pulse shown in Figure 10 was generated by minimizing the body components and maximizing the hand components of the HBM discharge network [10,11]. The ferrite-suppressed HBM pulse was generated by surrounding the zap gun discharge tip with appropriate ferrite toroids; effectively reducing the amplitude of the leading edge spike shown in Figure 9.

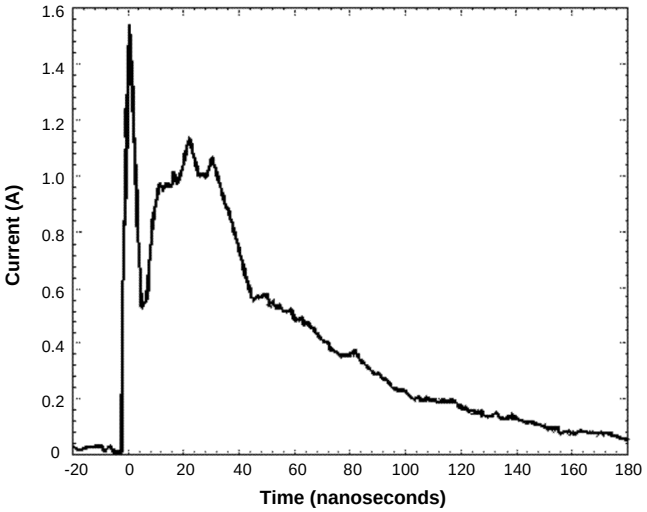

Figure 9: +500V System level HBM pulse

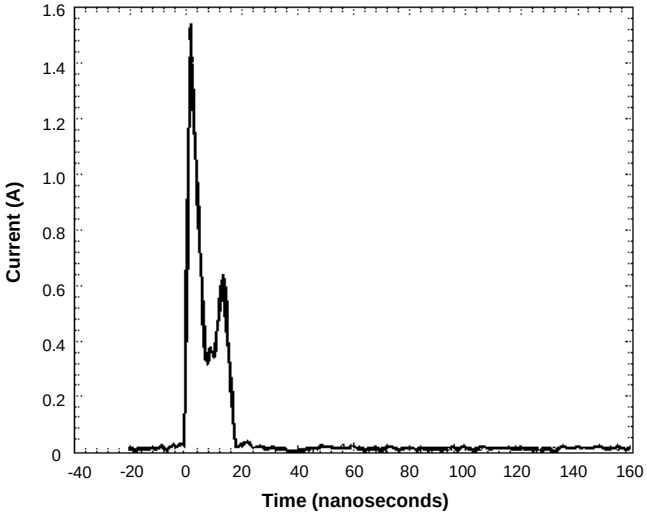

Figure 10: +500V CDM-like pulse generated using variable discharge module in hand-held gun

These new hardware configurations were then put to the test on various devices with known latch-up sensitivities (not necessarily sensitive for static latch-up). Figure 11 illustrates the typical result of a step-stress session where the stress discharge current is monitored using a Tektronix CT-1 probe and the device current is monitored using a Hall-effect probe.

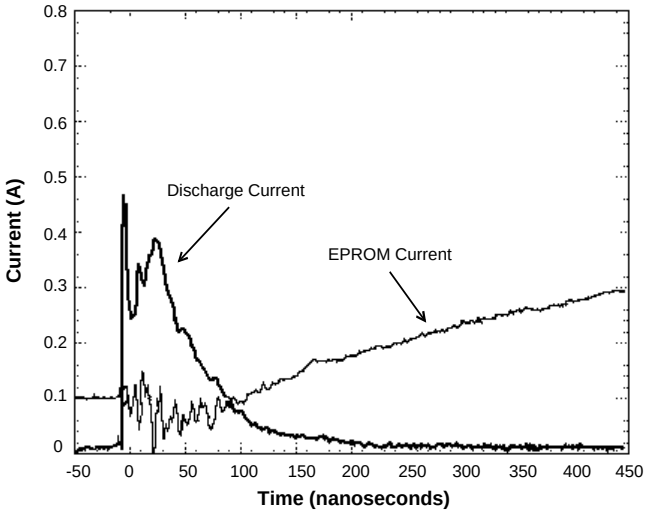

Figure 11: +150V system-level HBM pulse resulting in an EPROM latch-up failure

The lowest voltage stress able to initiate latch-up is recorded and referred to as the transient induced latch-up threshold. Table 1 compares the threshold results for different devices manufactured in 1.5µm, 0.5µm, and 0.35µm CMOS technologies. The conclusion to be drawn from this data is that quite often the CDM-like pulse does not possess enough energy to efficiently trigger latch-up. Results also show that the

ferrite-suppressed data is not significantly different from the more conveniently derived system-level HBM pulse.

Table 1: Comparison of TLU thresholds for three different manual RC TLU waveforms

Device I.D.	TLU Threshold Voltage (V)		
	IEC 1000-4-2 Pulse	Ferrite Suppressed	CDM-like Pulse
88	249V ± 21V	299V ± 27V	421V ± 20V
EPROM	< 130V	237V ± 9V	97V ± 17V
09M	880V ± 98V	853V ± 180V	> 1100V

Table 2 summarizes additional data that allows us to make the connection between latch-up (LU) risk and voltage threshold using the system-level HBM transient induced latch-up test technique.

Table 2: System-level HBM TLU data for various device codes

Device Code	**Process**	**TLU Threshold**	**Comments**
EPROM	0.6µm	+110V	Human with tweezers can easily trigger LU.
Part A	1.75µm	-250V	Weak design rules caused burn-in (melted sockets) and system LU problems.
Part G	1.75µm	+180V	
Part C	1.75µm	-300V	
2471	0.35µm	+230V	Marginal test chips with dense memory pushing spacing to limit causing LU in burn-in.
2339	0.35µm	+250V	
2435	0.35µm	+160V	
Part H Vddo	0.35µm	+450V	Sporadic (4%) burn-in LU.
Part H Vdda	0.35µm	+650V	Rare (0.2%) burn-in LU.

Observed results associate latch-up risk with system-level HBM TLU threshold ranges, as shown below:

Weak LU immunity:	0 to < 250 volts
Marginal LU immunity:	250 to < 500 volts
Robust LU immunity:	≥ 500 volts

Presently, the quest for an ideal RC TLU waveform continues, but the improvement afforded by the past efforts can be easily recognized. Frequently, marginal/sporadic latch-up resulting from worst-case conditions (such as 150°C burn-in at higher-than-nominal supply voltages) could not be recreated. We should now be encouraged by the application of a TLU technique to resolve such problems while working at room temperature. Figure 12 shows photo-emission from a 0.35µm chip that was triggered to latch at 25°C using a system-level HBM discharge to the Vdd pin (all other pins were floating). This latch-up sensitive area was directly correlated to the location experiencing occasional "internal EOS" during 150°C burn-in (see Figure 13).

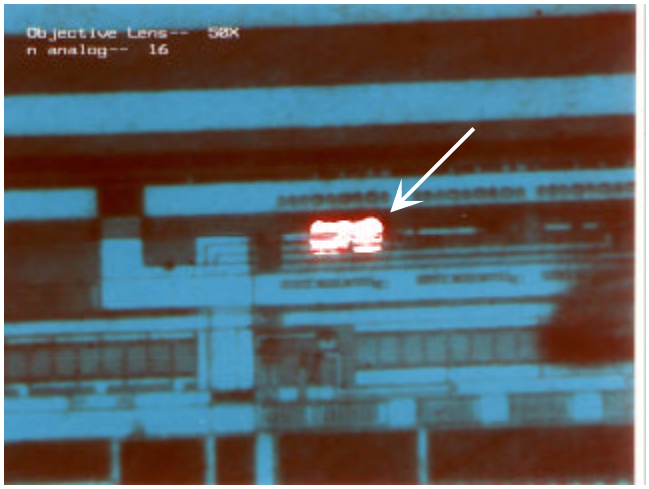

Figure 12: Photo-emission site during RC TLU latch event

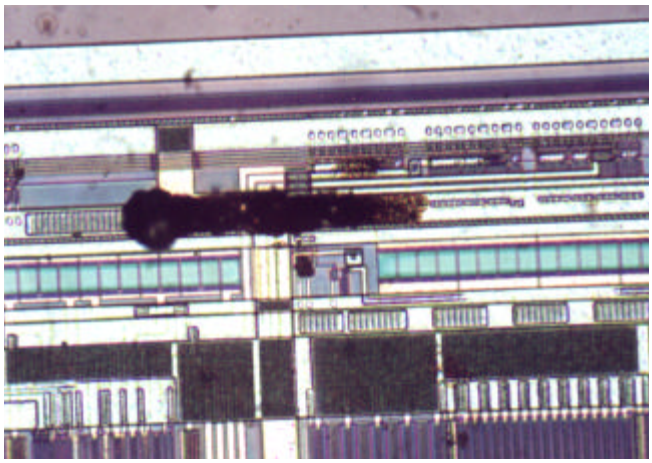

Figure 13: Optical photo of internal "EOS" after 24-hour burn-in; same location as Figure 12 emission site

Some additional refinement of the TLU stress waveform is being considered. The pulse risetime correlation to TLU voltage threshold has not been investigated sufficiently. Also, a pulse slightly longer than 120ns is being pursued so that a portion of the stress energy can escape the ESD protection circuitry. Any simplification of the present TLU waveform resulting in a more convenient waveform specification is also desirable.

Automated RC Pulse TLU

Another objective of the TLU effort was to incorporate a suitable RC pulse source and device under test (DUT) power supply into commercially available ESD/LU simulators. The DUT power supply must be able to quickly deliver the required current increase without the voltage dropping below specified levels. This is not a trivial problem to overcome in a test configuration where wire lengths can span many feet and include several layers of relay contacts. In any simulator for automated static latch-up (SLU) testing, there are three possible power supply response (PSR) set-ups [12].

Figure 14 represents the SLU PSR set-up where long wires totaling 4 to 6 feet will not affect the input pulse. These static pulses have risetimes and pulse widths in the microsecond to millisecond (slow) range. However, when the same set-up is used for transient (ns) pulses, the power supply never recovers to the specified requirements (90% of Vmax and risetime ≤ 500ns), as shown in Figure 15.

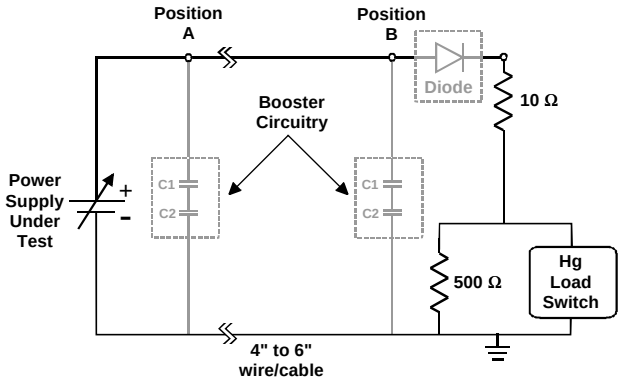

Figure 14: PSR test circuit with booster circuitry adjacent to the power supply (position A) or DUT socket board (position B)

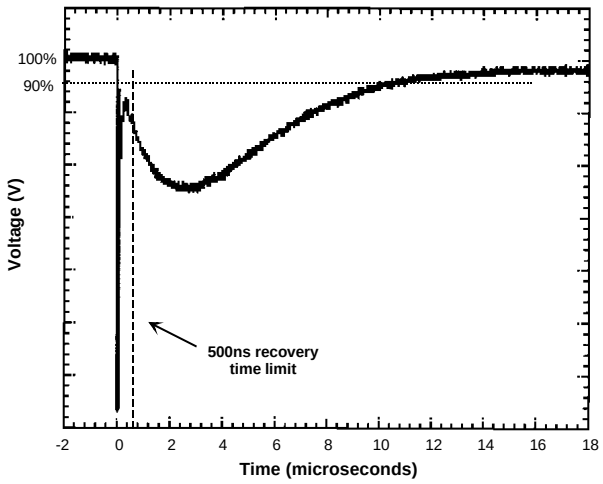

Figure 15: PSR test for automated TLU simulator without booster circuitry; note effect of internal wiring/cabling on response

In an attempt to prevent this poor response, an extra charge storage element, referred to as a "booster" circuit, was added to the SLU set-up (see Figure 14, positions A or B). As shown in position A of Figure 14, the SLU PSR set-up is used but the additional "booster" circuit (configuration of capacitors) is added adjacent to the power supply circuit. The power supply had better response (see Figure 16), but the recovery still occurred outside the specified requirements.

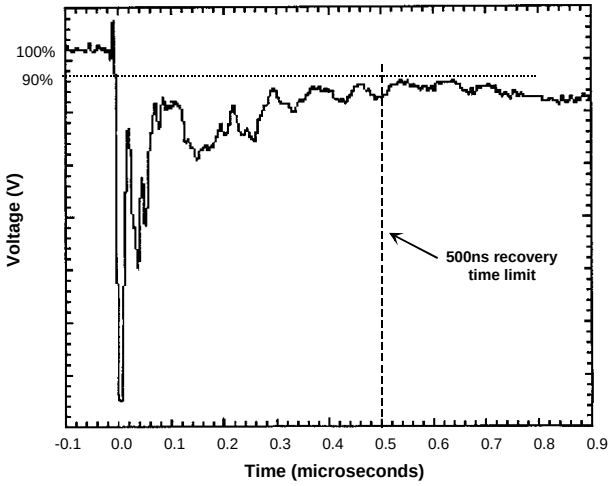

Figure 16: PSR test with booster circuitry located adjacent to the power supply (position A)

As shown in position B of Figure 14, the SLU PSR set-up is again used but the additional "booster" circuit is added next to the DUT socket board. The wire length between the "booster circuitry" and the socket board is less than 6 inches and effectively brings the response to within the specified requirements (see Figure 17).

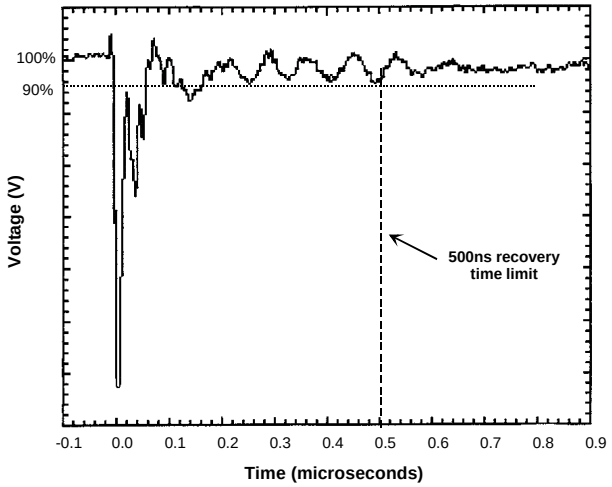

Figure 17: PSR test with booster circuitry located adjacent to the DUT socket board (position B)

There is one drawback. The power supply response for an automated TLU simulator (without booster circuitry) does not meet specified requirements, as shown in Figure 15. The addition of an isolation diode, as discussed in the earlier section on power supply response and isolation, actually degrades the power supply response further (see Figure 18).

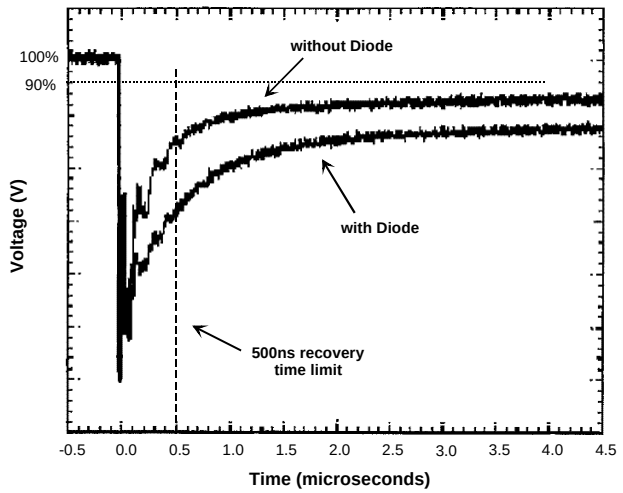

Figure 18: PSR test with and without isolation diode (no booster circuitry)

Clearly, the addition of the diode prohibits the power supply voltage/current into the DUT from being maintained while device power pins are stressed. Consequently, the setup may not sustain a latch-up event. Since the introduction of the isolation diode produces a predictable voltage drop, appropriate compensation may alleviate the situation. The use of an active voltage regulator positioned near the DUT has also been shown to work effectively. Alternative equipment architectures providing an additional layer of relays near the DUT to provide DUT power may provide another solution to the encountered response problem. The efforts are continuing.

Rectangular Pulse TLU

Rectangular pulses from transmission line pulsers are of particular interest for transient induced latch-up. They have been well established for the analysis of ESD-protection structures [13,14].

The configuration used for Transient Latch-Up (TLU) induced by Very Fast transmission Line Pulses (VF-TLP) is shown in Figure 19. It consists of three main parts: the fast response power supply, the test fixture for the DUT, and the pulse generator (VF-TLP).

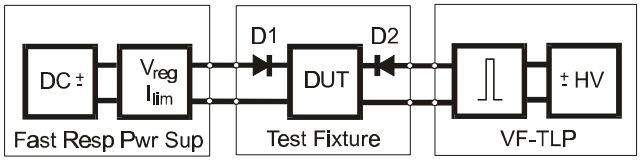

Figure 19: Test configuration for VF-TLP transient latch-up

The Very Fast Transmission Line Pulser (VF-TLP) generates 10ns, 5ns, and 3.5ns wide pulses with risetimes less than 500ps [15]. An incident voltage pulse of short duration, defined by the length of a transmission line, travels from the pulse generator to the DUT where it is reflected. The current transmitted into the tested DUT-pin and the voltage across the tested DUT-pin are calculated using the incident and reflected voltage pulses according to the following:

$$V_{trans} = V_{dut} = V_{incid} + V_{refl} \quad \text{[Formula 1]}$$

$$I_{trans} = I_{dut} = I_{incid} + I_{refl}$$

$$V_{incid} = (Z_o)(I_{incid})$$

$$V_{refl} = -(Z_o)(I_{refl})$$

$$I_{trans} = I_{dut} = (V_{incid}-V_{refl})/Z_o \quad \text{[Formula 2]}$$

This time domain reflectometry provides in-situ insight for the current and voltage at the DUT.

In order to connect the fast response power supply and the VF-TLP to the pins of a tested device, a special DUT-test fixture was developed using 50Ω micro-strip lines. Additionally, two decoupling diodes are necessary (see Figure 8). D1 isolates the power supply from the pulse source and D2 prevents the DC-current of the power supply from flowing through the VF-TLP on power up of the DUT. Both devices are fast switching Schottky barrier diodes (LL101). For pulses greater than the breakdown voltage of D1, a significant amount of current flows into the power supply leading to incorrect measured values of DUT current. This should be avoided.

The fast response power supply quickly (~2.5µs) limits the current to a safe, preset value once the trigger pulse has forced the device to enter the low resistance latch-up state. To perform the test, a controlled power supply voltage is applied to the DUT via D1. The stress pulse is injected into the DUT through the low-parasitic 50Ω path containing D2. Untested input pins are grounded, while untested bi-directional/output pins are floating. After applying the VF-TLP, latch-up has occurred when the compliance current of the power supply is permanently reached. Typical measurement results for the voltage and current transients at the tested DUT pin are represented in Figure 20 using Formulas 1 and 2.

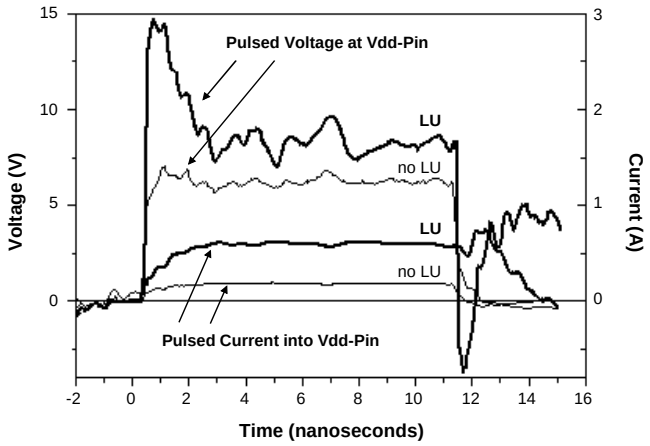

Figure 20: Pulsed voltage and current at DUT pin under test

The VF-TLP method was used to characterize the TLU-sensitivity of different device pins. All devices were known to be latch-up sensitive in the field. However, all devices had previously passed qualification tests, including static latch-up testing at room temperature. For all tested pins, it was possible to induce latch-up using VF-TLP.

The minimum VF-TLP pulse amplitude that triggers latch-up is a clear measure of device latch-up susceptibility. However, this minimum voltage also varies with the pulse width – wider pulses yield lower threshold voltages. Therefore, any TLU standard must specify a particular pulse width to be used.

Some of the tested devices exhibited a "window effect" [16]. These windows are discontinuities where latch-up may not always be observed in a predictable fashion at levels above the threshold voltage. These windows also appear to be pulse width dependent. This phenomenon is not well understood and continues to be investigated. Overall, VF-TLP promises to be a well-controlled, repeatable method of delivering fast risetime pulses to biased devices to assess latch-up susceptibility.

Combination Rectangular Pulse TLU

Another variation of the charged transmission line pulsing (TLP) methodology is the combination pulse. This configuration generates two rectangular wave pulses in succession. The basic concept is to apply an initial short duration and high voltage amplitude "impulse" to trigger latch-up. This is immediately followed by a second longer duration and lower voltage amplitude "impulse" to sustain latch-up after it occurs.

The combination rectangular square wave pulse is generated by using a Barth Electronics Model 732 pulse generator to produce a 50ps risetime pulse with a time duration that can be varied from 1ns to >100ns. Varying the pulse width requires changing the length of the transmission line that is charged and discharged to form the pulse. This pulse is split into two different paths, where each new pulse is altered to meet the desired shape or amplitude (see Figure 21). The two altered pulses are then combined to form the combination pulse (see Figure 22).

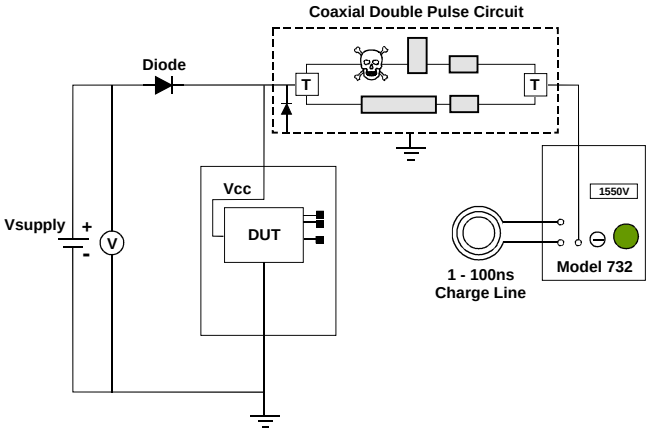

Figure 21: Combination rectangular pulse test configuration

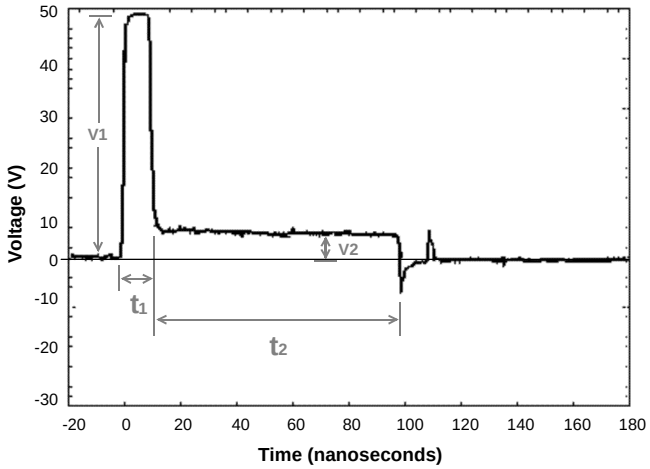

Figure 22: Combination rectangular pulse

After the initial pulse is split into two separate pulses, the first pulse path forms the short duration and high amplitude voltage pulse (t1 and V1 shown in Figure 22). This path uses a pair of shorted transmission lines directly connected across the 50Ω coaxial cable path. The shorted 50Ω lines are of equal length and chop the pulse to zero amplitude after it exits the coaxial cable.

The length of the pulse before it drops to zero is determined by the two way travel time of the shorted

coaxial cables. This type of pulse chopping circuit is known as a "suicide cross", which is inherently very reflective. To correct this, an attenuator is used to minimize the reflections that would otherwise distort the pulse shape. Since current continues to flow through the shorted cables, an opposite polarity pulse is produced at the end of the initial longer pulse. A fast recovery diode is placed at the output of the combiner to clip the negative pulse that occurs at the end of the combination pulse. Without clipping the negative polarity pulse, the device under test (DUT) could be driven out of latch-up almost as fast as the initial, positive pulse drives it into latch-up.

The second path is used to form a longer duration and lower amplitude secondary pulse (t2 and V2 shown in Figure 22) that is intended to maintain latch-up after it is initially triggered. A step attenuator is used to reduce the amplitude of the pulse over a range from near 0V to about 10V. This path does not change the original generated pulse length. After the initial pulse is split, the two "new" pulses are combined to form a composite pulse. Matched risetime filters can be placed before or after the initial split to slow the risetime of the initial pulse and determine its effect on the voltage level required to induce latch-up.

Initial tests using this combination rectangular pulse on 0.8µm CMOS EPROM 32 pin DIP devices (JEDEC 17 qualified) induced latch-up when the Vcc pin was pulsed (see Figure 23). More tests are planned to develop a matrix of specific risetime, width, and amplitude values for the initial pulse. Further investigation of the amplitude and length for the secondary pulse will determine the levels that can provide the highest sensitivity to TLU for the greatest number of devices.

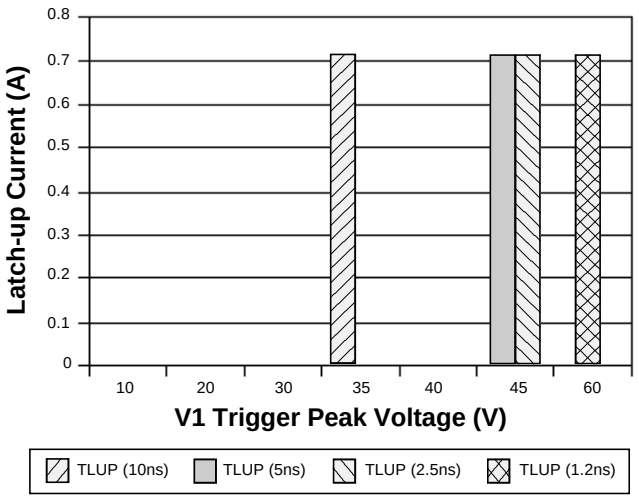

Figure 23: Relationship between initial impulse duration (t1) and amplitude (V1)

Bi-polar Stress TLU

Working group WG-5.4 activity using the BEI-790 TLU pulse generator [6] resulted in the discovery of a very unique latch-up (LU) test methodology. An under-damped bi-polar waveform is derived from the model 790 output, taken before the resistor of the 100nF/20Ω source (see Figure 1). The resulting waveform, as shown in Figure 24, is a low voltage, decaying sinusoid similar in shape to Machine Model but with much lower frequency (~500KHz).

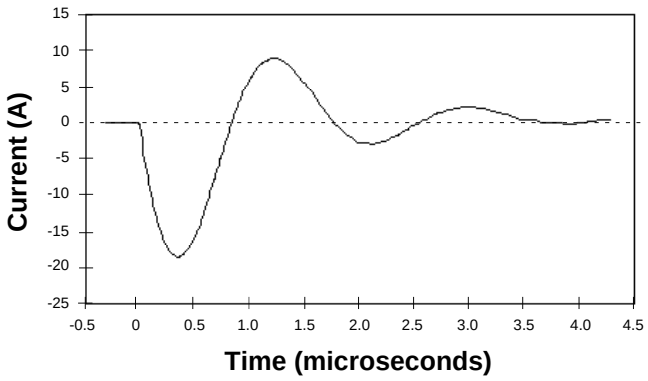

Figure 24: Bi-polar stress TLU waveform

In older static latch-up (SLU) methodologies, power pins are typically raised above the absolute maximum level (maximum allowable voltage applied to the power pin in a non-operating state) to insure LU does not occur due to channel hot carriers, punch-through, SCR triggering, or breakdown. However, negative voltage levels were not normally applied to power pins. In fact, the negative stressing of a positive-biased power pin (e.g., Vdd, Vcc, etc.), where thousands of N-Well/P-Well junctions in parallel would be forward-biased, was considered useless. In reality, these forward-biased N-Well junctions inject minority carriers (electrons) into the P-Well/P-Substrate as the potential of Vdd is pulled below ground. When the Vdd potential returns to a positive value, the N-Well now collects the minority carriers and creates the voltage drop across the N-Well sheet resistance that may trigger latch-up. This sequence creates a unique case where the same structure (N-Well) serves as both emitter and collector for charge carriers. As noted in the background section of this paper, many WG-5.4 members observed that most field returns (and occasional burn-in failures) exhibited a LU site and corresponding EOS damage within the die core, not at the I/O pins [5]. Since power busses travel throughout the die, all sub-circuits can be efficiently evaluated for LU using this new technique.

It has been previously shown [17] that sub-micron product appears most susceptible to a negative-going bi-polar transient and that some critical rate of polarity reversal is important. This effort was primarily concerned with complex high pin count product and focused on Vcc excitation driven by several concerns:

1. Significant software was required to place devices in an initial controlled state.
2. Transients applied to Vcc directly enter the die core, *for which there is no LU protection.*
3. Prevent damage to sensitive and expensive I/O pin drivers in ATE and vector testers.

A formal experiment [18] to validate the usefulness of the improved trigger was conducted using three generations of product with varying levels of real world sensitivities, as determined by field return data. Product was operated using an IMS ATS vector test system with an externally controlled HP power supply. All devices used N-Well CMOS technology and passed static latch-up (SLU) testing at temperature (125°C). Devices were stressed during both static and dynamic operation as follows:

- STATIC: All Inputs (including clock) held at ground with I/O pins floating.
- DYNAMIC: Clock and Inputs stimulated using a 20MHz "AND" pattern to create high I/O switching.

Table 3 shows that bi-polar withstand voltage levels scale well with field return data, indicating the bi-polar trigger promises discrimination of "good" and

Table 3: Bi-polar latch-up threshold voltage levels

Operating Condition	**LU Results & Observations**
Generation 1: Weak, Many Field Returns	
Static	-30V LU, robust on positive Volts (damage before LU)
Dynamic	-30V LU, robust for positive volts (damage before LU)
Generation 2: Few Returns - Revised version, Improved Core Layout	
Static	-60V LU, robust for positive volts (damage before LU)
Dynamic	-40V LU, robust for positive volts (damage before LU)
Generation 3: Zero Returns For LU, New Scaled Process	
Static	NO LU, permanent EOS damage at -120V
Dynamic	NO LU, permanent EOS damage at -120V

This improved negative bi-polar LU test methodology has been found applicable to a wide range of products (complexity approaching 512 pins) and technologies ranging from 1.0µm dual-metal to 0.25µm 5-metal. The bi-polar stimulus is believed to indicate susceptibility such that real world performance can be predicted. For dynamic device operation, stressing can be conducted under "near-real" operating conditions. Work is now focused on incorporating the bi-polar stress methodology into an automated simulator with an adequate power supply.

Summary

This effort identified several transient pulses suitable for efficiently triggering CMOS latch-up in integrated circuits. The different stimuli were compared for effectiveness in creating latch-up and several problematic issues were identified. A number of test system power supplies were found to have inadequate response to, and recovery from, rapid load changes associated with a latch event. Various double exponential RC transient stimuli ranging from short CDM-like discharges to longer EOS producing pulses were evaluated. While most stimuli were able to create a latch event in devices passing static latch-up requirements, they were not equally effective.

Although some differences exist within the working group, a consensus was reached in several areas. Foremost is the recognition that transient stresses are better stimuli for latch-up than static stresses. Another universal realization is that latch-up sensitivity assessment is a race between EOS and LU and therefore minimizing incident energy while maximizing injected current density is required.

Group members have also witnessed successful attempts to utilize LU stress waveforms derived from RC networks and charged transmission lines. Each technique has strengths and weaknesses. RC pulses are easily formed but more difficult to maintain. Transmission line pulses are more controlled and portable but require more finesse in composition and use. The polarity reversal of the bi-polar trigger can determine TLU susceptibility while minimizing risk of ESD damage. One perception that is shared by most but not all group members is the recognition that improved stressing of power pins can greatly improve LU test efficiency.

The TLU effort is ongoing with the ultimate goal of developing an alternative test method for assessing latch-up robustness and practical implementation in commercial test systems. The working group

constantly solicits information regarding latch-up experiences from the industry and has a survey on the ESDA website (**www.eosesd.org**) for those who are interested or feel they have information to contribute.

Acknowledgments

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