

New Latchup Mechanism in Complementary Bipolar Power ICs Triggered by Backside Die Attach Glue

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Abstract

It is shown that in complementary bipolar power ICs latchup can be caused by a thyristor formed by the V-PNP power transistor at the frontside of the die and a Ag-filled glue die attach at the backside of the die (used to provide a good thermal contact between the die and the Cu-heatsink). The thyristor is triggered by saturation of the V-PNP power transistors or by forward biasing the backside diode between Ag-filled glue and p-type silicon. The effect is strongly temperature dependent. It can be eliminated by either leaving the backside floating or by applying backside metallization. Consequences for latchup qualification testing are discussed.

1. Introduction

Latchup [1] is a known reliability risk in complementary bipolar power processes (featuring both vertical-PNP and vertical-NPN power transistors) as thyristors are intrinsically present in these technologies, see fig. 1 and 2. Furthermore complementary bipolar processes are more susceptible to latchup than CMOS processes as the presence of n- and p-type buried layers prevents the use of p⁻epi/p⁺⁺ low ohmic ($\approx 0.01 \Omega\text{cm}$) bulk epitaxial substrates. The thyristors are located at the frontside (top side) of the die, see fig. 1 and 2, and can be triggered by currents injected by both external spikes as well as by saturation of internal bipolar transistors. Note that in harsh automotive application environments these injection currents can be well over 1 A. Generally many design and layout measures are taken to prevent latchup from occurring like the use of guardrings, limitation of bipolar transistor saturation currents and by grounding the substrate as good as possible. Because of the above, latch-up testing is a routine part of product qualification programs for complementary bipolar power ICs as e.g. required by the Automotive Electronic Council (AEC).

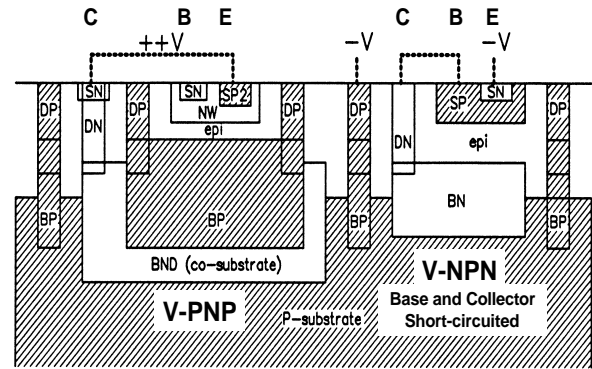


Fig. 1: Schematic view of a cross section of the complementary bipolar IC showing the V-PNP and V-NPN transistor.

Bipolar power ICs are often packaged in Single-In-Line (SIL) power packages where the low-doped p⁻substrate is attached to a copper (Cu)-heatsink by a silver (Ag)-filled epoxy glue to achieve low thermal resistance values. In the application the Cu heatsink is generally contacted to the ground potential (just as the p⁻ substrate).

The ICs are subsequently packaged in a SIL-power package. Here the p⁻ substrate backside is attached to a Cu-heatsink by an epoxy glue containing Ag-fillers to achieve low thermal resistance values, see fig. 3 and 5.

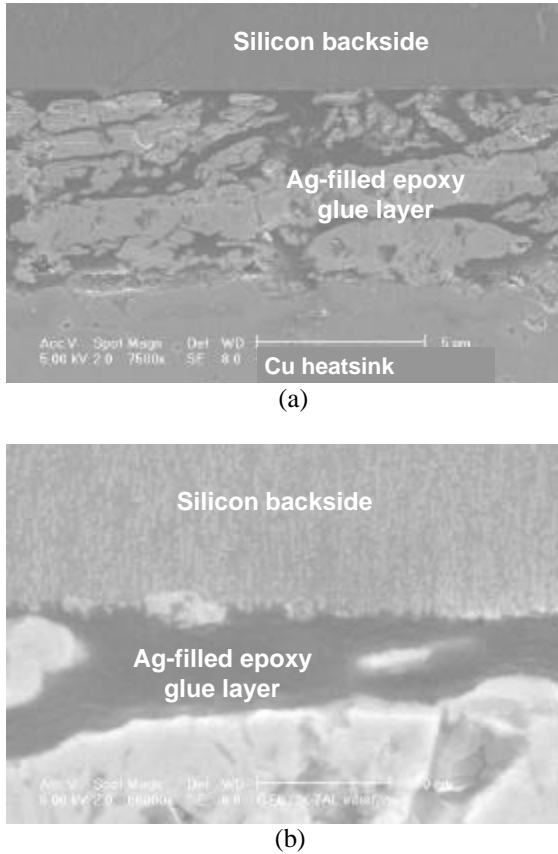


Fig. 5: SEM cross section showing a) the backside of the die, the 6 μ m thick silver filled epoxy glue layer and the copper heatsink and b) in more detail the backside die - epoxy glue interface.

Unfortunately, it appears that this packaging method results in the formation of a diode between the n-type Ag-filled epoxy glue layer and the low doped p⁻ substrate, see fig. 4 and 6. Note that diode does not behave like a real Ag-Si Schottky diode. Fig. 6 shows that the diode forward voltage is >0.7V. Given the barrier height for an Ag to p-type silicon metal-semiconductor contact of 0.54 eV at 23°C [2], a good Ag-Si(p-type) Schottky diode should exhibit a much lower forward voltage than observed here. Furthermore, we find that the n-type

Ag-filled glue layer also can act as the emitter of a parasitic NPN transistor (T4 in fig. 4) between the frontside and backside of the die where the the p⁻ substrate acts as the base and the deep buried-N (BND) isolation of the V-PNP transistor as collector, see fig. 4. Fig. 6 shows the bipolar gain of this transistor as a function of the emitter current for a small test structure. Despite the very thick base ($\approx 375 \mu\text{m}$), the NPN gain h_{fe} ranges from 10^{-4} to 10^{-2} at 25°C. Note that the h_{fe} scales with the collector area; in real circuits h_{fe} values up to 0.5 have been observed. Note that both the diode and the NPN characteristics are not well controlled as these are influenced by many parameters as e.g. the surface roughness of the backside of the silicon die, the thickness of native oxide layers on the silicon backside, the electron minority carrier lifetime in the p⁻ substrate, the thickness of the epoxy glue, the distribution and concentration of Ag-fillers in the epoxy glue. As a result, a large spread is observed in both the diode I(V) curves, see fig. 6, as well as the NPN current gain (h_{fe}) characteristics, see fig. 7, depending on the specific process flow. The fact that the NPN gain in fig. 7 increases with injected current is characteristic for metal-semiconductor junctions where the ratio of minority injection (electrons in this case) increases with current due to the enhancement of the drift-field component, which becomes much larger than the diffusion current [2].

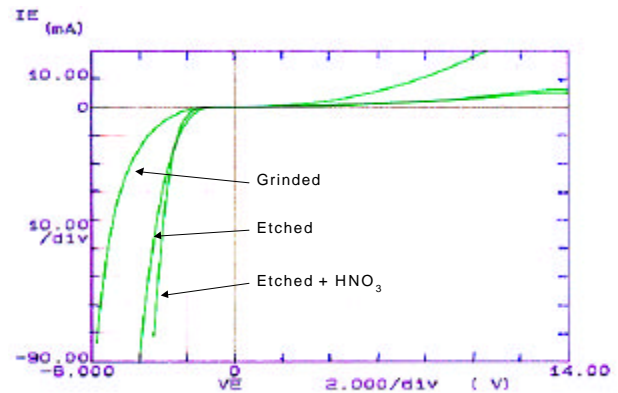


Fig. 6: I(V) characteristics at 25°C of the backside diode formed by the Ag-filled epoxy glue layer and the low doped p⁻-substrate for three different treatments of the backside of the wafer, a) grinded backside, b) wet etched backside and c) as b) but with an HNO₃ treatment resulting in a thicker native oxide layer on the wafer backside.

As shown in fig. 4, the parasitic NPN transistor T4 forms in combination with the V-PNP transistor T1 a thyristor between the frontside and the backside of the die. As the parasitic V-PNP has high gain, the thyristor loop gain is larger than 1 and thus latchup can occur.

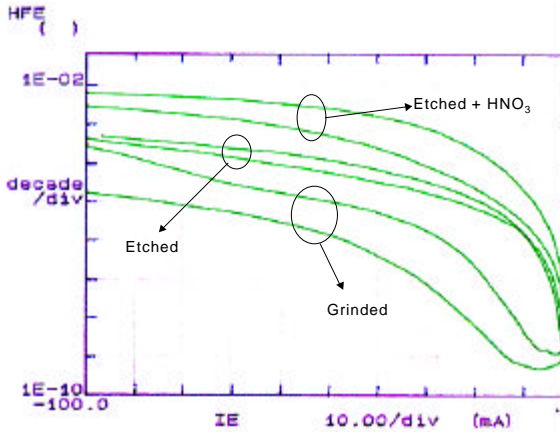


Fig. 7: Gain of the parasitic NPN transistor formed by the Ag-filled epoxy glue layer at the backside (emitter), p⁻ substrate (base) and BND-layer at the frontside (collector) as a function of the backside emitter current for the same treatments of the wafer backside as in fig. 6 ($V_{\text{base}}=0\text{V}$, $V_{\text{collector}}=-5\text{V}$, $T=25^\circ\text{C}$).

3. Latchup trigger mechanism

3.1 Backside current injection

One way to trigger the thyristor is by forcing the Cu-heatsink to a negative voltage and thus forward biasing the backside diode T4 and injecting electrons into the substrate. In table 1 typical trigger currents are shown for a typical product in this technology.

3.2 Saturation of V-PNP transistors

In a real automotive application, the thyristor can be triggered by severe saturation of the V-PNP power transistors. This occurs regularly during e.g. an engine start event of a car where the supply voltage can drop as low as 6V. In this case a large hole current is injected into the low doped p⁻-substrate resulting in a significant lifting of the substrate potential. Consequently, the backside diode T4 is forward

biased and electrons are injected into the substrate and collected by the BND-layer, see fig. 3 and 4. This causes a voltage drop across R_{BND} which forces parasitic PNP transistor T3 to switch on. A current now flows from the emitter of the V-PNP power transistor T1 to the substrate via T3, causing a voltage drop across R_{sub} . When this voltage exceeds the forward voltage of the backside diode, the parasitic NPN transistor T4 may remain conducting even when the V-PNP saturation event is over. Parasitic NPN transistor T2 then starts to operate in reverse and as a result the collector current of T4 will start to drive transistor T1 and a thyristor is being build-up.

Backside treatment	Die attach	H_{fe} NPN T4	Backside latchup trigger current
Etched	Ag-filled epoxy	$0.8 \cdot 10^{-3}$	120 mA
Etched+ HNO3	Ag-filled epoxy	$3 \cdot 7 \cdot 10^{-3}$	60 mA
Grinded	Ag-filled epoxy	0.3- $3 \cdot 10^{-3}$	130 mA
Etched	Ti/Ni/Ag backside metallization	$3 \cdot 10^{-6}$	>3 A

Table 1: Gain of the parasitic NPN T4 and latchup trigger current at 25°C for a typical product in case of injection from the backside diode for various treatments of the wafer backside as in fig. 6 and for various die attach materials.

The thyristor turns-on when the injected electron current from the backside diode I_{backside} exceeds a certain trigger value I_{trig} while the back-tab is at 0V. The effect is strongly temperature dependent, see fig. 8, as both the saturation current of the V-PNP power transistors and the substrate resistivity increase with temperature resulting in an increased substrate potential lifting. In combination with the drop in backside diode forward voltage with temperature, this results in a strong increase of the current I_{backside} injected by the backside diode. When it exceeds the latchup trigger current I_{trig} latchup will occur. Note that I_{trig} decreases with temperature due to the increase of the gain of the bipolars and the drop of diode forward voltages with temperature. Fig. 8 shows that for our typical product latchup will occur for $T > 105^\circ$.

4. Elimination of the backside triggered latchup mechanism

There exist several possibilities to prevent the above described latchup mechanism. The first is to disconnect the Cu-heatsink from the ground potential thereby forcing the emitter of T4 to be floating. This can be achieved by either leaving the external heatsink to which the Cu-heatsink is attached floating or by placing a thin electrically isolating sheet between them. This is a very robust solution but care must be taken not to deteriorate the thermal impedance characteristics. The second is to use an isolating epoxy glue instead of a glue containing Ag-fillers.

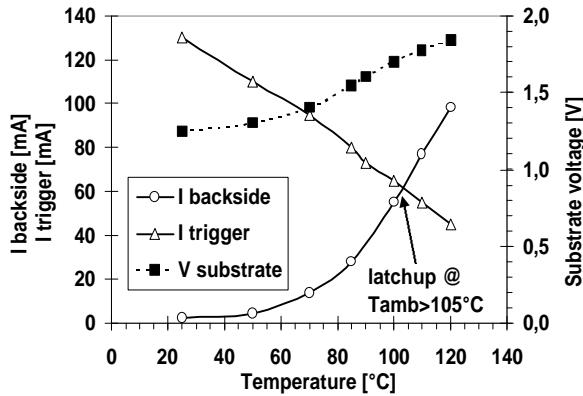
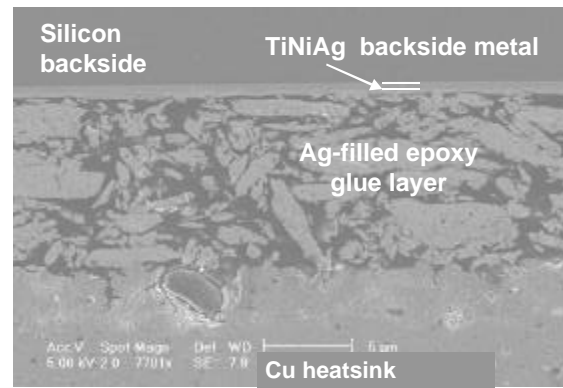


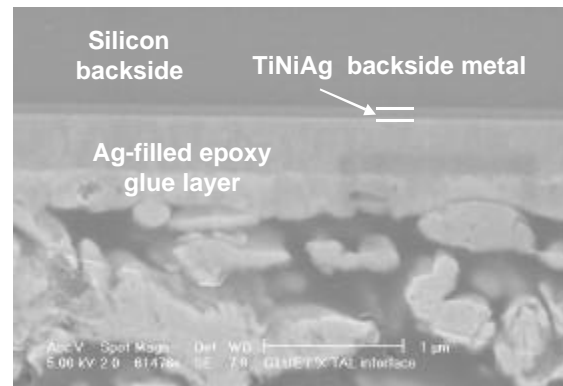
Fig. 8: Backside injection related latchup trigger current I_{trig} (triangles), substrate potential lifting (squares) and resulting backside diode injection current I_{backside} (crosses) as a function of temperature for the case of a typical product during a V-PNP saturation event at $V_{\text{supply}} = 7\text{V}$; at $T > 105^\circ\text{C}$ current $I_{\text{backside}} > I_{\text{trig}}$ and latchup will occur.

Again thermal impedance characteristics will determine the feasibility of this solution. The third option is to lower the resistivity of the p⁻ substrate, thereby reducing both the substrate potential lifting in case of saturation as well as the bipolar gain of the parasitic NPN transistor T4. If the loop gains remains < 1 no latchup will occur. It is however difficult to prove that this a 100% robust solution up to 150°C for all designs at all application conditions. The final solution is to apply a Ti-Ni-Ag backside metallization to the low doped p-type wafer backside, see fig. 9. The Ti-Si interface forms a kind of a Schottky diode with a barrier height of 0.61 eV

[2]. The corresponding $I(V)$ characteristics are shown in fig. 10 and it can be clearly seen that the diode forward voltage is reduced to about 0.3V . Furthermore, as the Schottky diode is a majority carrier device [2], the TiNiAg backside metallization decreases the bipolar gain of the parasitic NPN transistor T4 by more than a factor 100, see table 1. This is probably caused by a strongly reduced emitter efficiency in the case of the backside metal. As a result, the thyristor loop gain is effectively reduced to much lower than 1 thus preventing the occurrence of latchup. Furthermore the backside metallization also strongly reduces the substrate resistance R_{sub} . Table 1 shows indeed that no latchup is observed up to backside injection currents exceeding 3A .



(a)



(b)

Fig. 9: SEM cross section showing a) the backside of the die, the 100nm thick TiNiAg backside metallization, the $10\mu\text{m}$ thick silver filled epoxy glue layer and the copper heatsink and b) in more detail the backside die - TiNiAg interface.

5. Impact on latchup qualification testing

Our results clearly suggest that a number of improvements are required for the latchup test procedure of (medium) power ICs. Firstly we recommend that during the standard latchup test procedure the backside of the die (or any leadfinger that makes electrical contact to the diepad as in the case of certain medium power packages) must be contacted to ground potential. Secondly we recommend also a measurement of the latchup trigger current while injecting from the backside diode at maximum application temperature. The trigger current pass/fail criteria for this case are subject of discussion but probably should be $>500\text{mA}$.

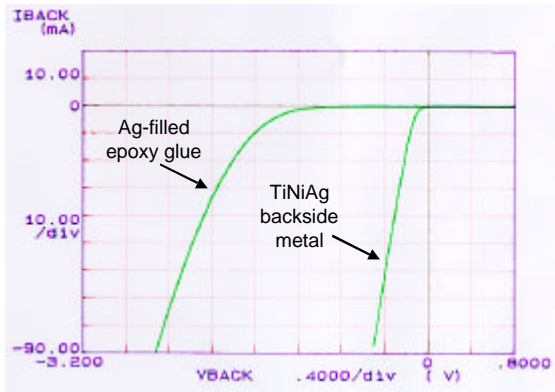


Fig. 10: I(V) characteristics at 25°C of the backside diode formed by a) the TiNiAg backside metal and the low doped p⁻substrate and b) the Ag-filled epoxy glue layer and the low doped p⁻substrate. In both cases the backside was wet etched.

6. Conclusions

A new latchup failure mechanism in complementary bipolar power ICs has been described. Latchup is caused by a thyristor constituted by the V-PNP power transistor at the frontside of the die and a parasitic NPN transistor between the frontside and the backside of the die. The emitter of this NPN transistor is formed by the Ag fillers in the die attach glue at the backside of the die, its base by the p⁻ substrate and its collector by the n-type BND isolation of the V-PNP transistor. The thyristor is triggered by saturation of the V-PNP power transistors or by forward biasing the backside diode between Ag-filled glue and p-type silicon. The effect is strongly tempe-

rature dependent. It can be eliminated by either leaving the backside floating, thus eliminating the parasitic NPN, or by applying backside metallization which strongly reduces the bipolar gain of the parasitic NPN.

Consequences for latchup qualification testing are that during the standard latchup test procedure the backside of the die (or any leadfinger that makes electrical contact to the diepad as in the case of certain medium power packages) must be contacted to ground potential. This is currently not prescribed in the existing latchup test specifications. Furthermore it would make sense to an additional test where the latchup trigger current is measured while injecting from the backside diode (all at maximum application temperature).

7. References

- [1] R.R. Troutman, 'Latchup in CMOS technology', Kluwer Academic Publishers, Boston, (1986)
- [2] S.M. Sze, 'Physics of Semiconductor devices', 2nd edition, John Wiley & Sons, New York, (1981)