ISTFA '93: The 19th International Symposium for Testing & Failure Analysis, Los Angeles, California, USA / 15-19 November 1993

Electro-Thermally Induced Parasitic Gate Leakage (GL)

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Abstract

The combination of new operational environments, assembly processes, new circuit designs, and the sophistication of encapsulation materials presents new opportunities for previously unknown failure modes. Electro-Thermally Induced Parasitic Gate Leakage (ETIP-GL or GL) is an environment and materials induced failure mechanism that adversely affects the performance and reliability of an integrated circuit. GL is a trapped-charge phenomenon found in plastic encapsulated Bi-Polar/I²L and Complimentary Metal-Oxide Semiconductor (CMOS) micro-circuit technologies. The effects of GL (degraded parametric and functional failures) can always be reversed by a high temperature unbiased bake. GL is similar to other trapped charge and other mobile ion phenomena in that it occurs at elevated temperatures in the presence of an electrical field or static charge. Circuit sensitivity is affected by circuit/chip design, physical layout/geometry, the fabrication process, and the electrical characteristics of the encapsulation material. The author has evaluated a variety of integrated circuit technologies, designs, and encapsulation materials and developed a method to analyze and characterize the effects of and sensitivity to GL. It has been determined that a micro-circuit's sensitivity to GL can almost be eliminated by the addition of a third layer metal grid during the die fabrication process or by extending the post mold cure time.

ELECTRO-THERMALLY INDUCED PARASITIC GATE LEAKAGE (GL) occurs at factory test sites which utilize high temperature handlers and high temperature assembly operations (i.e., ATE electrical testing, part level burn-in and infra-red reflow solder operations). Failed parts recover and become fully functional when exposed to an unbiased high temperature-oven bake, during de-soldering operations, or when the part was decapped and the die was exposed to normal levels of light. It has been determined that the failures were the result of a trapped charge phenomenon which resulted in a degradation of input pin impedance and subsequent logic failures. Improvements were made in process and handler grounding and the number of failures was reduced. The mechanism of failure was identified. A method to comparatively evaluate the interactive affects of the circuit design and assembly process was developed and alternative solutions are suggested.

The GL phenomenon was first identified in a dual metal, bi-polar, 52 pin, quad-packaged surface mount part. The failure occurred during hot testing in the form of an out of specification measurement which returned to normal when the parts were subjected to a high temperature bake or were opened for failure analysis. A procedure was developed to open the part in total darkness and the site of failure was determined by systematically stepping a 20 micro-meter spot of light over the die until the failure site was illuminated and the defect was cured. [1]

The cause of failure was found to be a forward biased enhancement mode parasitic FET with an accumulated charge in a floating epi pocket apparently providing a gate electric field. The failure occurred when a charge accumulated in the topside nitride passivation and became large enough to invert the n-epi surface. A very small negative charge at the die surface is known to invert the epi layer. The nitride interdielectric, residual hydrogen introduced during deposition, and a floating epi pocket with light doping were suspected as primary factors in the creation of the parasitic FET. [2] The symptoms and footprint of the process failure were readily replicated using a negative ionizing field at 150° C.

The GL effect can be equated to charging a capacitor through a variable resistance. A cross-section of a dual metal circuit and the equivalent GL circuit are illustrated in Figure 1.

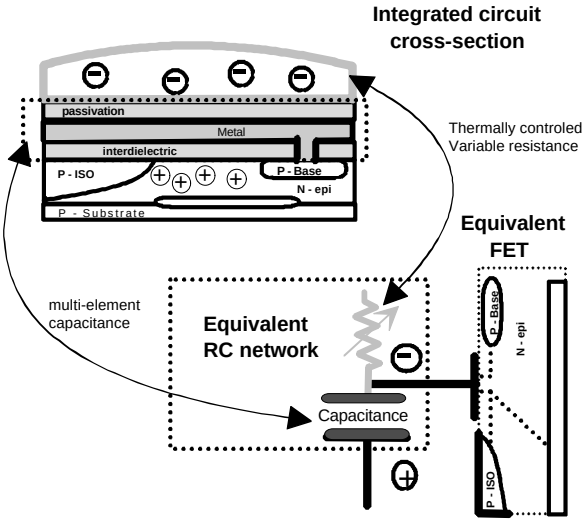

Fig. 1. Cross-section of a dual metal circuit and the equivalent GL circuit.

When a part is subjected to an ionizing voltage field, the die, acting like a capacitor, accumulates and stores an electrical charge within the passivation/epi layers. The magnitude of charge is dependent upon field strength, the conductivity of the encapsulation material, and duration of exposure. When the accumulated charge (symbolized by the È symbols in the plastic encapsulation material and the ⊕ symbols in the n-epi layer) reaches the inherent inversion voltage of the n-epi layer, an inversion layer is created between a p-type diffusion (p-base) and p-iso. The abnormal leakage current in the parasitic path between the base and the iso elements of the die is proportional to the accumulated charge. The parasitic path causes a change in the integrated circuit impedance. The result is a degradation of the associated input pin leakage characteristics and/or an increase in the part Icc and a circuit logic failure.

The plastic encapsulation material acts as a variable resistor and the passivation, metal, and interlevel layers form a multi-element capacitor. Current flow, in the form of electrons/ion migration will flow in the RC network when there is a difference in potential in the form of an ionizing field and a complete electrical path for the current flow. The magnitude of charge depends upon circuit resistance, equivalent capacitance, the applied voltage, and time.

Resistance as it relates to the GL effect, has been found to vary, depending upon the molding compound temperature and the applied voltage. Capacitance is a function of doping levels, passivation, interdielectric composition, pin configuration, and related circuitry.

The effects of GL are observable by curve tracing input pins or by functional and parametric testing.

Figure 2 a illustrates the characteristic curve of an input pin degraded by the GL affect. [3] Figure 2 b, shows the pin/curve returned to a normal state after an unbiased and unpowered thermal bake at 125° C for 4 hours.

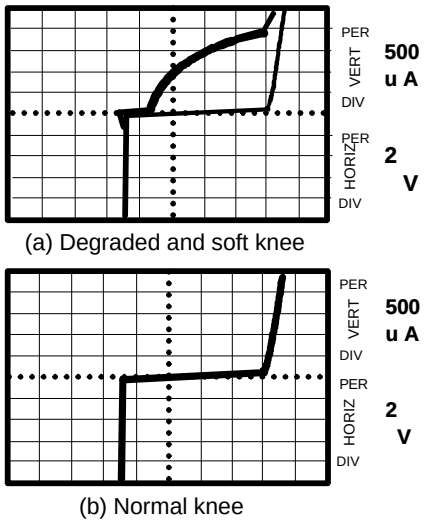

Fig. 2. The characteristic curves of an input pin exposed to and degraded by GL

Several engineering evaluations were performed to confirm the GL conclusions and to determine whether there was an effective alternate process, that would improve the resistance of a plastic encapsulated part to GL. The addition of an insulating polyimide layer, a third layer metal grid, various combinations of passivation/interdielectric materials, the incorporation of field plating, guard rings, various molding compounds and post mold cure-processes were evaluated.

A 12 micron polyimide surface coat was added to die with established sensitivity to GL. [4] The polyimide improved the resistance to charge inversion at the die level by a factor of 7.6 to 1 and die with 24 um coatings were found completely immune to inversion leakages at normal room temperatures. However the polyimide surface coated die, after packaging, were still sensitive to GL at high temperature. It is suspected that the polyimide dielectric effect breaks down at high temperatures ≥ 150° C.

Three passivation and interdielectric configurations were tested. Plasma Oxide passivation was applied as an interdielectric and as a passivation (POPO). Plasma Nitride was applied as an interdielectric and as a passivation (PNPN) and Plasma Nitride applied as a passivation with Plasma Oxide interdielectric (PNPO). The evaluation suggests that the PNPN process is roughly 1.7 times more susceptible to charge accumulation than PNPO, and 2.6 times more than POPO.

While an oxide inter-dielectric improves a part GL characteristics, the change to a plasma oxide process is a significant effort that would require extensive testing, analysis, and re-qualification of the fabrication processes. [5]

It was theorized that a Faraday Cage in the form of a third layer metal grid electrically connected to vcc or vdd would provide a drain for the migrating electrons/ions and prevent charge accumulation. Parts were fabricated with third layer metal grids of five different grid sizes (8, 24, 56, 120, and 248 microns.) The test parts were divided into three electrical configurations; the grids were electrically isolated, connected to vcc, and connected to vdd pins. All groups were exposed to an environment known to induce GL in ungrided parts of the same design and process. Figure 3 illustrates the third layer metal grid or Faraday cage concept.

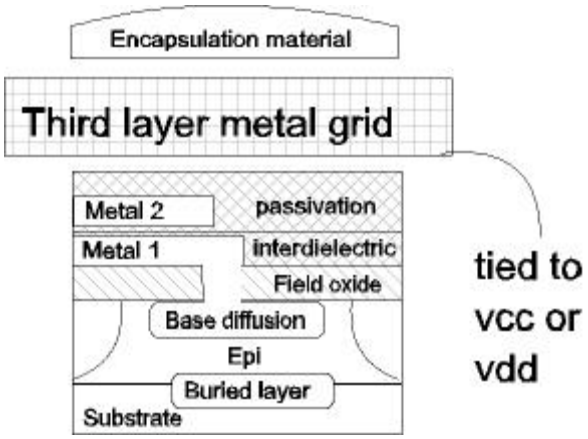

Fig. 3. A typical dual metal part with a third layer metal grid.

Parts with 8 and 24 micron grids connected to vcc or vdd consistently remained functional after the GL exposure. Parts with a 56 micron grid connected to vcc or vdd consistently failed momentarily, then recovered, indicating a mild GL effect. Parts with 120 and 248 micron grids connected to vcc or vdd, and those with grids electrically isolated, consistently failed. [6] Since the Faraday cage, in the form of a 8 and 24 micron third layer metal grid was effective in preventing GL, it was theorized that a cage effect could be duplicated by the addition of field plating and n+ guard rings to sensitive areas. Field plating is the process of overlapping the base and emitter interconnect metallization. The overlapping has the effect of enlarging the depletion layer and theoretically enhances stability of layers exposed to an electrostatic charge and prevents electrostatic narrowing in lightly doped regions. [7] Guard rings, in the form of n+ rings were expected to enhance depletion region stability by increasing the radii of the device corner curvatures. [8]

The addition of field plating has not made a measurable improvement in resistance to GL. Guard rings demonstrated marginal improvements in highly sensitive circuit areas at low GL exposure levels. However they too were ineffective at high exposure levels.

The sensitivity to the charge effect is consistent and unique to each part or process family, depending upon the circuit geometry, passivation, interlevel dielectric, and the fabrication process. To better evaluate the interaction of voltage, time and temperature, a test fixture was assembled to systematically reproduce field voltage and thermal environments.

The method of measurement was expanded to include both parametric and functional measurements and was accomplished using Automated Test Equipment.

A method was developed to provide a controlled and repeatable method of exposing parts to quantifiable exposure levels. While it is not an absolute quantification of the charge/field strength, it does provide for repeatable and relational measurements. Figure 4 illustrates the fixture and equipment used to create the GL environment.

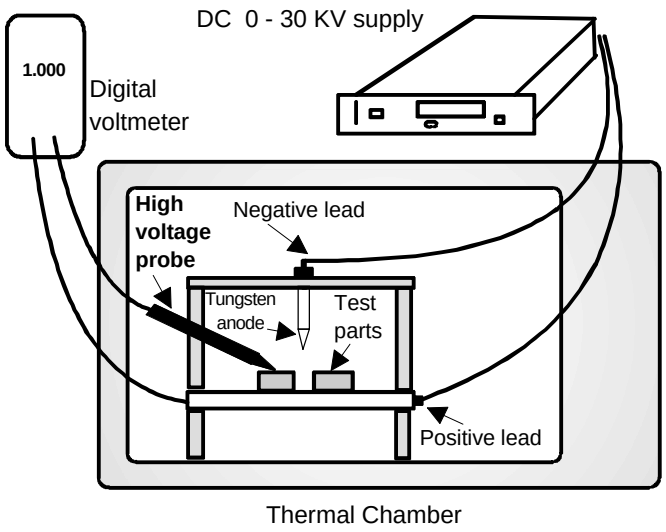

Fig. 4. Gl test fixture and equipment.

A regulated power supply is used to provide a DC positive and negative voltage which is variable from 0 to 30,000 volts. The pointed tungsten anode is used to provide a symmetrical ionizing field. Field strengths are measured with the DMM and a high voltage probe. The mechanical fixturing provides a conductive base plate and an adjustable means with which to set, maintain, and reproduce part to anode distance and test voltages. The thermal chamber provides for testing at elevated temperatures and controlled temperature ramp times. The parts to be tested are placed upon a conductive surface that is electrically connected to the positive terminal of the voltage source. The negative terminal of the voltage source is connected to a pointed tungsten probe. The source voltage and probe to part distance are adjusted within a range of 1 to 5 inches to produce the desired test voltage as monitored with the high voltage probe at the surface of the part.

Parts were electrically characterized and placed in three separate orientations; with the leads in intimate contact with the conductive surface, with the leads up (dead bug) position and with the leads resting on an insulated surface. Only the parts with the leads in intimate contact with a conductive surface and returned to the positive anode failed the post-exposure electrical test.

These results in conjunction with the third layer grid and polyimide experiments, strongly suggest that the GL effects are the result of current flow through package encapsulation material (at elevated temperature) and charge entrapment.

It was indeterminate, at this time, whether the change in sensitivity was due to a change in the molecular structure of the compound, the boiling off of accumulated moisture, or an outgassing of process residue/s (i.e., catalyst, hydrogen or die attach epoxy cure by-products).

It is generally assumed that an encapsulation compound is an insulator, is mechanically and electrically stable at temperatures ≤175° C, and that variations between compounds are primarily due to chemical composition and fillers (i.e., flame retardants and dimensional stabilizers). Preliminary experiments, however, indicated that the sensitivity of a part changed after repeated exposure to temperatures approaching the initial cure temperature.

An experiment was performed to identify and quantify the thermal affects upon the molding compound conductivity/resistance over a range of voltages and temperatures. Molding compounds from four suppliers were evaluated.

Material conductivity/resistance was determined by applying a voltage across the sample and measuring circuit currents. The measurement was repeated over a range of temperatures from 80° C to 180° C to determine the relationship between temperature and compound conductivity. Repetitive measurements were taken to determine if voltage potential affected conductivity.

Each test sample, taken from deliverable parts, was lapped and polished to provide a uniform surface and a thickness of .038 inches, then cleaned to remove any residual surface contamination. The test samples were placed upon the test fixture's conductive plate, which was connected to the positive terminal on the high voltage source. The negative terminal of the voltage source was attached to a pointed tungsten probe in physical contact with, and positioned at the center of the test samples. Current readings were taken at three voltage levels at each temperature to determine if there was a voltage induced change in conductivity.

While the material conductivity increased with an increase in test voltage, there was no noticeable permanent or residual voltage induced memory affect observed in this experiment. The thermally induced changes in the resistance of various materials are shown in Figure 5.

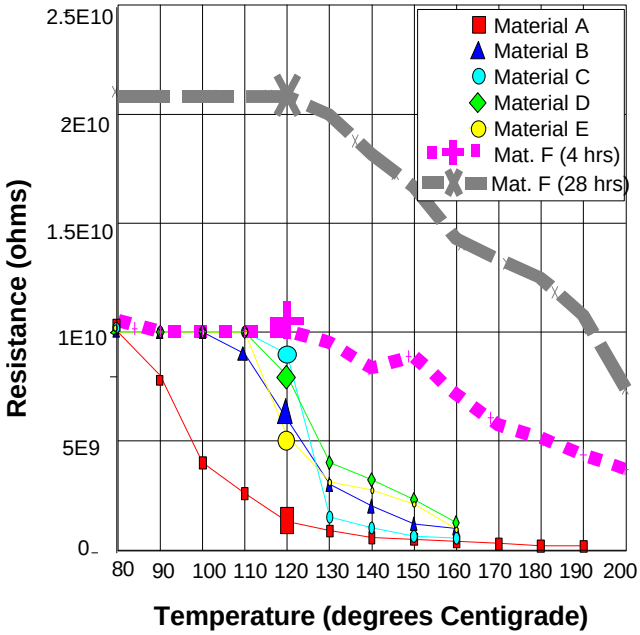

Fig. 5 Material resistance change with temperature.

The resistance of every material tested exceeded 1E10 ohms at temperatures of 80° C or lower. A significant decease in resistance (orders of magnitude) was observed in each material as temperature was increased from 80° C to 130° C. Material "F" illustrates the typical relationship between a normal (4 hour) and an extended (38 hour) cure. Material "F" also represents a low voltage measurement technique which reduced the voltage effect upon the resistance measurement. Every compound exhibited consistent reductions in resistance or increased conductivity with an increase in temperature.

This experiment confirmed that a molding compound conductivity is affected by both voltage and temperature. The measurements were repeated using a Dupont DEA conductivity/loss factor tester. Both test methods yielded results that were consistent with previous experimentation and suggested that GL in plastic encapsulated parts was the result of leakage currents (electron flow) through the molding compound at elevated temperatures.

Since the equivalent circuit appears to be a traditional RC charging circuit, there should be a coherent mathematical relationship between temperature, dwell, voltage and the magnitude of affect. The following formula shows this relationship.

$$GL = \ln.[(\sqrt{Voltage})x(Temp - 100)^2 x(\ln.Time)]$$

Where:
(ln = natural log) (Voltage = volts)
(Temperature = ° C) (Time = minutes)

The rationale was further tested by using the formula to quantify several factory environments known to cause GL. The calculated values of experimental/test environments which caused GL, and those which did not result in measurable GL were compared to factory environment calculations. Table 1 relates the example process and test environments ranging from those that caused little or no GL to those that caused GL 100 % of the time. Factory process examples, with an estimated voltage of 100 volts, are included for comparison.

Table 1. Comparison of GL factors, test environments, and processes.

E-Field (volts)	Temp. ° C	Dwell (min.)	GL (factor)	Comments
1000	110	12.5	8.99	*GL Test:* (very sensitive parts fail.)
300	155	2.5	10.44	*GL Test:* (some part types fail.)
1000	130	17.5	11.31	*GL Test:* (more part types fail.)
100	240	2.1	11.87	*IR Reflow:* (GL failures occur.)
100	125	2880.0	10.82	*Burn-In:* (GL failures occur.)
100	215	1.3	10.45	*Wave-solder:* (GL failures occur.)

A very low field voltage of ≤100 volts, when combined with the high temperatures at IR reflow, exceeds the GL thresholds in the experiments. The IR reflow temperature (240°C) is an absolute worst case thermally saturated part. While 240°C may be an overstatement, the IR reflow assembly operations have experienced the highest failure rate attributed to GL.

It should be noted that even if a field exists in conjunction with a high temperature, the part may or may not be affected. The part lead/s must be returned to the field source (even intermittently) and the source must be an ionizing source. Therefore parts with a common sensitivity may or may not fail in a given process and environment. The calculated levels are reasonable, consistent with process, materials, and part level experiments, and appear to be adequate for evaluation purposes.

Significant and repeatable changes in sensitivity were observed in parts when they were preconditioned by extended baking at temperatures greater than the original cure temperature of 175° C. Every part/material became more resistant to the effects of GL after an additional 20 hour cure at ≥175° C.

In a review of our molding processes it was found that the normal post mold cure duration was 4 hours and the normal cure temperature was 175°C.

Several types of integrated circuits and various compounds representing four suppliers, with and without an extended cure, were tested and evaluated. The product and sub groups tested are listed on the horizontal axis in Figure 6. Each bar represents a unique part type. Suffix "B" denotes baked or extended cure and "BH" denotes a bake followed by humidity. The vertical axis is the calculated GL factor. A larger number indicates a higher temperature, an increased voltage/e-field, or a longer dwell time. Each part type is shown at the exposure level where a failure occurred.

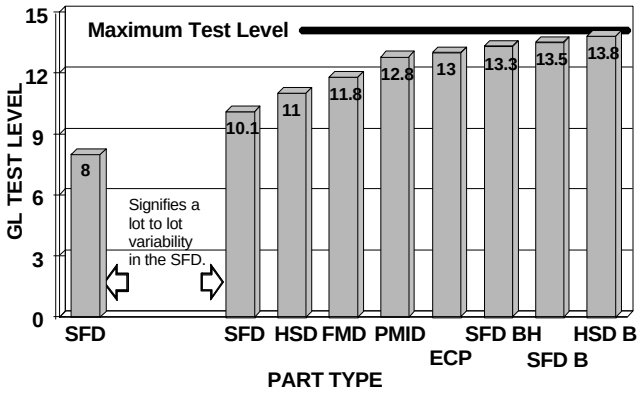

Fig. 6 Relative part resistance to GL.

The subgroups that were subjected to the extended cure (B and BH) were without exception found to be more resistant to GL than the normally processed parts. No failures were observed in an extended cure at a GL factor of 13.8, which was the highest level tested. While there is a correlation between molding compound resistance, cure temperature, cure duration, and GL, it was not known at this point whether the change in sensitivity was the result of a die fabrication process residue, such as hydrogen ions or the outgassing of the die bond epoxies entrapped during the molding process, or whether it was the result of a change in molding compound conductivity. It was also indeterminate whether the longer cure was causing additional polymer cross-linking, thereby changing the Glass Transition Temperature (Tg) or depleting residues (i.e., catalyst by-products) thereby reducing material conductivity, or merely removing absorbed moisture from the packages.

To determine whether absorbed moisture was a factor the GL responses of parts normally processed, extended cure, and extended cure followed by humidity were compared. The extended cure was performed at 175° C for 20 hours. Humidity conditioning consisted of 72 hours of 85° C and 85 % humidity. Samples from both groups SFD B, BH and HSD B were exposed to GL, and retested.

Humidity preconditioning of the samples had no observable effect on part performance and it was concluded that humidity was not a significant factor in the GL phenomenon.

Test die, from a common wafer, were selected after die attach cure and prior to packaging. The test die were divided into two equal groups. One group was baked for eighteen hours at 190° C to force the out-gassing of any process residuals (i.e., hydrogen). The abnormally high temperature 190° C was selected to insure the die attach epoxy was completely cured at a temperature greater than any seen in the remainder of the process.

The parts were then divided into four equal sub-groups, with each sub-group consisting of 50% pre-baked die and 50% standard process die. The sub-groups were cured at 175° C for varying times: subgroup 1 for 4 hours, subgroup 2 for 6 hours, subgroup 3 for 8 hours, and subgroup 4 for 24 hours. Electrical test yields were found to be consistent between the groups. Each sub-group demonstrated consistent changes in functional performance and Icc proportional to the cure time. The relative change in Icc (pre to post GL) by cure time was as follows:

Table 2, Relative change in Icc due to GL.

Post-mold cure time.	Delta Icc. milliamps.	Results/ comments
4 hours	2.3	baseline change
6 hours	2.3	same as base line.
8 hours	1.8	21% reduction in Icc.
24 hours	0.9	61% reduction in Icc.

The pre-assembly die bake cycle at 190° C, the 85° C/85% humidity, and extended cures from four to six hours had little to no affect on GL sensitivity. Extending the cure time to eight hours reduced the GL affected change in Icc by 21%. Extending the cure time to twenty four hours reduced the GL effect by 60%.

The effect of the longer cure time upon the mechanical integrity of the encapsulation material and die interface was evaluated. The test method entailed an initial characterization of the compound-die interface by acoustical microscopy, 168 hours at 85% humidity and 85° C, IR reflow (thermal shock), followed by post conditioning acoustical microscopy. There was no observable difference in mechanical integrity.

These results are consistent with previous experiments. If material conductivity is proportional to the degree of polymer cross-linking, additive by-products, and ambient temperature, it seems reasonable that a longer cure time will increase the molecular stability, out-gas by-products and increase the resistance to electron flow or ion migration through a material.

Most material application notes allude to similar "expected changes in a compound mechanical and electrical characteristics." [9] It is expected that a similar curve exists for the new "fast cure" products. The curve may however be related to a chemical change in the catalyst or other additives/residue rather than polymer cross-linking.

Summary and Conclusions:

GL is a trapped-charge phenomenon that affects plastic encapsulated integrated circuits in varying degrees depending upon technology, design, molding compound and compound cure profile. GL occurs at high temperatures when an ionizing/tribo-electric field is present and the integrated circuit pins are electrically common to the field source. The worst-case/largest charge occurs when all pins are returned directly to the ionizing source. GL can cause yield losses at high temperature processes, especially those with heated air flow (i.e., burn-in, high temperature handlers, and IR reflow solder operations).

Nitride passivated lightly doped dual metal thin-epi bi-polar parts, appear to be the most vulnerable. CMOS technologies have also demonstrated a sensitivity to GL. A part may be sensitive to a positive or negative field depending upon its design. The composition of and the combination of passivation and inter-dielectric has an effect. A part of a given design and process may be more or less sensitive, depending upon the post mold cure temperature and duration. The magnitude of the GL effect is dependent upon temperature, field strength, and duration of exposure.

Several methods of reducing the effects of GL were investigated and discussed: the addition of a third layer metal grid, metal field plating, n+ guard rings, and reducing the conductivity of the mold compound through extended post mold curing. The third layer metal grid connected to vdd or vcc was the only solution tested that was 100% effective in the prevention of GL. The effect of an additional layer of metal upon the long-term reliability, fabrication, and test yields of integrated circuits have not been evaluated. Further testing and evaluation are necessary to determine the effectiveness or benefit to be gained by field plating and n+ rings.

Experimentation with various post mold cure cycles has demonstrated that a longer (24 hour) cure changes molding compound electrical characteristic. That extended post mold cure significantly improves part tolerance and resistance to GL.

Humidity testing indicated the improved performance was not the result of drying the package. Multiple experiments have confirmed that GL sensitivity is affected by circuit fabrication technology, geometry and the encapsulation material/curing process.

Charge sensitive devices such as EPROMs and sub-micron geometries were not evaluated and there is a concern that they may be at significant risk.

While a longer cure time improves a part's GL characteristics, it is not an all encompassing solution. There are other tapped charge phenomenon, and alternative means of generating a charge. Applications, manufacturing assembly, and test operations that have static fields and high thermal environments will continue to present a GL risk to plastic encapsulated parts using today's materials and processes.

Integrated circuit designers and manufactures should evaluate each new design and process change for ETIP-GL sensitivity. Molding compound suppliers should be motivated to provide additional information regarding material electrical insulating characteristics.

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