The Effects of Materials and Post-Mold Profiles on Plastic Encapsulated Integrated Circuits

Richard D. Mosbarger (317-451-7718),
David J. Hickey (317-451-8861),
Delco Electronics, Kokomo, IN, 46904-9005

ABSTRACT

Post-mold cure contributes to the electrical and mechanical properties of Novalac molding materials and affects how those properties change with thermal and humidity environments. Forward biased parasitic gates may be created as the result of thermally induced material changes in conjunction with ionizing fields and by molding compound delamination from the die surface during high temperature assembly operations (e.g., IR-reflow). Molding material conductivity and tolerance to moisture depends upon the material and the post-mold cure environment. Test methods have been developed and equipment is available to quantify compound electrical and mechanical performance and thereby predict material and part performance.

BACKGROUND

Electro-Thermally-Induced Parasitic Gate Leakage

Electro-Thermally-Induced Leakage (GL) is a recently defined material related phenomena in integrated circuits. [1] GL is a thermally induced trapped charge failure mechanism. An integrated circuit's susceptibility to failure is affected by design, fabrication technology, type of molding compound, and the post mold cure profile. The GL phenomenon was first identified in a dual metal, bi-polar, 52 pin, quad-packaged surface mount part. [2] The failure, an out of specification measurement, occurred during hot testing. The measurement returned to normal values when the parts were subjected to a high temperature bake or were opened for failure analysis. The cause of failure was found to be a forward biased enhancement mode parasitic FET with an accumulated charge over a floating epi pocket providing the gate electric field. The failure occurred when a charge accumulated in the topside nitride passivation and became large enough to invert the n-epi surface.

The symptoms and footprint of the failure were readily replicated by the application of a negative ionizing field at elevated temperature (e.g., 150 to 160 °C). Figure 1 illustrates the GL test fixture.

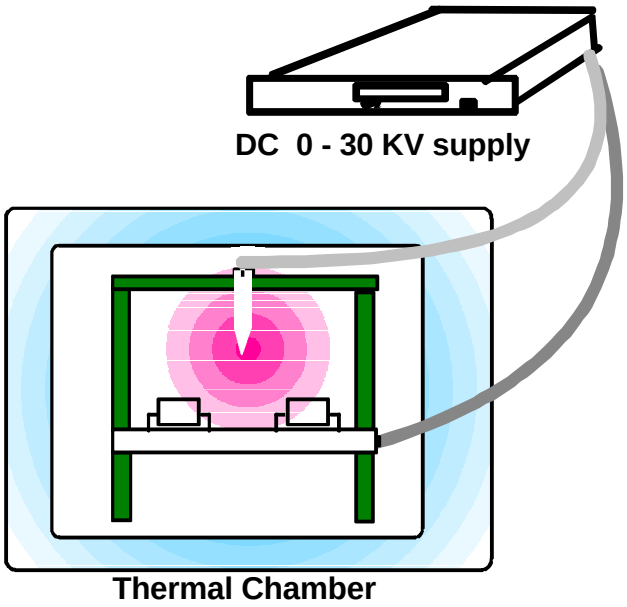

Fig. 1. GL test fixture.

The GL phenomena can be equated to that of charging a capacitor through a variable resistor. A cross-section representation of a bi-polar dual metal circuit and the equivalent GL circuit components are illustrated in Figure 2.

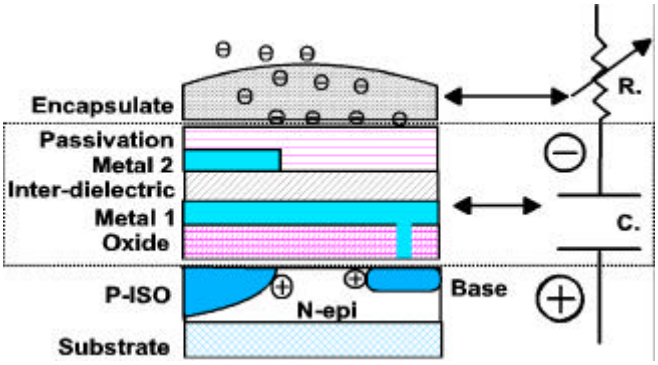

Fig. 2. Cross-section of a dual metal circuit and the equivalent GL circuit.

The molding material acts as a thermally controlled variable resistor. The passivation, metal, oxide and inter-dielectrics combine to form a multi-element capacitor. The temperature and resistance relationships are unique to each compound and molding process. Resistance for any given material will change as a function of the post mold cure temperature and time. Capacitance is a function of passivation, inter dielectric, and circuit lay out. Current will flow in the circuit when there is a difference in potential (e.g., an ionizing field and a complete electrical path). The ability to accumulate a charge and its magnitude depends upon circuit resistance, equivalent capacitance, the applied voltage, and exposure time.

Doping levels influence part sensitivity to the accumulated charge. When the accumulated charge (symbolized by the ⊕ symbols in the n-epi layer) reaches the inherent inversion voltage of the n-epi layer, an inversion layer is created between the p-type diffusion and p-iso. The abnormal leakage current in the parasitic path between the base and the isolation elements of the die is proportional to the accumulated charge. The result is a degradation of the associated input pin leakage characteristics and/or an increase in the part's I_{CC} and a circuit logic failure.

The effects of GL are detected by curve tracing input, measuring I_{CC}, or functional and parametric testing. Curve tracing the power pins or measurement of I_{CC} has been found to be the optimum method of characterizing parasitic leakage in dual metal bi-polar parts.

Figure 3 illustrates a typical input pin curve, Figure 4 shows the same pin degraded by the GL, and Figure 5 shows the same pin (recovered) after a 5 hour bake at 125 °C.

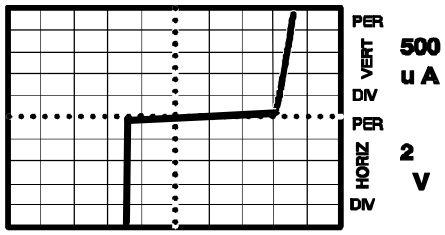

Fig. 3. Normal input pin characteristic curve.

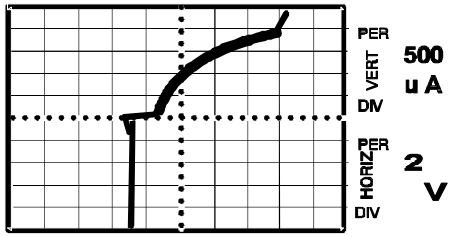

Fig. 4. Input pin exposed to and degraded by GL.

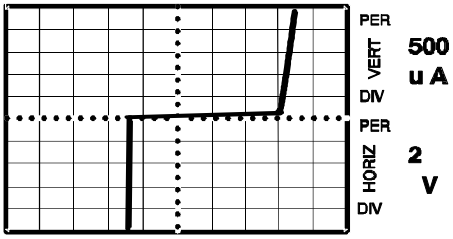

Fig. 5. Input pin returned to normal by an unbiased and unpowered thermal bake at 125 °C for 4 hours.

The sensitivity to the charge effect is consistent and unique to each part or process family, depending upon the circuit geometry, passivation, inter-layer dielectric, and the fabrication process.

Several experiments were performed to confirm the GL conclusions and to determine whether there was an alternate process which would improve a plastic molded part resistance to GL. The effect of an insulating polyimide layer and various combinations of passivation and inter-dielectric materials were evaluated. The effects of field plating, guard rings, the addition of a third layer metal grid, various molding compounds, and post mold cure-processes were evaluated.

A 12 micron polyimide surface coat was added to die with a known sensitivity to GL. [3] The polyimides (at room temperature) improved the resistance to charge inversion at the die level by a factor of 7.6 to 1. Die with 24 µm coatings were found completely immune to inversion leakage at normal room temperatures. The polyimide surface coated die was still sensitive to GL at high temperature. It is suspected that the polyimide dielectric effect changes (the material becomes more conductive at high temperatures ≥ 150 °C).

Three passivation and inter-dielectric configurations were tested. Plasma Oxide passivation was applied as an inter-dielectric and as a passivation (POPO). Plasma Nitride applied as an inter-dielectric and as a passivation (PNPN). Plasma Nitride applied as passivation with Plasma Oxide inter-dielectric (PNPO). The evaluation suggests that the PNPN process is roughly 1.7 times more susceptible to charge accumulation than PNPO, and 2.6 times more than POPO.

It was theorized that a Faraday cage in the form of a third layer metal grid electrically connected to power or ground would provide a drain for the migrating ions and prevent charge accumulation. Parts were fabricated with third layer metal grids of five different grid sizes (8, 24, 56, 120, and 248 microns.) The test parts were divided into three electrical configurations: with grids connected to a power pin, connected to a ground pin, and electrically isolated. Each group was exposed to an environment known to induce GL in ungrided parts of the same design and process.

Parts with 8 and 24 micron grids connected to power or ground consistently remained functional after the GL exposure. Parts with a 56 micron grid failed momentarily, then recovered, indicating a mild GL effect. Parts with 120 and 248 micron grids connected to power or ground consistently failed. Parts with electrically isolated grids consistently failed. [4]

Since a Faraday cage in the form of a 8 and 24 micron third layer metal grid connected to power or ground was effective in preventing GL, it was theorized that the effect could be duplicated by the addition of field plating and n+ guard rings to sensitive areas. Field plating is the process of overlapping the base and emitter interconnect metallization. The enlarged depletion layer theoretically enhances layer stability when exposed to an electrostatic charge and prevents electrostatic narrowing in lightly doped regions. [5] The addition of field plating did not make a measurable improvement in resistance to GL.

The addition of guard rings, in the form of n+ rings, was expected to enhance depletion region stability by increasing the radii of the device corner curvatures. [6] Guard rings demonstrated marginal improvements in highly sensitive circuit areas at low GL exposure levels. However, they too were ineffective at high exposure levels.

It was observed in the experimentation that resistance to GL improved proportionally to the time parts were exposed to temperatures above 175 °C. When extremely sensitive parts were baked or cured for 24 hours or more, they became extremely resistant or immune to GL.

The resistance of several molding compounds was measured by applying a high voltage across a slice of molding material and monitoring circuit current. The calculated resistance as a function of temperature is illustrated in Figure 6.

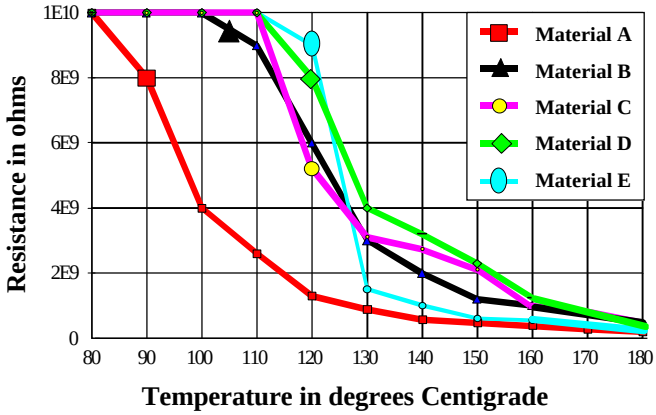

Fig. 6. Molding compound resistance as a function of temperature.

Figure 7 illustrates a similar change in conductivity or permittivity with temperature when it is measured with a 1 volt emf using a DuPont 2970 DEA system.

A single specimen was measured after a 4 hour cure at 175 °C, cured for an additional 24 hours at 175 °C, and then re-measured. The illustration shows a 40% reduction in permittivity as the result of the additional cure.

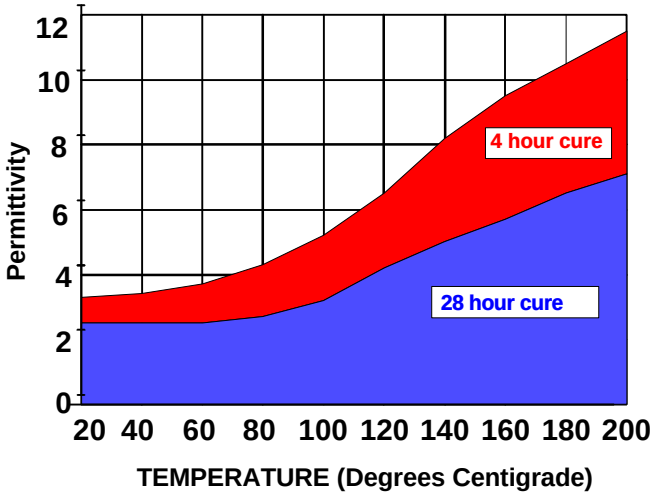

Fig. 7. DuPont DEA plot, permittivity versus cure time and temperature.

Delamination Induced Parasitics Gate Leakage

Parasitics can be generated mechanically when the molding compound delaminates from the die (much like the stripping of tape generates a static charge). The delamination charge induced effect was characterized in the same very sensitive, bi-polar, dual metal part used to evaluate compound electrical characteristics. The parts used to demonstrate the mechanical phenomena were assembled in a high-stress compound which was cured for 4 hours at 175 °C. This part, the high-stress compound, and cure cycle is known to delaminate with a moisture content of approximately 0.2% moisture by weight.

The initial integrity of the compound to die interface was verified by acoustic microscope and then I_{CC} was curve traced and recorded. The parts were then exposed to 168 hours of 85 °C at 60% RH and passed through a vapor phase solder reflow machine 2 times. After reflow, the parts were immediately curve traced again and then re-examined using acoustic microscopy. All four parts were found to be delaminated over 100% of the die surface.

The analysis of the electrical test data showed that the mechanically induced effects were an order of magnitude smaller than the previously described electro-thermally induces effects. A typical I_{CC} curve trace for a pre and post test (delaminated) part is shown in Figures 8 and 9.

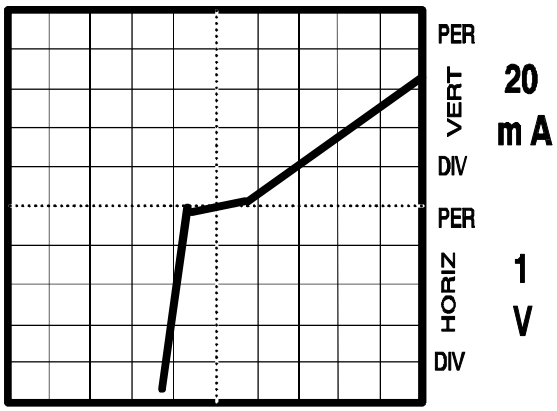

Fig. 8. Curve trace on V_{CC} before delamination.

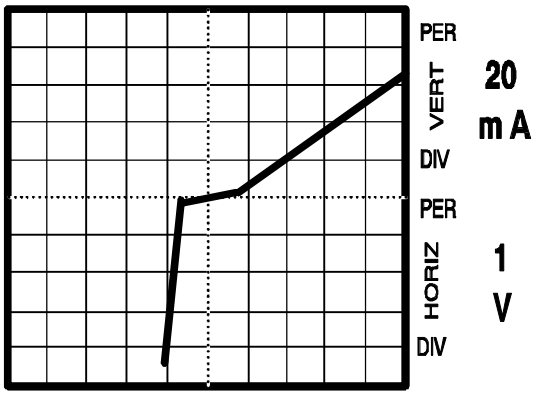

Fig. 9. Curve trace on V_{CC} after delamination.

The shapes of the traces are nearly identical. A more informative table that illustrates the differences of pre and post reflow traces at 5 V is shown below.

Table 1
I_{CC} at 5V before and after test

Part Number	I_{CC} @ 5V Before Reflow	I_{CC} @ 5V After Reflow	% Change in I_{CC} @ 5V
1	55.91 mA	57.16 mA	2.2 %
2	57.78 mA	59.64 mA	3.2%
3	63.99 mA	65.85 mA	2.9%
4	62.13 mA	63.99 mA	2.9%

Using a part that was considered the most sensitive to parasitics (a large die in bi-polar, thin epi, dual metal technology) in combination with high stress compound delamination induced parasitics resulted in a 2% to 3% increase in I_{CC} at 5 Volts.

Figure 10 illustrates the relationship that exists between delamination and Electro-Thermally induced changes in I_{CC}. There is a consistent order of magnitude or greater difference between the two phenomena. Electro-Thermally induced effects more closely replicate line pull device failure characteristics or footprints.

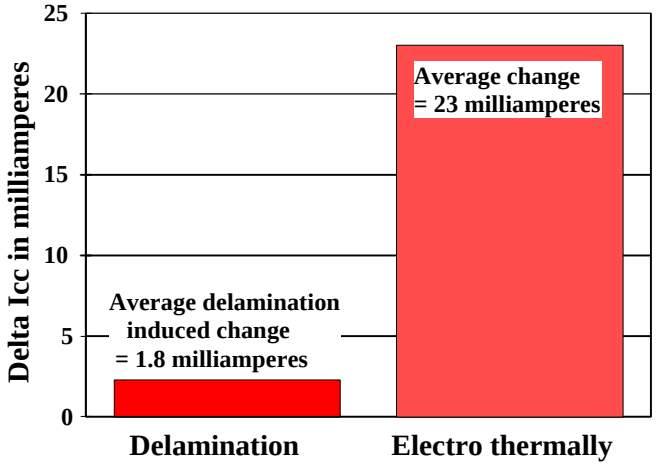

Fig. 10. The relationship of Electro-Thermally and gross delamination induced changes in I_{CC}.

POST MOLD CURE EXPERIMENT

To evaluate the affect of cure time and temperature, sixty-four combinations of molding materials, cure times, and cure temperatures were evaluated. Consistent and conclusive results show that variations in post-mold cure time and temperature dramatically affect the electrical and physical performance of molding materials.

Test results clearly demonstrate that material and post mold cures are key factors in moisture sensitivity/delamination and electro-thermally induced parasitics. This is further evidence that the method of using a fixed absolute moisture content (e.g., 0.1%) as a determination of moisture sensitivity for all parts ***is not*** a comprehensive nor completely reliable method.

Die were assembled in four different types of molding compounds, sub-groups from each compound were cured at 4 temperatures (175 °C, 185 °C, 195 °C, and 205 °C) for 4 different durations (4, 8, 16, and 32 hours). Samples from each sub-group were subjected to identical temperature and voltage fields to determine GL sensitivity. The difference in pre-exposure to post-exposure I_{CC} was analyzed to determine the relative affect of the various mold compounds, cure times, and temperatures. A smaller change in I_{CC} indicates a lower material conductivity.

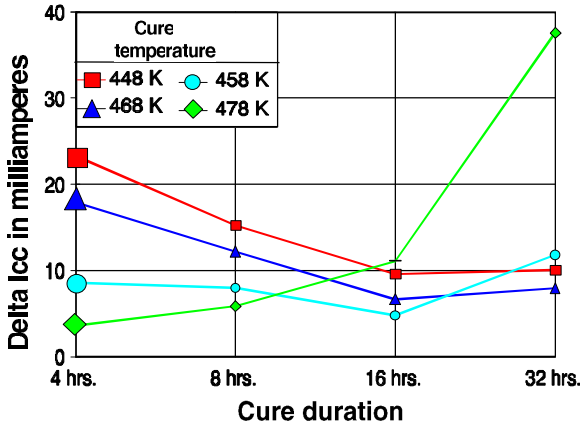

Fig. 11. Electro-Thermally induced change in the I_{CC} for high-stress compound 'A.'

Material 'A' in Figure 11 became increasingly less conductive as cure time was increased at the lower temperatures 175 °C (symbolized by the □) and 185 °C (symbolized by the Δ). At the higher temperatures, however, material conductivity increases with an increase in cure time. The characterization of delamination induced effects was performed using this material.

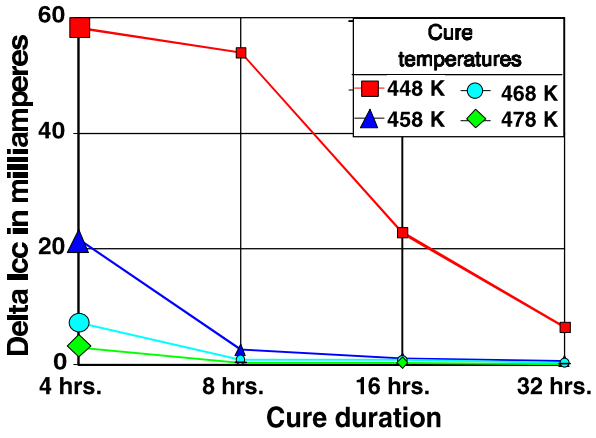

Fig. 12. Electro-Thermally induced change in I_{CC} for low-stress compound 'B.'

The low stress material 'B' illustrated in Figure 12 was the most consistent compound tested. It exhibited a significantly higher conductivity when cured at 175 °C for 4 hours than any other material tested. The low-stress material, however, consistently improved; conductivity and leakage decreased with an increase in cure time and/or cure temperature. There was no tendency towards increased conductivity in this material at extreme cure times or temperatures. A 4 hour cure at 195 °C provided adequate performance for the most sensitive 52-pin, dual metal, bi-polar quad pack tested.

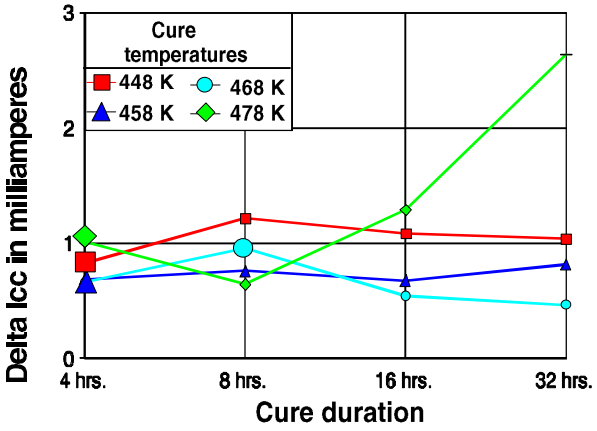

Fig. 13. Electro-Thermally induced change in I_{CC} in medium-stress compound 'C'.

Compound 'C' (Figure 13) was an order of magnitude less conductive than all the other materials evaluated. The 205 °C cure temperature demonstrated an initial decrease in conductivity between 4 and 8 hours. Conductivity increased with an increase in time after 8 hours. At all other temperatures, conductivity was consistently low and stable at the various cure times.

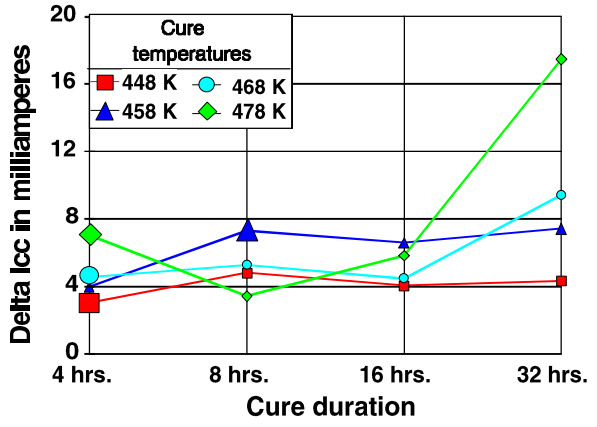

Fig.14. Electro-Thermally induced change in I_{CC} in medium-stress compound 'D'.

Inconsistent changes were observed in compound 'D', see Figure 14. When compound 'D' was cured at 205 °C, conductivity decreased as cure time increased up to 8 hours. Curing beyond 8 hours resulted in increasing conductivity with an increase in cure time. All other cure temperatures demonstrated a similar reaction (increase time resulted in a higher conductivity).

The moisture sensitivity of the parts in this matrix was also investigated. The parts were initially verified on the acoustic microscope as not delaminated, dried, exposed to a 85 °C and 60% relative humidity level for 168 hours, reflowed by a vapor phase machine, and inspected again on acoustic microscope. The 85 °C and 60% RH environment was chosen because parts that pass this level have an expected floor life of one year and may not (under some circumstances) require dry pack precautions. [7][8] The VPR reaches reflow temperatures of approximately 215 °C and dwells at the reflow temperature for 60 seconds.

The marked differences that occur between materials as the result of different post mold cure profiles are illustrated in Figures 15 and 16. These figures are a simulation of the acoustic data gathered from the parts after the moisture test. Each figure represents 64 encapsulated parts. The entire part is shown with the die being shaded or blackened. A sub-group of four parts was subjected to each cure temperature (shown on the horizontal axis) and time (shown on the vertical axis) combination. A gray or cross-hatch shading denotes an intimate and intact interface. A dark or solid color denotes an undesirable separation between the die surface and the molding compound.

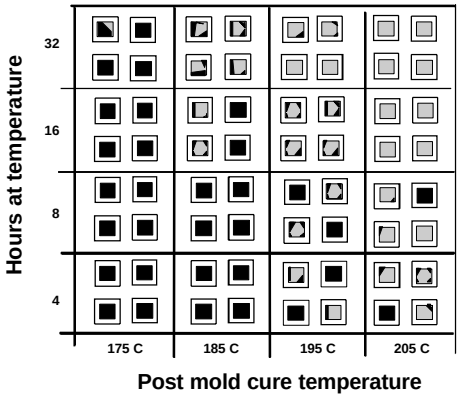

Fig. 15. The relationships of delamination to post-mold cure time and temperature in material 'A.' Black areas indicate delamination and the gray areas indicate adhesion between molding compound and die.

Material 'A' consistently demonstrated poor adhesive qualities. Acceptable adhesive properties were achieved only at the extreme high temperatures (205 °C) and at extended cure times (32 hours).

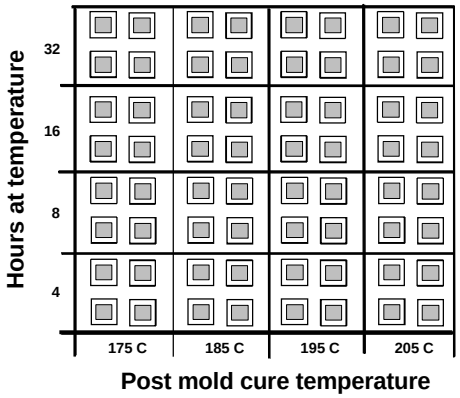

Fig. 16. The relationship of delamination to post-mold cure time and temperature in material 'B'. Black areas indicate delamination and the gray areas indicate adhesion.

The low-stress material 'B' exhibited excellent adhesive qualities. There was no evidence of delamination at this humidity level with cure times of 4 hours at 175 °C to 32 hours at 205 °C.

Material 'A' proved to be the most sensitive material, while the low-stress material 'B' and the medium-stress materials ('C' and 'D' which are not illustrated) demonstrated excellent adhesive qualities with no apparent damage at all levels of post-mold cure. While higher post mold cure temperatures and longer post mold cure times significantly improved the moisture sensitivity characteristics of compound 'A,' it had no measurable influence on compounds 'B,' 'C,' or 'D' at the 85 °C and 60% RH humidity level.

SPECIFICATION OF MATERIAL CONDUCTIVITY

Through experimentation and analysis of part performance in large volume processes, it has been possible to detail test methods that will reliably predict compound and part performance in a high temperature environment. Material ion conductivity levels that will insure acceptable performance in assembly process and field environments are suggested.

The following experiment based GL formula provides a means of quantifying the interactive effects of time, temperature, and electrical field strength. The calculation can be used to evaluate and compare process risks and/or part sensitivities to the GL phenomena.

$$GL = Ln[(\sqrt{Voltage}) \times (Temp - 100)^2 \times (LnTime)]$$

(Ln = natural log) (Time = minutes)
(Voltage = field strength in volts at part surface)
(Temperature = ° Centigrade)

Figure 17 illustrates the characteristic relationship pf the GL induced changes in dual metal bi-polar part I_{CC} to the calculated GL factor. There is a consistent direct correlation between the effect and each of the factors (time, temperature, or voltage). I_{CC} and the GL factor both increase with an increased stress or exposure. Logic failures occurred in the particular dual-metal, n-epi, bi-polar parts used in this evaluation when the change in I_{CC} exceeded 62 milliamperes. The magnitude of change was correlated to assembly process failures.

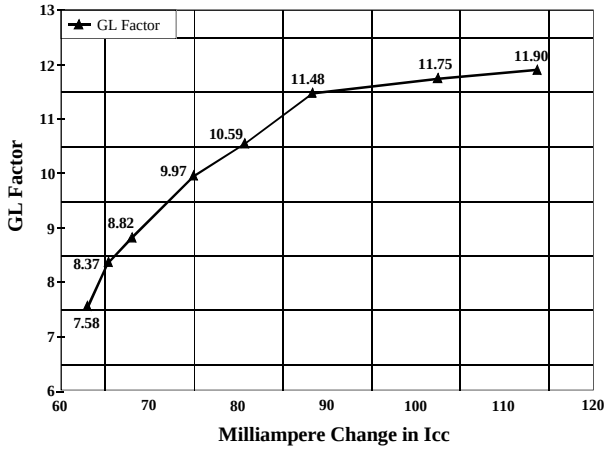

Fig. 17. The relationship of I_{CC} and GL Factor.

A range of test environments and factory processes (e.g., IR-reflow, burn-in, and wave-solder) with exposure levels that resulted little or no GL to those that resulted in a large effect are shown in Table 2.

Table 2.

Comparison of GL factors in
test environments to factory processes.

E-Field in Volts	Temp Deg. C	Dwell Min.	GL Factor	Comments
200	155	4.0	10.99	*GL Test:* very sensitive parts fail
300	155	4.0	11.19	*GL Test:* some parts fail
700	155	4.0	11.62	*GL Test:* more parts fail
100	220	2.1	11.57	*IR Reflow:* most process failures occur
100	125	2880.0	10.82	*Burn-in:* isolated failures occur
100	160	3.0	10.58	*Wave-solder:* isolated failures occur

Historical failure rates and the calculated GL exposure in three factory processes (IR-reflow, burn-in, and wave-solder) were compared. Since the actual electrical field strengths were unknown, a very low field voltage of 100 volts was used in the calculation. The low 100 volt field, when combined with the high temperature of IR reflow (240 °C), provided the worst case GL environment. The IR reflow assembly operations have demonstrated the highest failure rate attributed to GL. The extended time (2880 minutes of burn-in) in combination with the relatively low temperature of 125 °C yielded a lower GL factor. Experience has shown a very low incidence of confirmed GL failures at burn-in. Wave-solder was calculated to be the lowest factor and experiences the lowest failure rate.

Several types of integrated circuits and various compounds representing four suppliers with and without an extended cure, dry, and moisture saturated were tested and evaluated. The product and sub-groups tested are listed on the horizontal axis in Figure 18. Each bar represents a unique part type. The vertical axis is the calculated GL factor. A larger number indicates a higher temperature or a larger voltage-field. The bars indicate the numerical GL factor at the lowest exposure level that a failure for that part type occurred. A higher number or factor indicates a more robust part. The horizontal line at a 11.8 level indicates the suggested stress level that an acceptable part should pass based upon the failure and pass rates of the evaluated parts in surface-mount assembly process.

Parts were selected at random from deliverable product and tested for GL sensitivity. Additional samples of the 2 part types that were found to be the most sensitive were broken up into two sub-groups. Both sub-groups were cured for an additional 20 hours at 175 °C. One group was then saturated with moisture by a 168 hour soak at 85% humidity and 85 °C. The GL evaluation was then repeated on the extended cure and humidified parts.

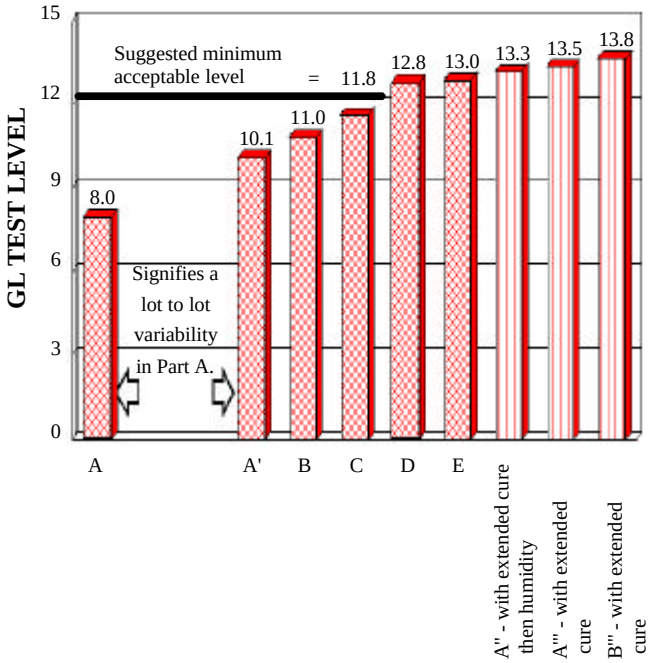

Fig. 18. Variability in part resistance to GL.

Part type A exhibited the greatest lot to lot variability (A to A') and was the most sensitive to GL. Part B exhibited a lesser degree of lot to lot variability and was the second most sensitive part tested. Line pull and field failures related to GL have been confirmed for both parts A and B.

Subgroups of A", A'", and B'" with both extended cure and extended cure followed by humidity exposure (the vertically striped bars in Figure 18) were all found to be more resistant to GL than the normally processed parts. Even when subjected to 168 hours at 85 °C and 85% humidity, part A" showed no significant change in the extended cure enhanced GL characteristics.

Since humidity preconditioning of the samples had no observable effect on GL performance, it was concluded that the package moisture content was not a significant factor in Electro-Thermally-Induced GL.

The analysis of field performance, assembly line defects, and test results suggests that there is a high risk of failure in any part that becomes non-conforming to its specification (increased current drain or logic fault) after an exposure to a GL level of 11.8 or less, using the static charge test method and test temperatures of 155°C.[9] An acceptance level of 11.8 can be achieved by proper mold compound selection and optimization of the post mold cure profile.

The DuPont 2970 Dielectric Analyzer (DEA) system provides an alternative and automated means with which to quantify material electrical performance (ion conductivity or permittivity measurement) as a function of temperature.

A preliminary level of performance has been determined by evaluating material conductivity and the resultant effect upon circuit performance in the assembly process and field environments. Figure 19 illustrates a suggested criterion for an acceptable level of ionic conductivity/permitivity.

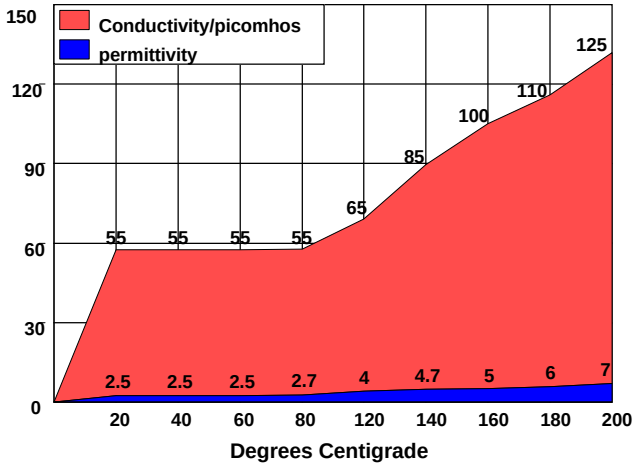

Fig. 19. Ionic conductivity change as a function of temperature.

The maximum acceptable ionic conductivity (as measured using a DuPont 2970 DEA) should fall within the envelope illustrated by the cross-hatch in Figure 19. Permittivity should not exceed 10 (the solid area in Figure 19).

In this experiment, the material was characterized to 200 °C. It is important, however, that permitivity and conductivity be characterized over a thermal range which includes the expected process and operational temperature extremes.

While the suggested level may be appropriate for the technologies and processes that were evaluated, it may or may not be the optimum for alternate compounds, other more robust or more sensitive technologies, designs, or hostile environments (e.g., high voltage applications, sustained junction temperatures of >150 °C, or space applications). Testing to this criterion does not negate the need for other test methods in use today (e.g., dielectric characterization).

Early experiments on a high current driver (which operates at very high junction temperatures) demonstrated that in heavy load applications this device was particularly vulnerable to GL.

The GL effects as the result of high voltage operation and elevated junction temperatures (125 to 175 °C) have not been quantified. Charge sensitive devices such as EPROMs and sub-micron geometries were not evaluated and there is a concern that they may be at significant risk.

SUMMARY AND CONCLUSIONS

GL is a trapped-charge phenomenon that affects plastic encapsulated integrated circuits in varying degrees depending upon technology, design, molding compound, and compound cure profile. GL occurs at high temperatures when an ionizing/tribo-electric field is present.

GL can cause yield losses at high temperature processes, especially those with heated air flow (e.g., high temperature handlers and IR reflow solder operations).

Electro-Thermally induced parasitics cause an increase in I_{CC} ranging from 5 to 60 milliamperes (a 10% to 100% increase). Gross delamination of the molding compound from the surface of the die produced changes in I_{CC} of 1.2 to 1.8 milliamperes (2% to 3% change).

Delamination varied with each material and cure duration and ***was not solely*** a function of the absolute moisture content.

While CMOS technologies have demonstrated a sensitivity to GL, nitride passivated, lightly doped, dual metal, thin-epi, bi-polar parts appear to be the most vulnerable. Passivation and inter-dielectric materials also affect sensitivity.

A part may be sensitive to a positive or negative field depending upon technology and design. The addition of a third layer metal grid connected to power or ground pins is effective in eliminating GL. Further testing is necessary to determine the affects of the grid on long term reliability. The addition of a polyimide coating, field plating, and n+ guard rings were marginal in their effect.

While an optimized cure time and temperature improves molding compound moisture sensitivity and electrical characteristics, extended cure is not an all encompassing solution. Larger die, reduced geometry, increased junction temperatures, high voltage applications, and high temperature environments will continue to present a physical and electrical risk to plastic molded parts.

Integrated circuit designers, IC manufactures, and compound suppliers must consider the functional characteristics and the end use environment in the evaluation of new materials, designs, and process changes.

ACKNOWLEDGMENTS

The following people enabled and made significant contributions to the content of this paper.

Gerry Servais: Who made this paper possible through his conception of and dedication to his group, the allocation of resources, and many technical and editorial consultations.

Steve Barlow and Steve Duey: For their early work in identifying and describing the GL phenomena, their design change experiments and for sharing of historical data and files.

Paul Staab: For his expertise in materials, consultations, and contributions to the set-up, execution, and analysis of the device level package experiment matrix.

Rick Tubbs and Brad McClellan: For their sharing of historical files, failure analysis processes, and their early investigation of GL.

REFERENCES:

[1] R. D. Mosbarger, "Electro-Thermally Induced Parasitic Gate Leakage (GL)," *Proceedings of 19th International Symposium for Testing & Failure Analysis*, 1993, pp. 205-211.

[2] Stephen Barlow and Ajay Desai, *Investigation of SFD-03 Fails From SFI ECM*, Kokomo, IN: Delco Electronics, 27 September, 1987.

[3] Stephen Barlow, *Die Level Surface Charge Inversion Testing for PNPN Passivation/Interlevel Materials With and Without 12 UM Polyimide Surface Coats (FAB Level)*, Kokomo, IN: Delco Electronics, 6 December 1989.

[4] Stephen Barlow, *Generic Leakage Third Layer Metal Experiment*, Kokomo, IN: Delco Electronics, July 1990.

[5] Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, New York, Chichester, Brisbane, Toronto, Singapore: John Wiley & Sons, Inc., 1984, pp. 77-79.

[6] Sorab K. Ghandhi, *VLSI Fabrication Principles*, New York, Chichester, Brisbane, Toronto, Singapore: John Wiley & Sons, Inc., 1983, pp. 357, 594, and 610.

[7] IPC-SM-786A Committee, IPC-SM-768: *Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages*, Draft, 9 October 1993.

[8] JEDEC Solid State Products Engineering Council, JEDEC-1.14 A112: *Moisture-Induced Stress Sensitivity for Plastic Surface-Mount Devices* (JCB-92-35A), Draft, December 1993.

[9] Richard D. Mosbarger, *Electro-Thermally- Induced Parasitic Gate Leakage (GL) Specification and Classification Criteria*, Method 322, Q-1000 Delco Electronics Qualification Procedures, Kokomo, IN: Delco Electronics, 4 January 1993.