Issues Concerning CDM ESD Verification Modules – The Need to Move to Alumina

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Abstract – In this work, we demonstrate that both capacitance and inductance must be the central parameters associated with the Charged Device Model (CDM) waveform verification modules. We also propose a change from the previously used FR-4 dielectric material substrate to a more stable Alumina. This improves waveform repeatability and will lead to better correlation of test results. This paper completes the groundwork for a full ESDA CDM device testing standard.

Introduction

Major discrepancies exist among results obtained from verification modules designed for verifying Charged Device Model (CDM) ESD simulator waveforms [1]. One such verification module is specified in ESD Association (ESDA) CDM draft standard DS5.3.1-1996 [2] and shown in Figure 1. The modules are constructed with two gold-plated or nickel-plated, etched copper disks (one small disk and one large disk, as shown in Figure 1a and 1b respectively) on single sided 0.800 mm thick FR-4 circuit board dielectric material. Each disk is created through a plating/etching process and is centered on dielectric material that is at least 30 mm square. These modules will be referred to as Capacitance Only Modules (COMs).

During waveform verification, the COM is placed on the charging plate of a CDM ESD simulator, with or without an additional thin (130 μm) dielectric film (see Figure 2). Another CDM standard, JEDEC JESD22-C101 [3], specifies two verification modules consisting of one small metal disk (diameter = 0.35 in or 8.89 mm) and one large metal disk (diameter = 1.00 in or 25.4 mm). These disks are brass plated nickel, and may have an optional gold flash coating over the nickel. These JEDEC standard verification modules will be referred to as Disk On Plate (DOP), since each disk is placed directly on the thick dielectric plate and held down with vacuum through the charging field plate (see Figure 3).

The limited repeatability and correlation of CDM simulator results have delayed the development of a full ESDA CDM standard. The present COM design variations reduce the repeatability of positive/negative peak current and risetime values, measured when verifying CDM simulators at specified voltage levels. Data shows that the existing COM design considers only the calculated capacitance values of devices. In this paper, we present reasons for adding inductance to the verification module, controlling module capacitance, and COM calibration. Some of the parameters affecting the COM design include the dielectric constant (K), disk diameter (D), and dielectric thickness (t).

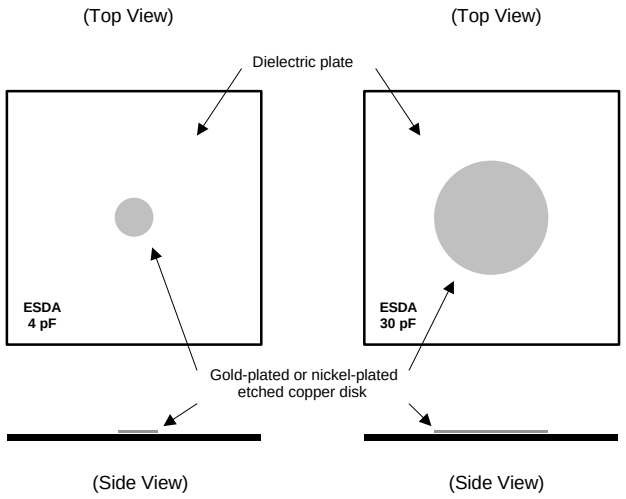


Figure 1: ESDA verification modules, (a) 4 pF and (b) 30 pF

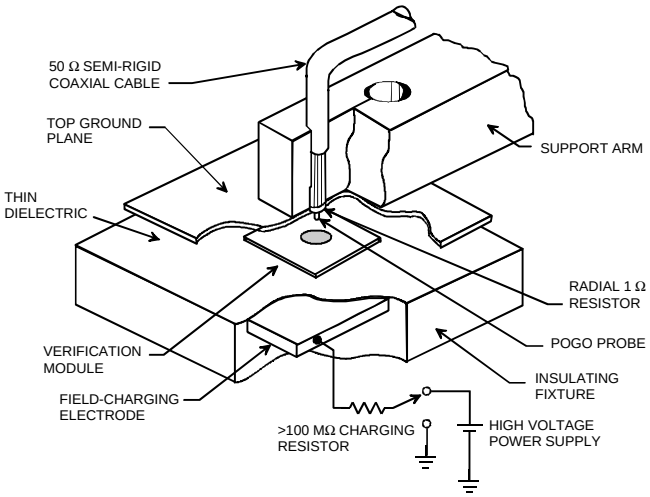


Figure 2: ESDA test configuration using COM verification module

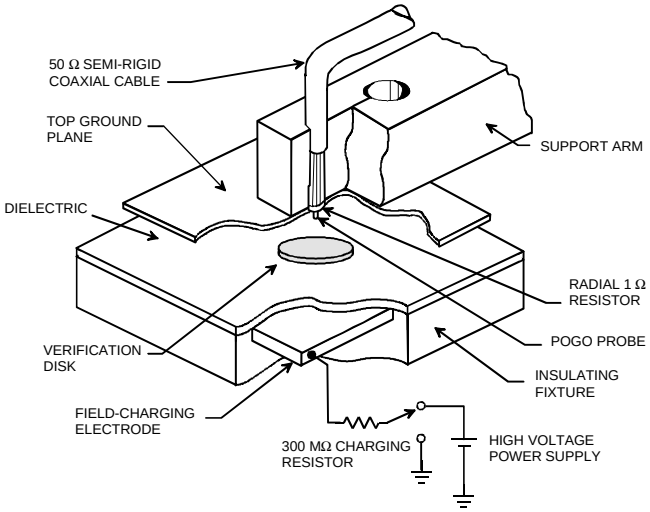


Figure 3: JEDEC test configuration using DOP verification module

Background

Data collected and presented [1] to the ESDA Device Testing Working Group 5.0 has shown that COMs, supposedly made to the same specification, can produce significantly different peak currents when measured under identical conditions. For small and large COMs, both peak current and risetime values measured with 1.0 GHz bandwidth (BW) digitizers are significantly lower than those measured with 3.5 GHz BW digitizers [4]. In practice, the bandwidth capability of the measuring system must be at least twice (2x) the ringdown frequency of the incident CDM pulse for no more than a 12% margin of error [5]. This was one of the first indications that a new verification module design was needed.

To investigate the power-law dependence of peak current [6] on the COM capacitance value, capacitance values were measured for fifteen different COMs from various vendors and lab locations. The capacitance values ranged from 3.31 - 4.58 pF for the small COM (4 pF) and from 15.60 - 33.20 pF for the large COM (30 pF). Some of the measured values fall well outside the acceptable capacitance range set by the ESDA standard [2]: 3.80 - 4.20 pF (4 pF +/- 5%) for the small COM and 28.50 - 31.50 pF (30 pF +/- 5%) for the large COM. These measurements assume that a dielectric thickness of 0.800 mm, as specified in the ESDA standard, is used during the construction of the COMs. However, measured COM dielectric thickness values ranged from 0.660 - 0.787 mm (see Appendix Table A1). These errors are additive and therefore contribute to the limited repeatability and correlation problems associated with the present verification modules. This was another indication to create new verification modules and specify the measurement of their capacitance values. The question becomes: “Why do the measured capacitance values have such a wide range?”

Theoretical Basis for Capacitance

It is important to consider the parameters controlling capacitance. Looking at the theoretical basis for capacitance [7], the following equation can be found:

$$C = E_o K A / t = E_o K (\Pi D^2) / 4t \quad \text{[Equation 1]}$$

where, E_o = dielectric permittivity
K = dielectric constant
A = cross-sectional area
t = thickness
D = diameter

Using Equation 1 and the specified values of capacitance, dielectric thickness, and disk diameter listed in the ESDA CDM draft standard DS-5.3.1 (see Appendix Table A2), a wide variation is possible for dielectric constant values, K. The dielectric constant is related to the material used to manufacture the verification modules. Using these calculated values for dielectric constant (K), further use of Equation 1 allows for the calculation and comparison of disk diameter and capacitance. The results show both a compliant and non-compliant value for capacitance, dependent on the dielectric constant value. All modules were constructed to meet specified requirements except for the dielectric constant value.

The above example illustrates the wide variation possible if certain parameters are not specified for the manufacture of verification modules. This is and has been a major problem, especially if the capacitance value of the COM is not measured/verified before using to obtain CDM waveform parameters. Similar arguments [8] can be advanced for the JEDEC standard. Since capacitance, metallic disk flatness, dielectric thickness, and FR-4 dielectric constant values are not given in the JEDEC standard (see Table A1), certain assumptions had to be made. These assumptions include use of dielectric constant values as calculated for the ESDA COM (5.10 and 5.68) and previously published JEDEC dielectric thickness values [6]. Based on this data, it is deduced that the thickness of the 6-in. x 6-in. square dielectric plate used by the JEDEC standard could be either 0.015 in (0.381 mm) or 0.030 in (0.762 mm). The results show that for a given disk diameter (8.89 mm) and dielectric thickness (0.781 mm), different capacitance values can be obtained. This discrepancy is due to the variation in the dielectric constant, K.

Measured capacitance values for several JEDEC disks and dielectric plate combinations ranged from 3.60 - 7.22 pF using the small disk and from 21.75 - 56.00 pF when the large disk is used. These measured values do not correspond to the capacitance values calculated using the dielectric constant value for the ESDA draft standard measurement and JEDEC disk diameter.

Further, the data in Table 1 shows the behavior of the large JEDEC disk as the dielectric thickness varies. To illustrate the dielectric constant effect, capacitance values are calculated for a given disk diameter, dielectric thickness, and dielectric constant. A disk diameter of 25.40 mm was used, as specified for the large JEDEC disk (see Table A2). Dielectric thickness values of t = 0.8 mm, as specified for ESDA (see Table A2), and t = 0.015 in (0.381 mm), from published data on JEDEC testing [6], were selected. It is well established that the dielectric constant of FR-4 material ranges from 3.6 to 5.5 [9]. For this illustration, the minimum (K = 3.6), maximum (K = 5.5), and average (K = 4.6) values were used. The resulting capacitance values, as shown in Table 1, vary widely and often fall outside the expected value of 30 pF. This is unrealistic and provides another example of how module parameter values can differ.

Table 1: Calculated capacitance values for Large JEDEC DOP

Diameter D, (mm)	Thickness t, (mm)	Diel. Constant K	Cap. C, (pF)
25.40	0.800	3.0 (K-min)	16.82
25.40	0.800	4.7 (K-avg)	26.36
25.40	0.800	6.0 (K-max)	33.64
25.40	0.381 [9]	3.0 (K-min)	35.32
25.40	0.381 [9]	4.7 (K-avg)	55.44
25.40	0.381 [9]	6.0 (K-max)	70.65

Additional measurements revealed that capacitance values varied for some verification disks depending on which side of the disk the data was collected. This is due to air gaps under warped disks (not flat on both sides). Theoretically, the peak current value must extrapolate back to a given capacitance value. As shown in Appendix Table A3, peak current measurements (1.0 GHz BW) taken for both ESDA and JEDEC verification modules are identical for a given charging voltage. If the capacitance values are not the same for both CDM standards (ESDA and JEDEC), the peak current values in both standards cannot be the same.

In comparing the small modules for both ESDA and JEDEC (see Table A3), we find that the ESDA COM specifies a peak current of 14 A at 500 V, while the JEDEC DOP is specified for a lower voltage (3.5 A at 200 V). Neither standard specifies a peak current value for both voltage levels. If linearity is assumed [10] similar to the large ESDA COM and JEDEC DOP, the peak current values can be extrapolated as 8.75 A at 500 V for the JEDEC DOP and 5.6 A at 200 V for the ESDA COM. There is no agreement here, identifying another major discrepancy between the two documents.

Capacitance Ratio Theory for Small and Large COMs

Using capacitance Equation 1, the simple capacitance ratio theorem of Equation 2, and assuming the dielectric constant (K) is the same for both the 4 pF and 30 pF COMs, a comparison of capacitance and diameter ratio values can be made.

$$\frac{C1}{C2} = \frac{A1/t1}{A2/t2} = \frac{(D1)(D1)/t1}{(D2)(D2)/t2} = \frac{(D1)(D1)}{(D2)(D2)} = \frac{(D1)^2}{(D2)^2} \qquad \text{[Equation 2]}$$

The ratio of capacitance values (4/30 or 0.1333) must equal the ratio of the squares of the calculated disk diameter values. This capacitance and diameter ratio relationship must be maintained if the peak current values for the small and large modules are to be consistent. If for simplicity (relative to manufacturing) we make the dielectric thickness value the same for both COMs, the ratio of the disk diameter values specified in the existing available CDM standards [2,3] becomes 0.1198 for ESDA and 0.1225 for JEDEC. This is a difference of 10% between the capacitance and diameter ratios; a difference that contributes to the existing variation in capacitance and eventual variation in peak current. A closer look reveals that the diameter ratios $(D1)^2/(D2)^2$ using values specified in each standard $(9)^2/(26)^2$ [ESDA] and $(8.89)^2/(25.4)^2$ [JEDEC] are too low and therefore not correct. The only correct disk diameter ratios are $(9.5)^2/(26)^2$ or $(9)^2/(24.65)^2$ for ESDA and $(8.89)^2/(24.35)^2$ or $(9.27)^2/(25.4)^2$ for JEDEC.

The Dielectric Constant

It is now easy to show that the dielectric constant (K) is a major factor. An assumed K ties a specific dielectric thickness to the final capacitance value and similarly, an assumed dielectric thickness ties a specific K to the final capacitance value being specified in the CDM standards. An increase in K results in an increase in C. It is seen that if no control in K exists, capacitance values will not agree and peak current values will not correlate.

It is well established that the dielectric constant of FR-4 ranges from 3.6 to 5.5 [9]. Recall that in Table A1 the extrapolated K values ranged from 5.10 to 5.68 when the module parameters of D, C and t are used as specified in the ESDA standard. This range in K values exceeds the maximum acceptable value used by the industry [9]. Similarly, the results for JEDEC parameters (see Table A1) and the assumed C and K values from Table A2, show calculated thickness values that are different from those found in the ESDA standard. A 5% change in capacitance corresponds to a 5% change in thickness if the diameter value remains constant. However, the change is approximately 2.6% for the disk diameters.

These results lead to a comparison of the possible ways to meet the required capacitance values specified in each standard (see Table 2). For the ESDA small disk module (D = 9.00 mm), a slight difference in thickness can produce both acceptable (C = 4.00 pF) and unacceptable (C = 3.31 pF) capacitance values (see Table 2, lines 1 and 3). For the JEDEC small disk (D = 8.89 mm), a slight difference in thickness also produces acceptable (C = 4.00 pF) and unacceptable (C = 3.23 pF) capacitance values (see Table 2, lines 2 and 4). The results are similar for the large module and disk. Although the K is held constant, the wide range in dielectric thickness values resulted in unacceptable capacitance values. This demonstrates not only the effect of a lack of control on parameters but also the effect of inadequate specifications used to manufacture the modules.

Table 2: Theoretical calculations and comparisons for FR-4

Standard	Diameter, D (mm)	Thickness, t (mm)	Diel. Const., K	Cap., C (pF)
1. ESDA	9.00	0.800	4.7	3.31 (c)
2. JEDEC	8.89	0.800	4.7	3.23 (c)
3. ESDA	26.0	0.800	4.7	27.62 (c)
4. JEDEC	25.4	0.800	4.7	26.36 (c)
5. ESDA	9.00	0.381	4.7	6.94 (c)
6. JEDEC	8.89	0.381	4.7	6.78 (c)

* Note: (c) identifies the calculated parameters

Measurement Limitations in Time Domain

As mentioned earlier, the resulting COM waveform risetime was at the limitation of 3.5 GHz BW digitizers. To accomplish the goal of reducing the waveform risetime values specified in the standard, discharge waveforms were measured from the pins of several packaged devices at voltage levels ranging from 500 V to 1000 V.

Device pins with different lead lengths produced waveforms with varied peak currents, risetimes, and full width half-maximum position (FWHM) values. In all cases, the values from the actual devices were much lower (peak currents), broader (FWHM), and slower (risetimes) than those obtained from the COMs [8]. The waveform shown in Figure 4 is from a 48-pin plastic dual-in-line (PDIP) packaged device with risetime ≈370 ps. This will allow for the use of 1.0 GHz BW digitizers during waveform verification.

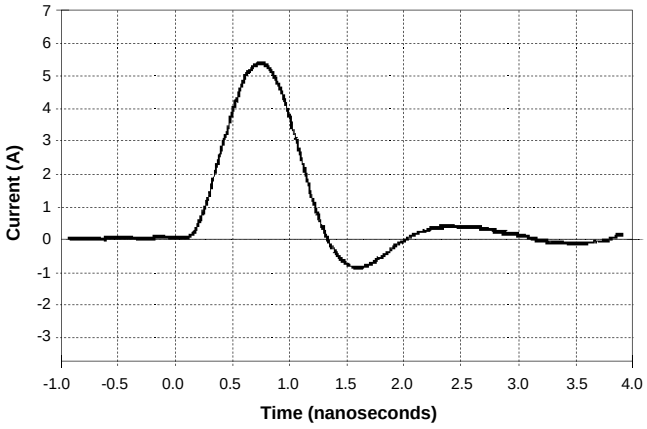


Figure 4: Discharge waveform from packaged device (silicon die in place)

The same was done for empty packages (no silicon die) and similar results were obtained (see Figure 5). These results, as shown in Table 3, show that the different CDM waveform parameters can be correctly associated with the inductance of the bond wire, lead frame, and empty package leads.

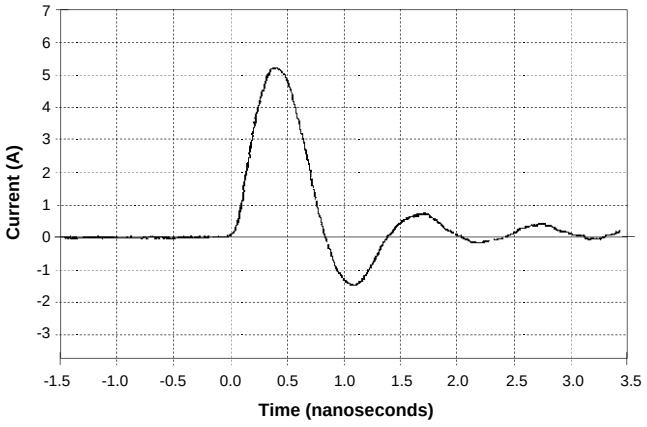


Figure 5: Discharge waveform from empty package (no silicon die)

Table 3: Data for packaged devices; empty and with silicon die in place

Package	Voltage (V)	Trise (ps)	Ip (A)	FWHM (ns)
20-24 pin PDIP (Empty)	500	250-330	4.55	0.50
20-24 pin PDIP (Empty)	1000	250-330	10.75	0.54
48 pin PDIP (Empty)	1000	370	15.99	0.70
32 pin PLCC (die in place)	1500	270	16.60	0.49
44 pin PLCC (die in place)	1750	330	17.66	0.54
44 pin PQFP (die in place)	1000	280	15.46	0.58
292 pin PGA (die in place)	1000	270	13.98	0.51
292 pin BGFA (die in place)	500	420	10.65	0.63

Inductance Consideration

A closer look at the COMs and DOPs reveals an important fact: there is no consideration for the inductance and impedance of the packaged device. The present modules are comprised solely of a conductive disk in intimate contact with one side of the dielectric material, becoming a capacitor when the dielectric side is placed on the CDM charge plate as shown in Figure 6.

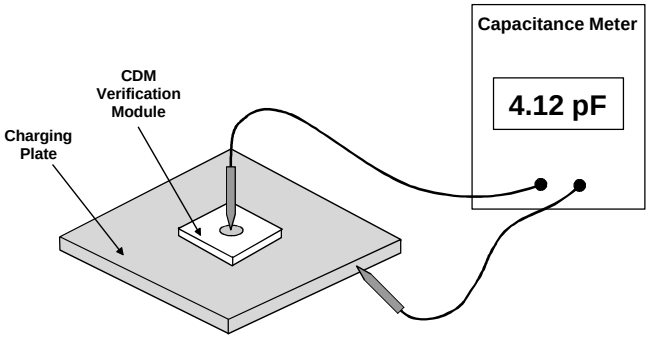
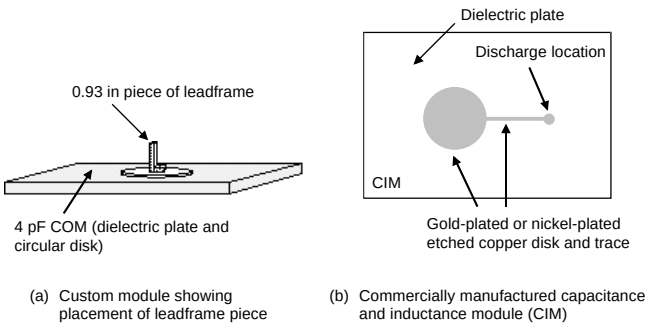


Figure 6: Illustration of COM module placement on charge plate

In order to duplicate the RLC effect of a packaged device, initial custom modules were constructed using a 0.93-in piece of leadframe cut from a 48-pin plastic dual-in-line (PDIP) package. The leadframe was soldered (vertically) to the center of the circular conductive plate of a small 4 pF COM (see Figure 7). We will refer to this new module as the Capacitance-Inductance Module (CIM).



(a) Custom module showing placement of leadframe piece

(b) Commercially manufactured capacitance and inductance module (CIM)

Figure 7: First generation CIM using vertical piece of leadframe

This CIM produced waveforms (see Figure 8) similar to both the empty packages (no silicon die) and the packaged devices (silicon die in place). The waveform shown in Figure 8 is from an empty 24-pin plastic dual-in-line (PDIP) package (~24 pF) with all pins downbonded to the leadframe. Since the risetime ≈340 ps, the 1.0 GHz BW digitizer can be used during waveform verification.

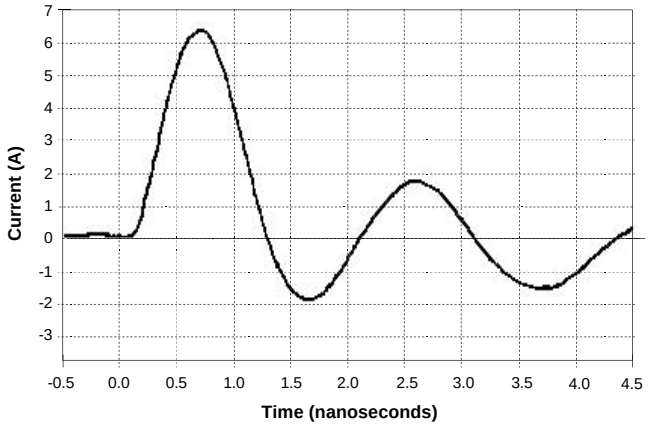


Figure 8: Discharge waveform from first generation CIM

In order to have some idea of the inductance associated with this new design, another CIM was constructed with the leadframe soldered to the edge of the disk and made to lie in a horizontal position (see Figure 9). Time Domain Reflectometry (TDR) measurements, using a HP54120/121A 12 GHz Sampling Scope, were performed on the home-built CIM and resulted in an inductance value of 9.89 nH, where the relationship L = (t)(Z) is used with t = time in nanoseconds and Z = impedance in ohms across the CIM structure [11]. An impedance range of 85 Ω to 94 Ω was measured across the structure and produced a capacitance value of 5.62 pF using the relationship C = (t)/(Z). The measured capacitance value was 5.10 pF using both the Boonton Capacitance Meter Model #5200 and the HP Impedance Analyzer Model #4191A. This value is well within the range of measured capacitance values of 2 - 11 pF for empty packages (no silicon die) and 1 - 26 pF for packaged devices (silicon die in place).

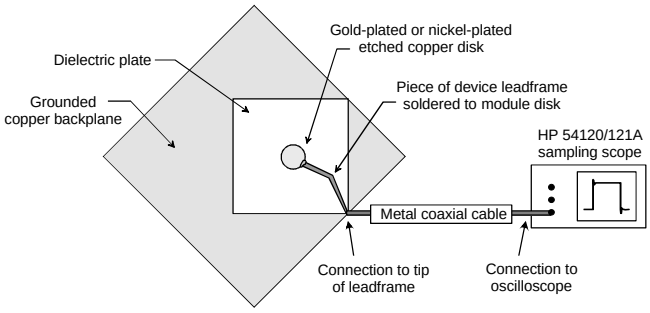


Figure 9: Second generation CIM and TDR measurement configuration

Because of the much slower risetime values associated with the CIM (see Table 4), a 1.0 GHz BW digitizer (350 ps risetime) could be used to measure the discharge waveforms. This is a critical issue since the 3.5 GHz BW digitizer is no longer commercially available. Properly designed and manufactured CIMs (see Figure 2b) of 4 pF, 10 pF, 20 pF, 30 pF, and 40 pF capacitance values were used to collect the data shown in Table 5. The CIMs were then submitted to the ESDA CDM WG-5.3.1 for a major round robin effort, confirming the slower risetime values and lower peak current values of Table 5.

Table 4: Module data for 3.5 GHz BW measurement

Module	Cap. (pF)	Charge (V)	Ip1 (A)	Ip2 (A)	Ip3 (A)	Trise (ps)	FWHM (ns)
COM	4	500	7.1 to 7.83	3.12 to 3.35	1.41	130 to 140	0.24
CIM	4	500	6.0 to 6.86	2.70 to 3.64	1.27	200 to 220	0.37

Table 5: Theoretical and measured CIM parameter values

Theoretical C (pF)	Measured C (pF) at 1 MHz	Theoretical D (mm)	3.5 GHz Trise (ps)	1.0 GHz Trise (ps)
4.00	5.12	9.50	234	334
10.0	9.80	15.00	313	425
20.0	21.40	21.25	371	459
30.0	31.8	26.00	420	494
40.0	39.4	30.00	480	520

The Move to Alumina Ceramic Dielectric

If we turn our attention to other parameters affecting the discharge waveform, we find humidity to be a major contributor. Obviously, the properties and kinetics of the discharge arc will change with humidity [12,13,14]. However, it has been overlooked that a change in humidity will also affect the moisture content of the FR-4 dielectric substrates involved in both COMs and DOPs. FR-4 is a polymeric material known to absorb as much as 22% moisture content (as shown in Table 6) during a 24-hour period at room temperature [9]. Collected data reveals a major change in peak current (Ip) value for a FR-4 dielectric after exposure to moisture for 24 hours. The FR-4 material also has a dielectric constant dependent on frequency (see Table 6), as specified [9] and demonstrated by Carey and DeChiaro [6]. Since the energy and waveform shape of the CDM discharge event is dependent on the dielectric constant of the verification module, a more stable dielectric constant is required.

Table 6: Comparison of parameter values for various dielectric materials

Name	Material	Diel. Constant, K	% Moisture	% Solvent	Loss Factor
FR-4	Epoxy glass	4.4 to 5.5 (up to 1 MHz)	0.17 to 0.22%	4.7%	-----
RF-35	Ceramic-filled epoxy glass	3.4 to 3.6 (up to 2 GHz)	0.02%	Inert	0.0018 to 0.025
Alumina-96	Ceramic	9.5 to 9.0 (up to 8 GHz)	0.00%	Inert	0.0002 to 0.0008

Table 6 shows that the best overall material seems to be Alumina, a ceramic material with minimal change in K over frequency up to 8 GHz (see Table 6). Specifically, note the inert nature of Alumina to solvents and absence of moisture absorption. Based on the tabulated data and using Equation 1, new sets of COMs and CIMs (similar to Figure 4b) were designed and manufactured using the Alumina dielectric substrate.

Table 7 shows the theoretical and measured capacitance values obtained for various dielectric thickness and disk diameter values. Note that the measured capacitance values range from 3.90 - 29.8 pF as Alumina dielectric thickness and disk diameter were varied. Some of this initial data was obtained by simply placing the disks on the dielectric plate and using the vacuum to hold the disk in place for the measurements.

Table 7: Measured parameters for Alumina dielectric material

Diameter (in) / (mm)	Thickness (in) / (mm)	Theoretical Cap. (pF)	Measured Cap. (pF)
0.354 / 9.00	0.025 / 0.635	7.79	7.30
0.600 / 15.24	0.025 / 0.635	20.00	22.90
0.350 / 8.89	0.010 / 0.254	19.84	13.30
0.354 / 9.00	0.025 / 0.635	8.50	7.98
0.354 / 9.00	0.030 / 0.762	6.50	6.65
0.354 / 9.00	0.050 / 1.267	4.00	3.90
0.970 / 24.65	0.050 / 1.267	30.00	29.80

The new Alumina CIM configuration was then used to obtain waveforms (see Figure 10) over a voltage range of 250 V to 2000 V and first peak current (Ip) values were measured. A plot of the peak current (Ip) values versus charging voltage for an 8.5 pF Alumina CIM revealed a linear relationship (see Figure 11). This work does not preclude the use of other stable ceramic substrate materials.

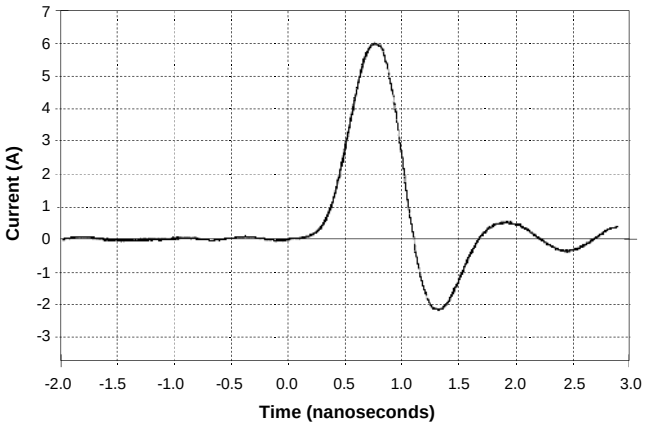


Figure 10: Discharge waveform from new Alumina CIM

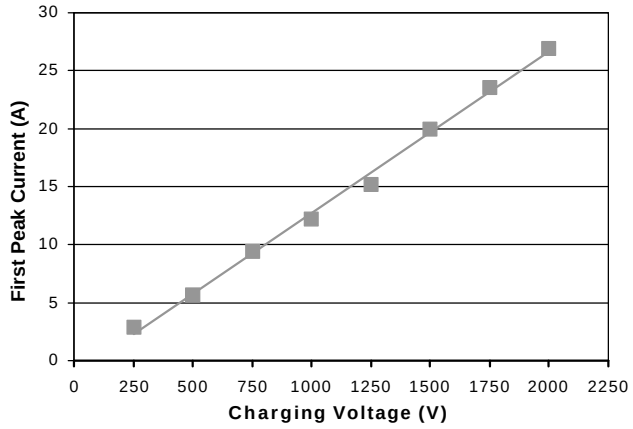


Figure 11: Plot of first peak current (Ip) versus charging voltage for Alumina CIM

Summary

Major discrepancies exist among different Charged Device Model (CDM) ESD simulators when using present verification module designs to obtain discharge waveforms. These modules, referred to as a COM (ESDA) or DOP (JEDEC), only considered capacitance values of devices while ignoring the inductance associated with packaged devices. We show that there can be large variations in the capacitance values if certain parameters like dielectric constant (K), disk diameter (D), and dielectric thickness (t) are not specified. We introduced the CIM verification module, consisting of both capacitance and inductance to better represent actual devices. Discharge waveforms obtained from the new CIM modules closely replicate the discharges from packaged devices. This work has demonstrated that a change is needed from the present FR-4 dielectric material substrate to an Alumina substrate that is more stable for a number of critical parameters. This new dielectric material can greatly improve waveform repeatability and will lead to better correlation of test results. We show that a change to Alumina is needed to allow for the completion and release of a full ESDA CDM standard.

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Appendix A

Table A1: Measured ESDA COM parameter values

Parameter	Required Value, (mm) *	Measured Value, (mm)
Dielectric Thickness	0.800	0.660 to 0.787
Small Disk Diameter	9.00	9.02 to 9.22
Large Disk Diameter	26.00	26.21 to 26.42

* Note the absence of a tolerance value

Table A2: ESDA & JEDEC verification parameter values

Parameter	ESDA	JEDEC
Dielectric Material (6x6 inch)	FR-4	FR-4
Dielectric plate dimensions	30 mm x 30 mm	N/A
Dielectric plate thickness	0.80 mm	N/A
Module Capacitance	4.0 pF +/- 5%	N/A
Module Capacitance	30 pF +/- 5%	N/A
Disk diameter (small)	9.0 mm	8.89 mm (0.35-in +/-0.005-in)
Disk diameter (large)	26.0 mm	25.40 mm (1.00-in +/-0.005-in)
Ground Plane dimensions	N/A	N/A
Dielectric film on charge plate	130 microns	FR-4 plate used
Disk thickness	N/A	1.27 mm (0.050-in +/-0.002-in)

Table A3: Module parameters for 1.0 GHz BW measurement

Standard	Thickness (mm)	Cap. (pF)	Ip (A) at 200V	Ip (A) at 500V	Ip (A) at 1000V
ESDA	0.800	4	N/A	4.5 +/-20%	9.0 +/-20%
JEDEC	N/A	N/A	N/A	4.5 +/-11%	9.0 +/-11%
ESDA	0.800	30	N/A	14 +/-20%	N/A
JEDEC	N/A	N/A	3.5 +/-14%	N/A	N/A