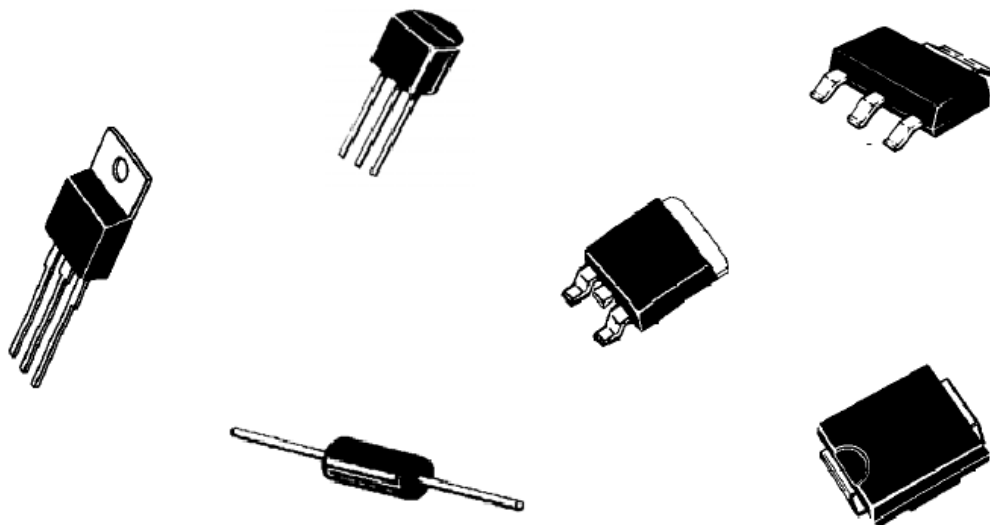


FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS



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This document is dedicated in memoriam to:
Bob Knoell (1957-2018)

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**FAILURE MECHANISM BASED STRESS TEST QUALIFICATION
FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS**

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures and tables have also been revised, but changes to these areas have not been underlined.

Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.

1. SCOPE

This document defines minimum stress test driven qualification requirements and references test conditions for qualification of discrete semiconductors (e.g. transistors, diodes, etc.). This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. Additionally, this document does not relieve the supplier from meeting any user requirements outside the scope of this document. In this document, "user" is defined as any company developing or using a discrete semiconductor part in production. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

1.1 Purpose

The purpose of this specification is to determine that a part is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Military

MIL-STD-750 Test Methods for Semiconductor Devices

1.2.2 Industrial

UL-STD-94 Test for Flammability of Plastic Materials of Parts in Devices and Appliances.

JEDEC JESD-22 Reliability Test Methods for Packaged Devices

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

JEDEC/IPC J-STD-035 Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components

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1.2.3 Automotive

AEC-Q001 Guidelines for Part Average Testing

AEC-Q005 Pb-Free Test Requirements

AEC-Q006 Qualification Requirements for Components Using Copper (Cu) Wire Interconnections

AEC-Q101-001 Human Body Model (HBM) Electrostatic Discharge (ESD) Test

AEC-Q101-003 Wire Bond Shear Test

AEC-Q101-004 Miscellaneous Test Methods

- Unclamped Inductive Switching
- Dielectric Integrity
- Destructive Physical Analysis

AEC-Q101-005 Charged Device Model (CDM) Electrostatic Discharge (ESD) Test

AEC-Q101-006 Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

1.2.4 Other

IATF 16949

1.2.5 Decommissioned

AEC-Q101-002 Machine Model (MM) Electrostatic Discharge (ESD) Test

- Removed from JEDEC due to obsolescence. HBM and CDM cover virtually all known ESD-related failure mechanisms.

1.3 Definitions

1.3.1 AEC Q101 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the part is "AEC-Q101 qualified". The supplier, in agreement with the user, can perform qualification at sample sizes and conditions less stringent than what this document requires. However, that part cannot be considered "AEC-Q101 qualified" until such time that the unfulfilled requirements have been successfully completed. Note that there are no "certifications" for AEC-Q101 qualification and there is no certification board run by AEC to qualify parts.

The minimum ambient temperature range for discrete semiconductors per this specification shall be -40°C to +125°C operational.

Any parts being qualified with Cu wire must follow the requirements in AEC-Q006. The test requirements in AEC-Q006 supersede what is in this document. All other tests are performed to AEC-Q101 (see note 3 in Table 2).

1.3.2 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user's method of approval is beyond the scope of this document.

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1.3.3 Terminology

In this document, “part” refers to the same entity as would “device” or “component” (i.e., a singulated diode, transistor, varistor, etc.) with the die molded in a plastic mold compound or unmolded (i.e. metal can transistors, glass diodes, etc.) with solderable terminations for board attachment. Discrete products delivered as bare die or in wafer form are still qualified to Q101 using appropriate carriers or surrogate packages.

2. GENERAL REQUIREMENTS

2.1 Precedence of Requirements

In the event of conflict in the requirements of this specification and those of any other documents, the following order of precedence applies:

- a. The purchase order
- b. The individual agreed upon part specification
- c. This document
- d. The reference documents in Section 1.2 of this document
- e. The supplier's data sheet

For the part to be considered qualified per this specification, the purchase order and/or individual part specification cannot waive or detract from the requirements of this document.

2.2 The Use of Generic Data to Satisfy Qualification and Re-qualification Requirements

The use of generic (family) data to simplify the qualification/re-qualification process is encouraged. To be considered, the generic data must be based on the following criteria:

- a. Part qualification requirements listed in Table 2.
- b. Matrix of specific requirements associated with each characteristic of the part and manufacturing process as shown in Table 3.
- c. Definition of family guidelines established in Appendix 1.
- d. Represent a random sample of the normal population.
- e. Use the worst-case part within product/process family.

Appendix 1 defines the criteria by which parts are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the part in question.

With proper attention to these qualification family guidelines, information applicable to other parts in the family can be accumulated. This information can be used to demonstrate generic reliability of a part family and minimize the need for part-specific qualification test programs. This can be achieved through qualification of a range of parts representing the “four corners” of the qualification family (e.g., highest/lowest voltage, largest/smallest die, etc.). Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Table 2. Table 1 provides the requirements showing how the available part test data may be applied to reducing the number of lots required for qualification. Electrical characterization to the individual user part specification must be performed for each part submission, generic characterization data is not allowed. **The user(s) will be the final authority on the acceptance of generic data in lieu of specific part test data.**

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Table 1: Part Qualification/Re-qualification Lot Requirements

Part Information	Lot Requirements for Qualification
New part, no applicable generic data.	Lot and sample size requirements per Table 2.
A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1.	Only part specific tests as defined in section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
A new part that has some applicable generic data.	Review <u>Section 2.2 above</u> to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Table 3 to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests.

Table 2 defines a set of qualification tests that must be considered for both new part qualifications and re-qualification associated with a design or process change.

Table 3 defines a matrix of appropriate qualification tests that must be considered for any changes proposed for the part. Table 3 is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification/requalification in question. **It is the supplier's responsibility to present and document rationale for why any of the highlighted tests need not be performed.**

2.3 Test Samples

2.3.1 Lot Requirements

Lot requirements are designated in Table 2, herein.

2.3.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

2.3.3 Reusability of Test Samples

Parts that have been used for nondestructive qualification tests may be used to populate other qualification tests. Parts that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.3.4 Sample Size Requirements

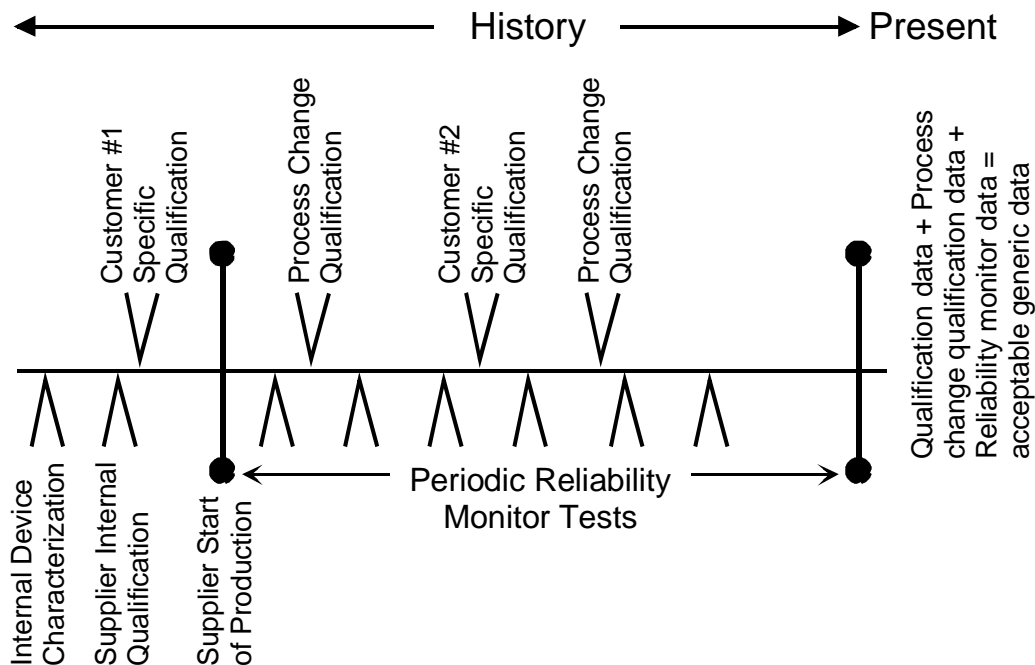
Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. If the supplier elects to submit generic data for qualification/requalification, the specific test conditions and results must be reported. Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.3 for each test requirement in Table 2. Part specific qualification testing should be performed if the generic data does not satisfy these requirements.

- The supplier must perform any combination of the specific part to be qualified and/or an acceptable generic part(s) that totals a minimum of 3 lots x 77 pcs/lot.

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2.3.5 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data as long as the appropriate reliability data is submitted to the user for evaluation. Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. Potential sources of data could include any user specific data (withhold user name), process change qualification, and periodic reliability monitor data (see Figure 1).



Note: Some process changes (e.g., die shrink) will affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

Figure 1: Generic Data Time Line

2.3.6 Pre- and Post-Stress Test Requirements

All pre- and post-stress test parts must be tested to the electrical characteristics defined in the individual user part detail specification at room temperature.

2.4 Definition of Test Failure after Stressing

Test failures are defined as devices exhibiting any of the following criteria:

- a. Parts not meeting the electrical test limits defined in the first user's part specification or appropriate supplier part specification. Minimum test parametric requirements shall be as specified in Appendix 5.
- b. Parts not remaining within $\pm 20\%$ of the initial reading of each test after completion of environmental testing. For leakages below 100nA, tester accuracy may prevent a post stress analysis to initial reading.
 - o For IOL, PTC and TC tests on products with $R_{DSon} \leq 2.5$ mOhm max, the allowed value for the shift of R_{DSon} is ≤ 0.5 mOhm.

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- For breakdown voltage only, a shift of >20% of the initial measured value is a failure only if the final reading is within 20% of the datasheet maximum value.
- c. The allowed leakage limits which are not to exceed 10 times the initial value for moisture tests and 5 times the initial value for all others.
 - For MOSFETs only, for 0h test values <10nA (IGSS and IDSS), the allowed value after stressing is **100nA** for moisture tests and **50nA** for other tests.
- d. Any part exhibiting external physical damage attributable to the environmental test.

Parts exceeding these requirements must be justified by the supplier and approved by the user. If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

2.5 Criteria for Passing Qualification/Re-qualification

Passing all appropriate qualification tests specified in Table 1, either by performing the tests (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the part per this document.

Parts that have failed the acceptance criteria of tests required by this document require the supplier to satisfactorily determine root cause, implement and verify the corrective action to assure the user that the failure mechanism is understood and contained. The part shall not be considered as passing stress-test qualification until the root cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. If generic data contains any failures, the data is not usable as generic data unless the supplier has verified corrective action for the failure condition. Upon qualification data submission, the user may request the supplier to demonstrate the effectiveness of the corrective actions.

It is strongly recommended to conduct thorough analysis to detect potential component weakness on tested parts that produce behavior or responses that are outside the sampling population, even if those parts are still marginally within acceptance criteria.

Any unique reliability tests or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and user requesting the test, and will not preclude a device from passing stress-test qualification as defined by this document.

2.6 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 2 are beyond the scope of this document. Deviations (e.g., accelerated test methods) must be demonstrated to the AEC for consideration and inclusion into future revisions of this document.

See Appendix 7: AEC-Q101 and the Use of Mission Profiles for more information.

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3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Part

Stress test requirements and corresponding test conditions for a new part qualification are listed in Table 2. For each qualification, the supplier must present data for ALL of these tests, whether it is stress test results on the specific part or acceptable generic family data. A review is to be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user. For each part qualification, the supplier must present Certificate of Design, Construction and Qualification to the requesting user. See Appendix 2.

3.2 Re-qualification of a Changed Part

Re-qualification of a part is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the part (see Table 3 for guidelines).

3.2.1 Process Change Notification

The supplier will meet mutually agreed upon requirements for product/process changes.

3.2.2 Changes Requiring Re-qualification

As a minimum, any change to the product, as defined above, requires performing the applicable tests listed in Table 2, using Table 3 to determine the re-qualification test plan. Table 3 should be used as a guide for determining which tests need to be performed or whether equivalent generic data can be submitted for the test(s).

3.2.3 Criteria for Passing Re-qualification

All requalification failures shall be analyzed for root cause, with corrective and preventive actions established as required. The part and/or qualification family may be granted "qualification status" if, as a minimum, proper containment is demonstrated and approved by the user, with corrective and preventive actions established and verified, normally via requalification.

3.2.4 User Approval

A change may not affect a part's operating temperature grade, but may affect its performance in an application. Individual user authorization of a process change shall be based on a contract between Supplier and User, and is outside the scope of this document.

3.3 Qualification Test Plan

The supplier is requested to initiate a discussion with each user (as needed) resulting in completion of a signed Qualification Test Plan agreement as soon as possible after supplier selection for new parts, and at the time of notification (see Section 3.2.2) prior to process changes. The Qualification Test Plan, as defined in Appendix 3, shall be used to provide a consistent method of documentation supporting what testing will be performed as required by Tables 2 & 3.

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4 QUALIFICATION TESTS

4.1 General Tests

Test flows are shown in Figure 2 and test details are given in Table 2. Not all tests apply to all parts. For example, certain tests apply only to hermetically packaged parts, others apply only to power MOSFET parts, and so on. The applicable tests for the particular part type are indicated in the "Note" column and the "Additional Requirements" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test.

4.2 Part Specific Tests

The following tests must be performed on the specific part (i.e., family data is not allowed for these tests):

- a. Electrostatic Discharge Characterization (Table 2, Tests E3 and E4)
- b. Parametric Verification (Table 2, E2) - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user part specification.

4.3 Data Submittal Type

Data to be submitted to the user are classified in three types (Data Type column in Table 2):

4.3.1 Data Type 1

Data (generic or specific) from these tests should be formatted as defined in Section 4.4 and included in each qualification submission.

4.3.2 Data Type 2

Package specific data that should not be included with each qualification submission (except where the package is new). In place of this data the supplier can submit a "Document of Completion" that references successful completion of the specific test previously performed, provided no significant changes have been made. For Test C2 (Physical Dimensions), the Document of Completion should be completed referencing the appropriate user packaging specification.

4.3.3 Data Type 3

Re-qualification data should be included in the qualification submission as required by Table 3. For new parts, data should be included in the qualification submission as required by Table 2. These tests shall be considered by the supplier during re-qualification plan development as useful tools to provide supporting rationale for new part qualification (including new packages) and/or process changes. It is the supplier's responsibility to present rationale for why any of these tests need not be performed.

4.4 Data Submission Format

A data summary shall be submitted as defined in Appendix 4. Raw data and histograms shall be submitted to the individual user upon request. All data and documents (e.g., justification for non-performed tests, etc.) shall be maintained by the supplier in accordance with IATF 16949 requirements.

4.5 Requirements for Testing Pb-free Components

The supplier shall follow the requirements of AEC-Q005 Pb-Free Test Requirements for all parts whose plating material on the leads/terminations contains <1000ppm by weight of lead (Pb).

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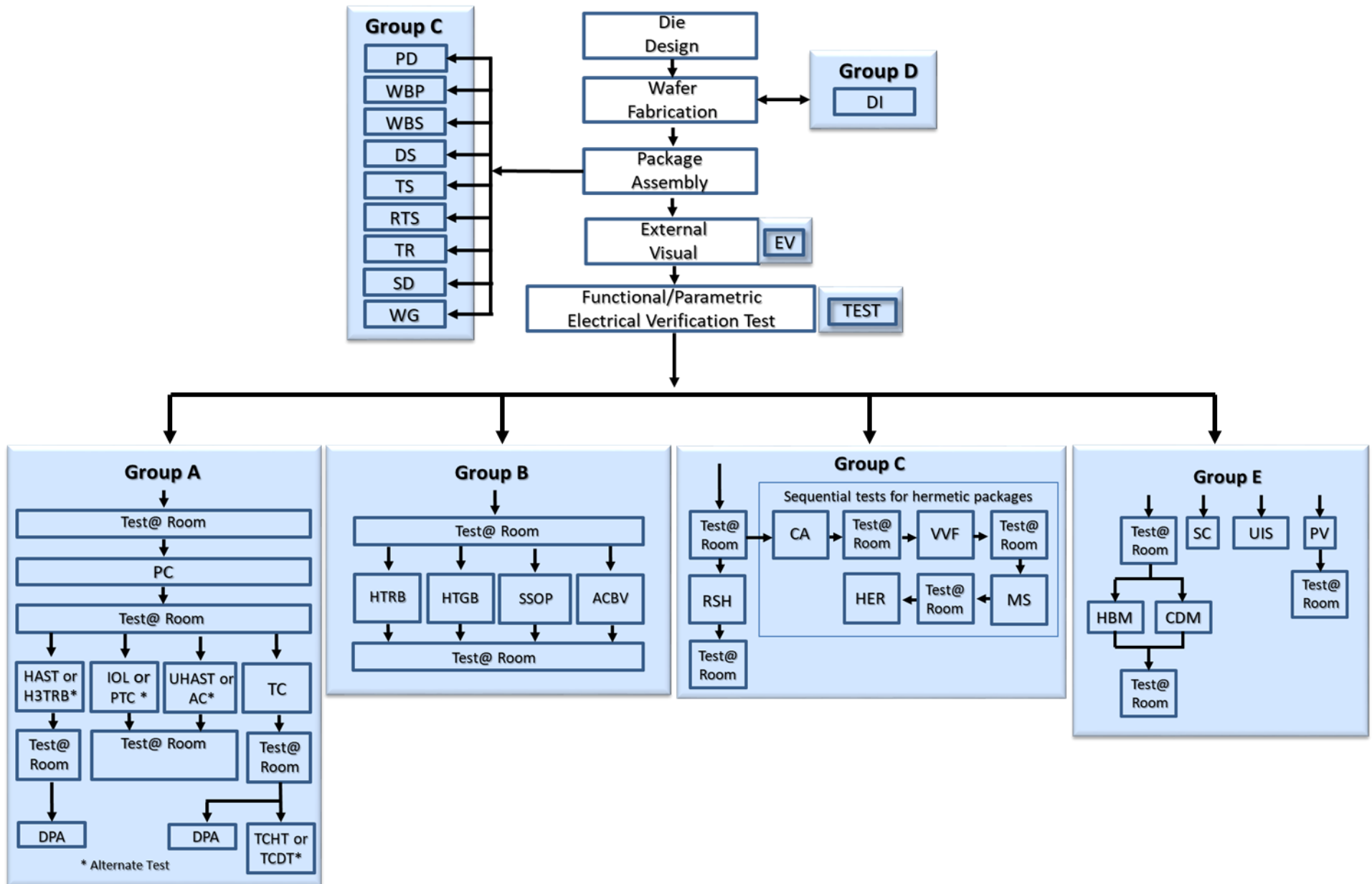


Figure 2: Q101 Stress Test Flowchart

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Table 2: Qualification Test Methods

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Pre-conditioning	PC	A1	1	G ₁ S	SMD qualification parts before Tests A2, A3, A4, A5 & C8		0 Fails	JEDEC/IPC J-STD-020 JESD22-A-113	Performed on surface mount parts (SMDs) prior to Tests A2, A3, A4, A5 & C8 only. TEST before and after PC. Any replacement of parts must be reported.
Highly Accelerated Stress Test	HAST	A2	1	D ₁ G ₁ U ₁ V ₁ 3	77	3 Note B	0 Fails	JEDEC JESD22-A-110	96 hours at T _A =130°C/85%RH, or 264hrs TA=110°C/85%RH with part reverse bias at 80% of rated voltage up to a voltage above which arcing in the chamber will likely occur (typically 42V). TEST before and after HAST.
High Humidity High Temp. Reverse Bias	H ³ TRB	A2 alt	1	D ₁ G ₁ U ₁ V ₁ 3	77	3 Note B	0 Fails	JEDEC JESD22-A-101	1000 hours at T _A = 85°C/85% RH with part reverse biased at 80% of rated breakdown voltage up to a maximum of 100V or limit of chamber. TEST before and after H3TRB as a minimum.
Unbiased HAST	UHAST	A3	1	D ₁ G ₁ U	77	3 Note B	0 Fails	JEDEC JESD22-A-118, or A101	96 hours at T _A =130°C/85%RH or 264 hours at TA=110°C/85%RH. TEST before and after UHAST.
Autoclave	AC	A3 alt	1	D ₁ G ₁ U	77	3 Note B	0 Fails	JEDEC JESD22-A-102	96 hours, T _A = 121°C, RH = 100%, 15psig. TEST before and after AC.
Temperature Cycling	TC	A4	1	D ₁ G ₁ U ₁ 3	77	3 Note B	0 Fails	JEDEC JESD22-A-104 Appendix 6	1000 cycles (T _A = minimum range of -55°C to maximum rated junction temperature, not to exceed 150°C). Can reduce duration to 400 cycles using T _A (max) = 25°C over part maximum rated junction temperature or using T _A (max) = 175°C if the maximum rated junction temperature is above 150°C. TEST before and after TC. See Section 2.4 for RDSon pass/fail limits.

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Table 2: Qualification Test Methods (continued)

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (continued)									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Temperature Cycling Hot Test	TCHT	A4a	1	D ₁ G ₁ U ₁ 1, 2	77	3 Note B	0 Fails	JEDEC JESD22-A-104 Appendix 6	125°C TEST after TC using PV-determined limits at hot, followed by decap and wire pull (Test C3 WBP) on all wires from 5 devices per appendix 6 for parts with internal bond wire sizes 5 mil diameter and less. (Samples may be a sub set of test A4).
TC Delamination Test	TCDT	A4a alt	1	D ₁ G ₁ U ₁ 1, 2	77	3 Note B	0 Fails	JEDEC JESD22-A-104 Appendix 6 J-STD-035	100% AM inspection after TC, followed by decap, inspection or wire pull (Test C3 WBS) on all wires from 5 parts per appendix 6 for 5 highest delaminated parts. If AM shows no delaminating, no decap, inspection and wire pull is required.
Intermittent Operational Life	IOL	A5	1	D ₁ G ₁ P ₁ T ₁ U ₁ W ₁ 3	77	3 Note B	0 Fails	MIL-STD-750 Method 1037	Tested per duration indicated in Table 2A. T _A =25°C. Parts powered to insure ΔT _J ≥ 100°C (not to exceed absolute maximum ratings). TEST before and after IOL as a minimum. See Section 2.4 for RDSon pass/fail limits.
Power Temperature Cycling	PTC	A5 alt	1	D ₁ G ₁ T ₁ U ₁ W	77	3 Note B	0 Fails	JEDEC JESD22-A-105	Perform PTC if ΔT _J ≥ 100°C cannot be achieved with IOL. Tested per duration indicated for Timing Requirements in Table 2A. Parts powered and chamber cycled to insure ΔT _J ≥ 100°C (not to exceed absolute maximum ratings). TEST before and after PTC as a minimum. See Section 2.4 for RDSon pass/fail limits.

NOTE: “alt” indicates an option to perform either/or of the same test number.

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Table 2: Qualification Test Methods (continued)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
High Temperature Reverse Bias	HTRB	<u>B1</u>	1	D ₁ G ₁ K ₁ P ₁ U ₁ V ₁ X ₁ 3	77	3 Note B	0 Fails	MIL-STD-750-1 M1038 condition A (for diodes, rectifiers and Zeners) M1039 condition A (for transistors)	1000 hours at the maximum specified DC Reverse Voltage while adjusting the junction temperature to avoid thermal runaway. Adjusting the ambient temperature T _A down from Ta(MAX) to compensate for current leakage and/or power dissipation is allowed. Bias should only be removed upon cool down to 30°C+/-5°C if there are relaxation effects for a given technology. When the maximum DC Reverse Voltage is not used, report the DC Reverse Voltage used during qualification. TEST before and after HTRB as a minimum. (See note X for HTRB.) Decap and wire pull on 5 parts after HTRB for bipolar and Schottky devices that are only utilizing bonding systems with dissimilar metals at the die (e.g., Au/Al). The bond should be stronger than the wire.
AC blocking voltage	ACBV	<u>B1a</u>	1	D ₁ G ₁ P ₁ U ₁ Y	77	3 Note B	0 Fails	MIL-STD-750-1 M1040 condition A	1000 hours at the maximum AC blocking voltage and junction temperature specified in the user/supplier specification. The ambient temperature T _A is to be adjusted to compensate for current leakage. TEST before and after ACPV as a minimum.
Steady State Operational	SSOP	<u>B1b</u>	1	D ₁ G ₁ O ₁ U	77	3 Note B	0 Fails	MIL-STD-750-1 M1038 condition B (Zeners)	1000 hours at rated IZ max, T _A to rated T _J , TEST before and after SSOP as a minimum.
High Temperature Gate Bias	HTGB	<u>B2</u>	1	D ₁ G ₁ M ₁ P ₁ U ₁ 3	77	3 Note B	0 Fails	JEDEC JESD22-A-108	1000 hours at the specified T _J (max) rating, with gate biased positive or negative (depending on the technology) at 100% of maximum gate voltage rating indicated in the detail specification with part biased OFF. Perform three lots of negative bias and three lots of positive bias for the initial qualification of a new technology, if appropriate. Can reduce duration to 500 hours through increasing T _J by 25°C, TEST before and after HTGB as a minimum. Decap and wire pull on 5 parts after HTGB for MOSFETs only that are utilizing bonding systems with dissimilar metals (e.g., Au/Al). The bond should be stronger than the wire.

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Table 2: Qualification Test Methods (continued)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Destructive Physical Analysis	DPA	<u>C1</u>	1	D ₁ G	2	1 Note B	0 <u>Fails</u>	AEC Q101-004 Section 4	Random sample of parts that have successfully completed H3TRB or HAST, and TC.
Physical Dimension	PD	<u>C2</u>	2	G, N	30	1	0 <u>Fails</u>	JEDEC JESD22-B-100	Verify physical dimensions to the applicable user part packaging specification for dimensions and tolerances.
Wire Bond <u>Pull</u> Strength	WBP	<u>C3</u>	3	D ₁ G ₁ E	10 bonds from min of 5 parts		0 <u>Fails</u>	MIL-STD-750-2 Method 2037 for Au and Al wire <u>AEC Q006 for Cu wire</u>	<u>Condition C or D. For Au wire diameter >1mil, minimum pull strength after TC = 3 grams. For Au wire diameter <1mil, refer to MIL-STD-750-2 Method 2037 as a guideline for minimum pull strength. For Au wire diameter <1mil, wire bond pull shall be performed with the hook over the ball bond and not at mid-wire.</u>
Wire Bond <u>Shear</u> Strength	WBS	<u>C4</u>	3	D ₁ G ₁ E			0 <u>Fails</u>	AEC Q101-003 <u>JESD22 B116</u>	See attached procedure for details on acceptance criteria and how to perform the test. <u>For Cu wire, refer to JESD22-B116 for shear criteria.</u>
Die Shear	DS	<u>C5</u>	3	D ₁ G	5	1	0 <u>Fails</u>	MIL-STD-750-2 Method 2017	<u>Also required for Pre- & Post-process change comparison to evaluate process change robustness related to die attach per Table 3 guidelines for test C5.</u>
Terminal Strength	TS	<u>C6</u>	2	D ₁ G ₁ L	30	1	0 <u>Fails</u>	MIL-STD-750-2 Method 2036	Evaluate lead integrity of <u>through-hole</u> leaded parts only.
Resistance to Solvents	RTS	<u>C7</u>	2	D ₁ G	30	1	0 <u>Fails</u>	JEDEC JESD22-B-107	Verify marking permanency. (Not required for laser etched parts or parts with no marking.)
Resistance to Solder Heat	RSH	<u>C8</u>	2	D ₁ G	30	1	0 <u>Fails</u>	<u>JEDEC JESD22-A-111 (SMD), or B-106 (PTH)</u>	TEST before and after RSH. SMD parts shall be fully submerged during test and preconditioned per MSL rating.
Thermal Resistance	TR	<u>C9</u>	3	D ₁ G	10	1	0 <u>Fails</u>	JEDEC JESD24-3, 24-4, 24-6 as appropriate	<u>Also required for Pre- & Post-process change comparison to evaluate process change robustness per Table 3 guidelines for test C9. Measure TR to assure specification compliance and provide process change comparison data.</u>

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Table 2: Qualification Test Methods (continued)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS (continued)									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Solderability	SD	<u>C10</u>	2	D ₁ G	10	1 Note B	0 <u>Fails</u>	JEDEC J-STD-002	Magnification 50x, Reference solder conditions in Table 2B. Apply test method A for through-hole, or both test methods B and D for SMD.
<u>Whisker Growth Evaluation</u>	<u>WG</u>	<u>C11</u>	3		-	-	-	AEC-Q005	For whisker requirements. Test to be done on a family basis (plating metallization, lead configuration).
Constant Acceleration	CA	<u>C12</u>	2	D ₁ G ₁ H ₁ (1)	30	1 Note B	0 <u>Fails</u>	MIL-STD-750-2 Method 2006	Y1 plane only, 15k g-force. TEST before and after CA.
Vibration Variable Frequency	VVF	<u>C13</u>	2	D ₁ G ₁ H ₁ (2)	Items <u>C12</u> through <u>C15</u> are sequential tests for hermetic packages. (See note H on Legend page.)			JEDEC JESD2-B-103	Use a constant displacement of 0.06 inches (double amplitude) over the range of 20Hz to 100 Hz and a 50g constant peak acceleration over the range of 100 Hz to 2 KHz. TEST before and after VVF.
Mechanical Shock	MS	<u>C14</u>	2	D ₁ G ₁ H ₁ (3)				JEDEC JESD22-B-104	1500 g's for 0.5mS, 5 blows, 3 orientations. TEST before and after MS.
Hermeticity	HER	<u>C15</u>	2	D ₁ G ₁ H ₁ (4)				JEDEC JESD22-A-109	Fine and Gross leak test per individual user specification.
TEST GROUP D – DIE FABRICATION RELIABILITY TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Dielectric Integrity	DI	<u>D1</u>	3	D ₁ M	5	1	0 <u>Fails</u>	AEC Q101-004 Section 3	All parts must exceed gate breakdown voltage minimum (Power MOS & IGBT only). Also required for Pre- & Post-process change comparison to evaluate process change robustness related to the dielectric material per Table 3 guidelines for test D1.

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Table 2: Qualification Test Methods (continued)

TEST GROUP E – ELECTRICAL VERIFICATION TESTS									
STRESS	ABV	#	DATA TYPE	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
External Visual	EV	E0	1	G ₁ N	All qualification parts submitted for testing		0 Fails	JEDEC JESD22-B101	Inspect part construction, marking and workmanship.
Pre- and Post-Stress Electrical Test	TEST	E1	1	G ₁ N	All qualification parts tested per the requirements of the appropriate part specification.		0 Fails	User specification or supplier's standard specification	Test is performed as specified in the applicable stress reference at room temperature.
Parametric Verification	PV	E2	1	N	25	3 Note A	-	Individual AEC user specification	Test all parameters according to user specification over the <u>part</u> temperature range to insure specification compliance.
<u>ESD HBM Characterization</u>	<u>ESDH</u>	<u>E3</u>	1	D ₁ W	30 HBM	1	=	AEC Q101-001	<u>TEST before and after ESD.</u>
<u>ESD CDM Characterization</u>	<u>ESDC</u>	<u>E4</u>	2	D ₁ W	30 CDM	1	=	AEC Q101-005	If applicable, the supplier must document that a <u>small package</u> could not hold sufficient charge to perform the test. TEST before and after ESD.
Unclamped Inductive Switching	UIS	E5	3	D	5	1	0 Fails	AEC Q101-004 Section 2	<u>Also required for Pre- & Post-process change comparison to evaluate process change robustness per Table 3 guidelines for test E5.</u> (Power MOS and internally clamped IGBTs only).
Short Circuit Characterization	SC	E6	3	D ₁ P	10	3 Note B	0 Fails	AEC Q101-006	For smart power parts only.

* **Note:** All electrical testing before and after the qualification stresses (including pre-conditioning) are performed to the limits detailed in the individual user specification at room temperature only. For generic qualifications, the supplier's standard specification limits at room temperature may be used.

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LEGEND FOR TABLE 2

Notes:

- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify an acceptable number of lots were used.
- B Where generic (family) data is provided in lieu of component specific data, 3 lots of generic and/or part-specific data are required.
- D Destructive test, parts are not to be reused for qualification or production.
- E Ensure that each size wire is represented in the sample size.
- G Generic data allowed. See Section 2.3.
- H Required for hermetic packaged parts only. Items #16 through #19 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- K Not applicable to Voltage Stabilizers (Zeners)
- L Required for leaded parts only.
- M Required for MOS & IGBT parts only.
- N Nondestructive test, parts can be used to populate other tests or they can be used for production.
- O Required for Voltage Stabilizers (Zeners) only.
- P Consideration should be made for whether this test is to be applied to a Smart Power part or substituted with an equivalent Q100 test. Elements for consideration include the amount of logic/sensing on the die, intended user application, switching speed, power dissipation, and pin count.
- S Required for surface mount parts only.
- T When testing diodes under Intermittent Op Life conditions the 100 degree junction temperature delta may not be achievable. Should this condition exist, a Power Temperature Cycling (A5 alt) test shall be used in place of Intermittent Operational Life (A5) test to ensure the proper junction temperature changes occur. All other parts should use IOL.
- U For these tests only, it is acceptable to use unformed leaded packages (e.g., IPAK) to qualify new die going in the equivalent package (e.g., DPAK) provided the die size is within the range of sizes qualified for the equivalent package.
- V For bi-directional Transient Voltage Suppressor (TVS) devices, one-half the test duration in each direction shall be performed.
- W Not required for Transient Voltage Suppressor (TVS) parts. For TVS parts, PV data in Section 4.2 will be after 100% Peak Pulse Power (Pppm) has been performed to rated Ippm current.
- X For switching parts (e.g., fast/ultrafast rectifiers, Schottkys) the rated junction temperature specified in the user/supplier specifications refers to a switch mode application condition. For those parts that can experience thermal runaway in HTRB using a DC reverse condition on a switch mode part, the maximum rated junction temperature at the rated DC Reverse Voltage may not be specified in the user/supplier specification and those test conditions should be stated in the qualification test plan/report. Example: for a 100V Schottky part; 100V would be applied with T_A adjusted to maximum T_J capability without driving part into thermal runaway, Voltage, T_A and T_J achieved would be reported as test conditions in the qualification test plan/report.
- Y Required for Thyristors only.
- 1 Required for MOSFETs parts with internal bond wire sizes 5 mil diameter and less.
- 2 Tests A4A and A4Aalt are not executed on Cu wire bonded products. Instead, follow the requirements in AEC-Q006.
- 3 Follow the requirements in AEC-Q006 for parts being qualified with Cu wire.

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Table 2A: Timing Requirements for Intermittent Operational Life (Test A5) or Power Temperature Cycling (Test A5alt)

Package Type	Number of Cycles Required $\Delta T_J \geq 100^\circ\text{C}$	Number of Cycles Required $\Delta T_J \geq 125^\circ\text{C}$	Time per cycle
All	60,000/(x+y) 15,000 cycles	30,000/(x+y) 7,500 cycles	Fastest capable (minimum 2 min. on/off) x min. on + y min. off

Example 1: A package capable of 2 minutes on/4 minutes off would require 10,000 cycles [60,000/(2+4)] at $\Delta T_J \geq 100^\circ\text{C}$ or 5,000 cycles at $\Delta T_J \geq 125^\circ\text{C}$.

Example 2: A package capable of 1 minute on/1 minute off would require 15,000 cycles at $\Delta T_J \geq 100^\circ\text{C}$ or 7,500 cycles at $\Delta T_J \geq 125^\circ\text{C}$.

X = the minimum amount of time it takes for the part to reach the required ΔT_J from ambient temperature.

Y = the minimum amount of time it takes for the part to cool to ambient temperature from the required ΔT_J .

The method of instrumentation, part mounting and heat sinking on the test board will influence x and y per package.

Table 2B: Solderability Requirements (Test C10) for SnPb Plated Terminations per J-STD-002

Type	Test Method	Solder Temperature	Steam Age Category
Leaded Through-Hole	<u>A or A1</u>	<u>245+/-5°C reflow:</u> <u>215+/-5°C Pb-free</u> <u>backward compatibility</u>	<u>C or E</u>
SMD Standard Process	<u>S or S1</u>	<u>215-230°C</u>	<u>C or E</u>
SMD Dissolution of Metals test	D	<u>260+/-5°C</u>	<u>C or E</u>

* **Note:** Refer to AEC-Q005 Pb-Free Test Requirements for solderability requirements of Pb-free terminated parts.

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Appendix 1: Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. There must be valid and obvious links between the data and the subject of qualification.

For parts to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. For each qualification test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by rationale clearly detailing similarity). All parts using the same process and materials are to be categorized in the same qualification family for that process and are acceptable by association when one family member successfully completes qualification with the exception of the device specific requirements of Section 4.2.

Prior qualification data obtained from a part in a specific family may be extended to the qualification of subsequent parts in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g., site, material(s), process(es)), refer to Section 2.3 that allows for the selection of worst-case test vehicles to cover all the possible permutations.

A1.1 Fab Process

Each process technology (e.g., Power MOS, Bipolar, Zener, etc.) must be considered and subjected to stress-test qualification separately. No matter how similar, processes from one fundamental fab technology cannot be used for the other.

Family requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

A1.1.1 Wafer Fab Technology

- Power MOS
- Small Signal MOS
- Power Bipolar
- Small Signal Bipolar
- IGBT
- Rectifier
- Ultrafast Rectifier
- Schottky Rectifier
- Zener
- Transient Voltage Suppressor
- Pin
- Varactor
- Germanium
- Gallium Arsenide
- SCRs

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A1.1.2 Wafer Fab Process - consisting of the same attributes listed below:

- Process flow
- Layout design rules
- Number of masks
- Cell Density (where applicable)
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Doping process (e.g., diffusion vs. ion implantation)
- Passivation/Glassivation material and thickness range
- Oxidation process and thickness range (for gate and field oxides)
- Front/back metallization material, thickness range and number of levels

A1.1.3 Wafer Fab Site

A1.1.4 Example:

3 lots of a FAB family in any package outline for the following Qualification tests:

- HTRB
- HTGB
- H3TRB / HAST

Example:

For a given FAB family of Gold doped fast efficient rectifiers with a NiAu metal:

An axial-leaded 1A, 200V, 50mil² die size part
A surface mount 3A, 100V, 100mil² die size part
A through-hole TO-247, 30A, 600V, 135 mil² die size part

All 3 of these for the 3 tests above would constitute the requirement as 3 die sizes within the same FAB family under the same process controls.

A1.2 Assembly Process

The processes for each package type must be considered and subjected to stress-test qualification separately. For parts to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user(s) to support the acceptance of generic data with package type, die sizes, paddle sizes and die aspect ratios different than the device being considered for stress-test qualification. The important attributes defining a qualification family are listed below:

A1.2.1 Package Type (e.g. TO-220, SOT-23, DO-41, SOIC, etc.)

- Range of paddle (flag) size qualified for the die size/aspect ratio under consideration.

A1.2.2 Assembly Process - consisting of the same attributes listed below:

- Leadframe base material
- Leadframe plating (internal and external to the package)
- Die attach material/method
- Wire bond material, wire diameter, and process
- Plastic mold compound or other encapsulation material

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A1.2.3 Assembly Site

A1.2.4 Example

3 lots of a package family using any die structure that has the same die backside metallization will suffice for the following Qualification tests. It is highly desirable that two of the lots come from the maximum and minimum die size allowed by the package design rules.

- IOL / PTC
- TC
- AC / UHST
- H3TRB / HAST

A1.3 Qualification of Multiple Families and Sites

When the specific product or process attribute to be qualified or re-qualified (i.e., via process, material or site change) will affect more than one wafer fab family or assembly family, the qualification test vehicles should be three lots of a single part type from each of the technology and package families that are projected to be most sensitive to the changed attribute with sample sizes split to include a minimum of 30 pieces from each of 3 assembly lots from each assembly / fab site.

Below is the recommended process for qualifying changes across many process and product families:

- a. Identify all products affected by the proposed process changes.
- b. Identify the critical structures and interfaces potentially affected by the proposed change.
- c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Conduct a risk assessment into potential failure mechanisms. Note that steps (a) to (c) are equivalent to the creation of an FMEA.
- d. Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and device sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.
- e. Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.
- f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

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Appendix 2: Certification of Design, Construction and Qualification

Supplier Name:

Date:

The following information is required to identify a part that has met the requirements of AEC-Q101. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at <http://www.aecouncil.com>.

**This template is available as a stand-alone document that can be downloaded at
<http://www.aecouncil.com>**

Item Name	Supplier Response
1. User's Part Number:	
2. Supplier Part Number/Generic Part Number:	
3. Device Description:	
4. Wafer/Die Fab Location & Process ID: a. Facility name/plant #: b. Street address: c. Country:	
5. Wafer Probe Location: a. Facility name/plant #: b. Street address: c. Country:	
6. Assembly Location & Process ID: a. Facility name/plant #: b. Street address: c. Country:	
7. Final Quality Control A (Test) Location: a. Facility name/plant #: b. Street address: c. Country:	
8. Wafer/Die: a. Wafer size: b. Die family: c. Die mask set revision & name:	
9. Wafer/Die Technology Description: a. Wafer/Die process technology: b. Gate oxide thickness (MOSFETs only): c. Number of mask steps:	
10. Die Dimensions: a. Die width: b. Die length: c. Die thickness (finished):	
11. Die (frontside) Metallization: a. Die metallization material(s): b. Number of layers: c. Thickness (per layer): d. % of alloys (if present):	
12. Die Passivation: a. Number of passivation layers: b. Die passivation material(s): c. Thickness(es) & tolerances:	

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13. Die Overcoat Material (e.g., Polyimide):	
14. Die Prep Backside: a. Die prep method: b. Die metallization: c. Thickness(es) & tolerances:	
15. Die Separation Method: a. Kerf width (μm): b. Kerf depth (if not 100% saw): c. Saw method:	Single <input type="checkbox"/> Dual <input type="checkbox"/>
16. Die Attach: a. Die attach material ID: b. Die attach method: c. Die placement diagram:	See attached <input type="checkbox"/> Not available <input type="checkbox"/>
17. Package: a. Type of package (e.g., plastic, ceramic, unpackaged): b. JEDEC designation (e.g. MS029, MS034, etc.):	
18. Mold Compound: a. Mold compound supplier & ID: b. Mold compound type: c. Flammability rating: d. Fire Retardant type/composition: e. Tg (glass transition temperature)($^{\circ}\text{C}$): f. CTE (above & below Tg)(ppm/ $^{\circ}\text{C}$):	UL 94 V1 <input type="checkbox"/> UL 94 V0 <input type="checkbox"/> CTE1 (below Tg) = _____ CTE2 (above Tg) = _____
19. Wire Bond: a. Wire bond material: b. Wire bond diameter (mils): c. Type of wire bond at die: d. Type of wire bond at leadframe: e. Number of bonds over active area:	
20. Leadframe (if applicable): a. Header material: b. Header width (mils): c. Header length (mils): d. Header plating composition: e. Header plating thickness (μinch): f. Leadframe material: g. Leadframe bonding plating composition: h. Leadframe bonding plating thickness (μinch): i. External lead plating composition: j. External lead plating thickness (μinch):	
21. Thermal Resistance: a. θ_{JA} $^{\circ}\text{C}/\text{W}$ (approx.): b. θ_{JC} $^{\circ}\text{C}/\text{W}$ (approx.): c. θ_{JL} junction-to-lead $^{\circ}\text{C}/\text{W}$ (approx.): d. θ_{JM} junction-to-mounting base $^{\circ}\text{C}/\text{W}$ (approx.):	

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<p>22. Maximum Process Exposure Conditions:</p> <p style="margin-left: 20px;">a. MSL @ rated SnPb temperature: b. MSL @ rated Pb-free temperature:</p>	<p><i>* Note: Temperatures are as measured on the center of the plastic package body top surface.</i></p> <p style="margin-left: 20px;">_____ at _____ °C (SnPb) _____ at _____ °C (Pb-free)</p>
<p><u>Attachments:</u></p> <p>Die Photo <input type="checkbox"/></p> <p>Package Outline Drawing <input type="checkbox"/></p> <p>Die Cross-Section Photo/Drawing <input type="checkbox"/></p> <p>Wire Bonding Diagram <input type="checkbox"/></p> <p>Die Placement Diagram <input type="checkbox"/></p>	<p><u>Requirements:</u></p> <p>1. A separate Certification of Design, Construction & Qualification must be submitted for each <u>part number</u>, wafer fab, and assembly location.</p> <p>2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below.</p>
<p>Completed by: _____ Date: _____</p>	<p>Certified by: _____ Date: _____</p>
<p>Typed or Printed: Signature: Title:</p>	Signature area for certifier

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Appendix 3: Qualification Test Plan

The supplier is requested to complete and submit the Discrete Semiconductor Qualification Test Plan as part of the pre-launch Control Plan whenever qualification submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where "family" data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this specification. An approved copy of the Qualification Test Plan shall be included with each qualification submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix 1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Test Plan Form, found on the AEC website, should be used. In this case, a bipolar discrete part was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site etc. This example is shown for illustration purposes only and should not limit any requirements from Table 1 herein.

Page 1 of 1		Discrete Semiconductor Component Qualification Plan					Rev: E 12/13/19	
User P/N: N611045BFDAARA		User Component Engineer: John Doe						
User Spec. #: ES-N611045BFDAARA		General Specification: AEC-Q101						
Supplier: Sam's Discount Semiconductors (SDS)		Supplier Manufacturing Site: Shanghai, China						
Supplier Generic P/N: PZT3904		Required PPAP Submission Date: 7/1/2019						
Supplier Internal P/N: SDF-3417-AR		Family Type: Bipolar SOT-223, 20 mil square die						
Reason for Qual: New device qualification								
Item	Test	Test Conditions	Exceptions	Est. Start	Est. Comp.	# Lots	S. S.	Remarks
1	TEST	Electrical Characterization @ 25C		4/1/2019	4/5/2019	all	all	
2	Preconditioning	per AEC-Q101		4/8/2019	4/10/2019	all	all	
3	External Visual	per AEC-Q101		4/11/2019	4/12/2019	all	all	
4	Parametric Verification	Characterization @ -55, 25, & 150C		4/15/2019	4/19/2019	3	30	
5	HTRB	Reverse biased @ 64V		4/22/2019	6/24/2019	3	77	
6	HTGB		N/A Bipolar device					
7	Temperture Cycling		Use attached generic data forthis package related test.					generic data uses -65/150C (rather than -55C)
8	Autoclave	Ta = 121C, P = 15PSIG, RH = 100%	Use attached generic data forthis package related test.					
9	H3TRB	Reverse biased @ 64V		4/22/2019	6/24/2019	3	77	
10	IOL		T on/off = 2 minutes, 15,000 cycles	4/22/2019	6/24/2019	3	77	SDS internal standard
11	ESD	per AEC-Q101		4/22/2019	6/24/2019	1	30	
12	DPA	per AEC-Q101		6/24/2019	6/24/2019	3	2	2 ea from H3TRB and TC only.
Comments:								
1. Supplier requests 1 lot qualification of this device type in addition to attached rel reports to similar parts to total 3 lots. Rel Report #23-602 (PZT3906, the PNP compliment of this part) and #23-665 (PZTA62 NPN Darlington with larger 35 MIL die)								
2. In addition, the die is qualified in SOT-23 version of this device, the SOT-223 package is qualified with larger (35 MIL) bipolar die (N611002BFDAARA & N611007BFDBARA).								
3. Attached quarterly reliability results for 2017 & 2018 on generic PZT3904.								
4. These devices all share the same wafer and assembly processes.								
5. Tests 14-23 covered by annual SOT-223 packaging qual last approved 11/18.								
Prepared by (supplier):				Approved by (User):				
Typed/Printed				Typed/Printed				
Signature				Signature				
Title				Title				

* Note: This plan is only an example and does not represent all the required tests in this document.

Figure A3.1: Example of Discrete Semiconductor Qualification Test Plan

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Appendix 4: Data Presentation Format

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Discrete Semiconductor PPAP submittal. Figure A4.1 is an example of a completed Environmental Test Summary. Figure A4.2 is an example of a completed Parametric Verification Summary. The format of both summaries shall be followed. Soft copies of the formats may be found on the AEC website or is available upon request. Other equivalent formats are acceptable if approved by the user.

Supplier		User Part Number			
Sam's Discount Semiconductors		N611045BFDAARA			
Name of Laboratory		Part Description			
SDS Qual Lab		Bipolar SOT-223 Transistor			
Test #	Test Description	Test Conditions	# Lots	# Tested	# Failed
2	Preconditioning	Per Spec	3	77	0
3	External Visual	Per Spec	3	381	0
5	HTRB	Reverse Biased @ 64V; Tj = 150C	3	77	0
9	H3TRB	Reverse Biased @ 64V; 85C/85%RH	3	77	0
10	IOL	T on/off = 2 min, 15K Cycles	1	77	0
11	ESD	Per Spec	1	30	N/A
12	DPA	Per Spec	3	2	0

* **Note:** This listing of test results is only an example and does not represent all the tests in this document.

Figure A4.1: Environmental Test Summary Example

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Supplier Sam's Discount Semiconductors			User Part Number N611045BFDAARA					
Lot Number JB-117A (Test Lot 2)			Temperature 25 Degrees C					
Test Name	Unit	Spec LSL	Spec USL	MIN	MAX	MEAN	STD.DEV.	Cpk
BV _{CEO}	V	40	-	46.3	54.2	49.4	1.1	1.45
BV _{CBO}	V	60	-	65.7	73.9	69.4	1.21	1.7
BV _{EBO}	V	6	-	6.7	8.3	7.2	0.9	1.64
I _{BL}	nA	-	50	0.15	37.2	24.2	0.2	10.2
I _{CEX}	nA	-	50	0.02	12.3	8.7	0.45	9.8
h _{FE1}	--	40	-	45.6	93.2	72.3	6.7	1.8
h _{FE2}	--	70	-	71.7	114.2	96.2	5.2	2.01
h _{FE3}	--	100	300	103.2	294.4	187.3	19.1	2.7
h _{FE4}	--	60	-	78.7	114.3	98.7	3.7	1.95
h _{FE5}	--	30	-	37.2	46.2	41.2	0.9	2.7
V _{CESAT1}	V	-	0.2	0.07	0.17	0.12	0.011	1.81
V _{CESAT2}	V	-	0.3	0.16	0.25	0.21	0.01	1.41
V _{BESAT1}	V	0.65	0.85	0.71	0.81	0.76	0.01	2
V _{BESAT2}	V	-	0.95	0.56	0.86	0.63	0.015	3.7
f _T	MHz	300	-	463	587	505	12	1.72
C _{OBO}	pF	-	4	2.7	3.6	3.13	0.15	2.1
C _{IBO}	pF	-	8	2.6	4.5	3.25	0.2	2.2
h _{IE}	Kohm	1	10	2.3	4.6	3.7	0.2	1.8
h _{RE}	10 ⁻⁴	0.5	8	0.79	1.57	1.23	0.13	1.83
h _{fe}	--	100	400	214	363	303	9	3.8

Figure A4.2: Parametric Verification Summary Example

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Appendix 5: Minimum Parametric Test Requirements

For Table 1 Test E1 (Pre- & Post-Stress Electrical Test), the following electrical parameters shall be used (as a minimum):

Transistors

<u>Bipolar</u>	<u>FET</u>	<u>IGBT</u>
BV_{CEX}	BV_{DSS}	BV_{CES}
I_{CEX}	I_{DSS}	I_{CES}
I_{EBX} or I_{CBX}	I_{GSS}	I_{GES}
$V_{CE(SAT)}$	$R_{DS(ON)}$	$V_{CE(SAT)}$
h_{FE}	G_{fs} (if specified)	h_{FE}
	$V_{GS(th)}$ or $V_{GS(OFF)}$	$V_{GE(th)}$

Diodes

V_F , I_R , V_{BR} (Diodes)
 V_Z or V_{CLAMP} (Zeners)
 R_F (PIN Diode, if applicable)

Varactors

I_R , C_T

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Appendix 6: Plastic Package Opening for Wire Bond Testing, and Inspection

A6.1 Purpose

The purpose of this Appendix is to define a guideline for opening plastic packaged devices so that reliable wire pull or bond shear results will be obtained. This method is intended for use in opening plastic packaged devices to perform wire pull testing after temperature cycle testing or for bond shear testing.

A6.2 Materials and Equipment

A6.2.1 Etchants

Various chemical strippers and acids may be used to open the package dependent on your experience with these materials in removing plastic molding compounds. Red Fuming Nitric Acid has demonstrated that it can perform this function very well on novolac type epoxies, but other materials may be utilized if they have shown a low probability for damaging the bond pad material.

For some part designs (i.e., green compound molded), etching by red fuming Nitric acid and sulfuric acid will etch Al wire/Al pad in high temperature. The process will damage 5mil Al (including below 5mil).

Room temperature etchants should be used where possible.

A6.2.2 Plasma Strippers

Various suitable plasma stripping equipment can be utilized to remove the plastic package material.

A6.3 Plastic Package Opening Procedure for Wire Bond Testing

- a. Using a suitable end mill type tool or dental drill, create a small impression just a little larger than the chip in the top of the plastic package. The depth of the impression should be as deep as practical without damaging the loop in the bond wires.
- b. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, and at least 75% of the bond wire length.

Caution: Do not expose the wire bond at the leadframe. These bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible.

* **Note:** For some part designs, especially for small packages, mounting the part may be required to ensure the structural integrity of the package during the package opening process and wire pull testing.

- c. Using suitable magnification, inspect the bond pad areas on the chip to determine if the package removal process has significantly attacked the bond pad metallization. If a bond pad shows areas of missing metallization, the pad has been degraded and shall not be used for bond shear or wire pull testing. Bond pads that do not show attack can be used for wire bond testing.

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A6.4 Plastic Package Opening Procedure for Wire Bond Inspection after Temperature Cycling

- a. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, the bond wire length, and the wire bond at the leadframe.

Caution: Care must be taken when exposing leadframe wire bonds. These bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible.

* **Note:** For some part designs, especially for small packages, mounting the part may be required to ensure the structural integrity of the package during the package opening process and wire pull testing.

- b. Using suitable magnification, inspect the bonds for damage from Temp cycle delamination.

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Appendix 7: AEC-Q101 and the Use of Mission Profiles

A7.1 SCOPE

Successful completion of the test requirements in Table 2 allows the claim to be made that the part is AEC Q101 qualified. Additional testing may be agreed between Component Manufactures and Tier 1 Component Users depending on more demanding application environments. To address these more stringent conditions, application based Mission Profiles may be used for a reliability capability assessment.

A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime.

A7.1.1 Purpose

This appendix provides information on an approach that can be used to assess the suitability of a component for a given application and its mission profile for unique requirements. The benefit of applying this approach is that, in the end, the reliability margin between the component (specification) space and the application (condition) space may be shown.

- Section A7.2 demonstrates the relation between AEC-Q101 stress conditions / durations and a typical example of a set of use life time and loading conditions.
- Section A7.3 describes the approach, supported by flow charts that can be used for a reliability capability assessment starting from a mission profile description.

A7.1.2 References

- **SAE J1879/J1211/ZVEI** Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
- **JEDEC JEP122** Failure Mechanisms and Models for Semiconductor Devices

A7.2 BASE CONSIDERATIONS

A7.2.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are an example used for demonstration purpose only. Many typical mission profiles will differ in one or more characteristics from what is shown below.

- service lifetime in years
- engine on-time in hours
- engine off time { idle} in hours
- non-operating time in hours
- number of engine on-off cycles
- service mileage

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other forms of loading under use conditions, to the above lifetime characteristics. Examples of these and how they relate to the test conditions in Table 2 are shown in Table A7.1.

A7.2.2 Relation to AEC-Q101 Stress Test Conditions and Durations

The basic calculations in Table A7.1 for each of the major stress tests demonstrate how one can derive suitable test conditions for lifetime characteristics based on reasonable assumptions for the loading. Caution should always be taken on use of excessive test conditions beyond those in Table 2, because they may induce unrealistic fail mechanisms and/ or acceleration.

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A7.3 METHOD TO ASSESS A MISSION PROFILE

This section demonstrates how to perform a more detailed reliability capability assessment in cases where the application differs significantly from existing and proven situations:

- Application has a demanding loading profile
- Application has an extended service lifetime requirement
- Application has a more stringent failure rate target over lifetime

These considerations may result in extended test durations. In addition, there may be components manufactured in new technologies and/or containing new materials that are not yet qualified. In such cases, unknown failure mechanisms may occur with different times-to-failure which may require different test methods and/or conditions and/or durations.

For these cases, two flow charts are available to facilitate both Tier 1 and Component Manufacturing in a reliability capability assessment:

- Flow Chart 1 in Figure A7.1, describes the process at Component Manufacturer to assess whether a new component can be qualified by AEC-Q101.
- Flow Chart 2 in Figure A7.2, describes (1) the process at Tier 1 to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at Component Manufacturer to assess whether an existing component qualified according to AEC-Q101 can be used in a new application.

For details on how to apply this method, please refer to SAE J1879, SAE J1211 and/or ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

In summary, the flow charts result in the following three clear possible conclusions:

- a. AEC-Q101 test conditions do apply.
- b. Mission Profile specific test conditions may apply.
- c. Robustness Validation may be applied with detailed alignment between Tier1 and Component Manufacturer.

In addition, not shown in the flow charts, the expected end of life failure rate may be an important criterion. Regarding failure rates, the following points should be considered:

- No fails in 231 devices (77 devices from 3 lots) are applied as pass criteria for the major environmental stress tests. This represents an LTPD (Lot Tolerance Percent Defective) = 1, meaning a maximum of 1% failures at 90% confidence level.
- This sample size is sufficient to identify intrinsic design, construction and/or material issues affecting performance.
- This sample size is NOT sufficient or intended for process control or PPM evaluation. Manufacturing variation failures (low ppm issues) are achieved through proper process controls and/or screens such as described in AEC-Q001 and -Q002.
- Three lots are used as a minimal assurance of some process variation between lots. A monitoring process has to be installed to keep process variations under control.
- Sample sizes are limited by part and test facility costs, qualification test duration and limitations in batch size per test.

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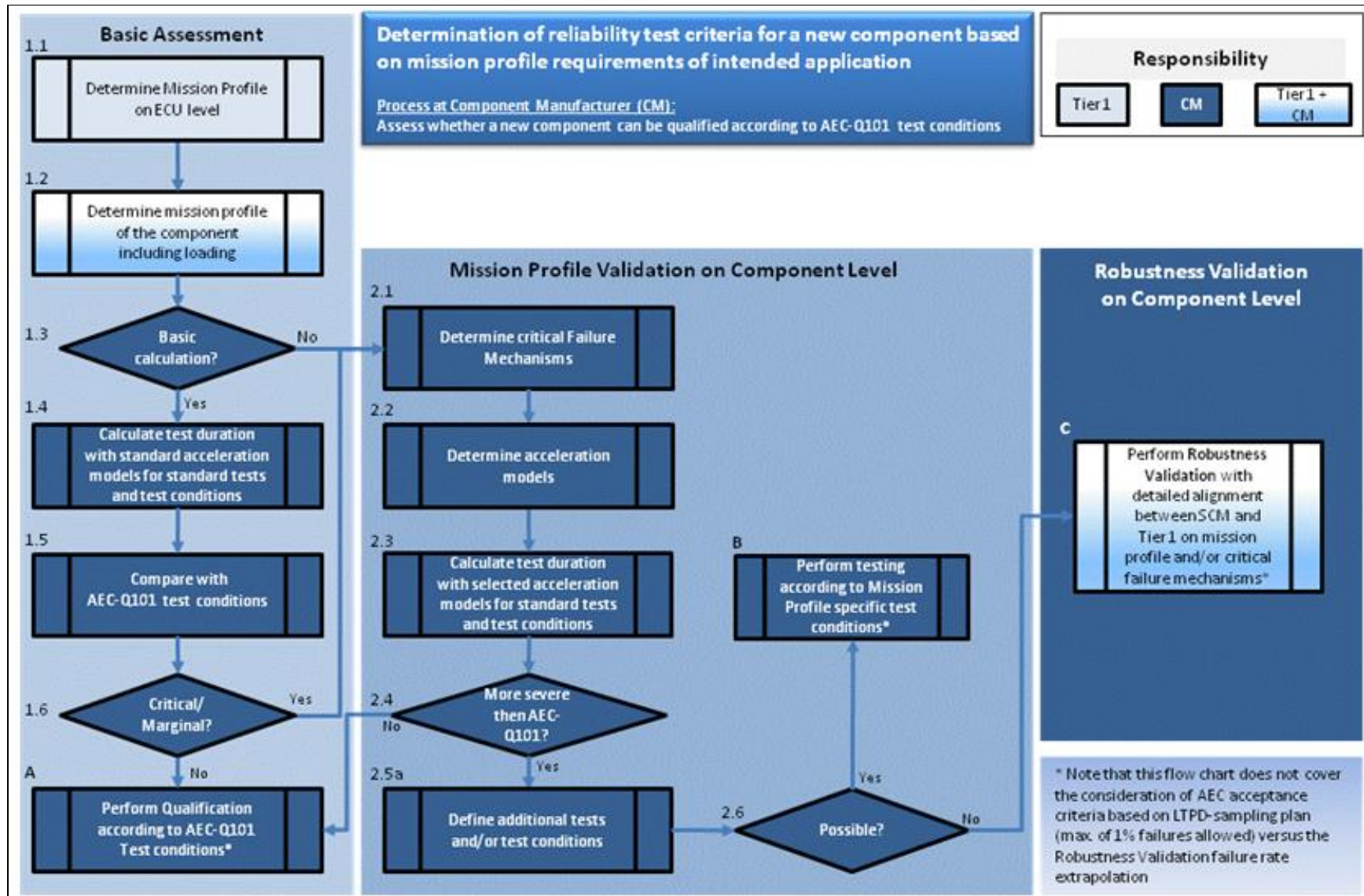


Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component

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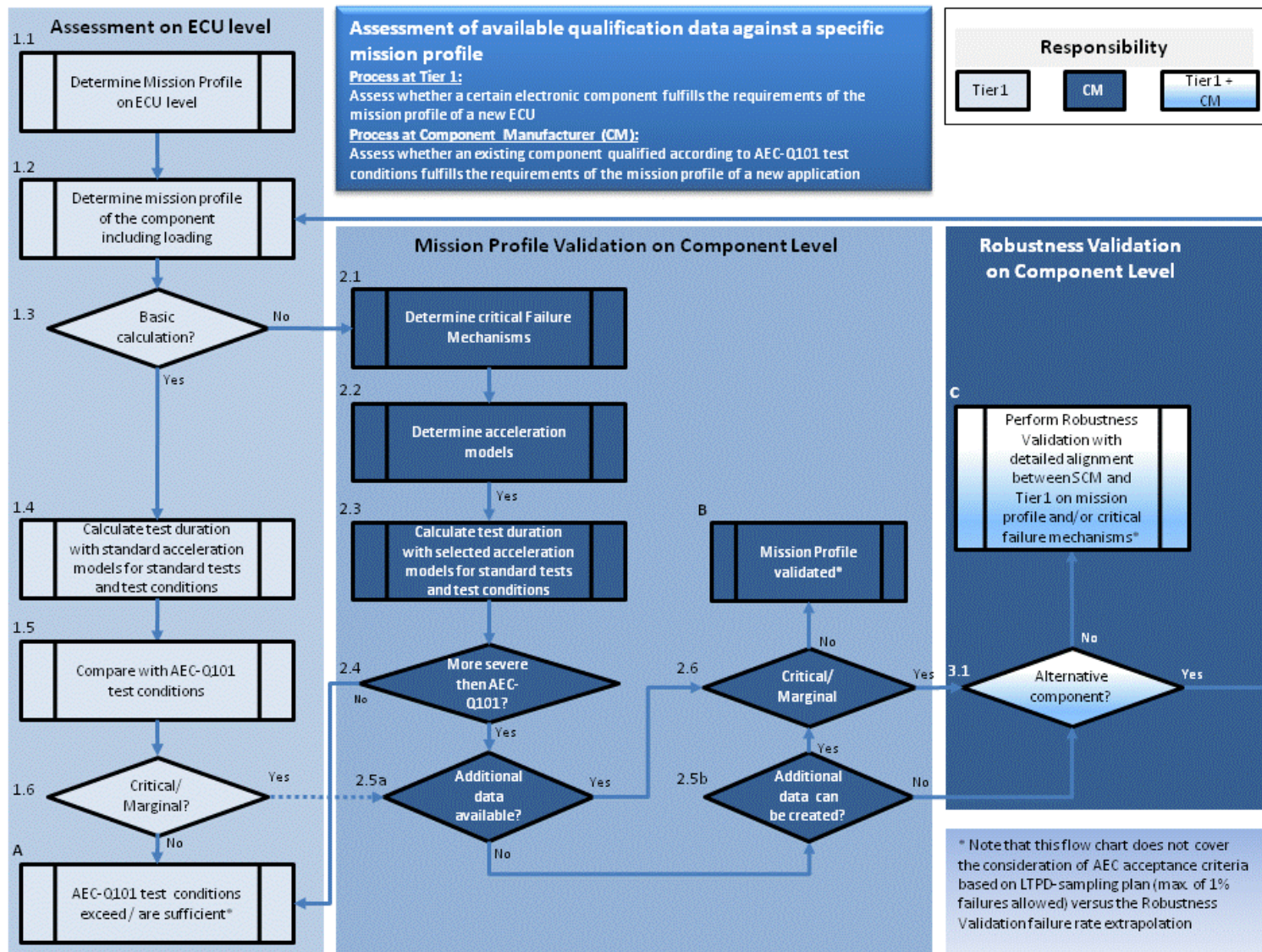


Figure A7.2: Flow Chart 2 – Assessment of Existing, Qualified Component

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Table A7.1: Basic Calculations for AEC-Q101 Stress Test Conditions and Durations

Loading	Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in °C) (K = °C + 273)	Model Parameters	Calculated Test Duration	Q101 Test Duration
Operation	<p>$t_u = 12,000$ h (average <u>operating use</u> time over 15 <u>years</u>)</p> <p>$T_u = 100$ °C (average junction temperature in <u>use environment</u>)</p>	<p>High Temperature Reverse Bias (HTRB)</p> <p>or</p> <p>High Temperature Gate Bias (HTGB)</p>	<p>$T_t = 150$ °C (junction temperature in test environment)</p>	<p>Arrhenius</p> $A_f = \exp\left[\frac{E_a}{k_B} \cdot \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ <p>Also applicable for High Temperature Storage <u>Life (HTSL)</u></p>	<p>$E_a = 0.7$ eV (activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV)</p> <p>$k_B = 8.61733 \times 10^{-5}$ eV/K (Boltzmann's Constant)</p>	<p>$t_t = 916$ hr (test time)</p> $t_t = \frac{t_u}{A_f}$	<p><u>1000 hours</u></p>
Thermo-mechanical	<p>$n_u = 54,750$ cycles (number of engine on/off cycles over 15 <u>years of use</u>)</p> <p>$\Delta T_u = 70$ °C (average thermal cycle temperature change in use environment)</p>	<p>Temperature Cycling (TC)</p>	<p>$\Delta T_t = 205$ °C (thermal cycle temperature change in test environment: -55 °C to 150 °C)</p>	<p>Coffin Manson</p> $A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$	<p>$m = 4$ (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)</p>	<p>$n_t = 744$ cycles (number of cycles in test)</p> $n_t = \frac{n_u}{A_f}$	<p><u>1000 cycles</u></p>
	<p>$n_u = 54,750$ cycles (number of engine on/off cycles over 15 <u>years of use</u>)</p> <p>$\Delta T_u = 55$ °C for <u>solder die attach</u> (average thermal cycle temperature change in use environment)</p>	<p>Intermittent Operational Life (IOL)</p>	<p>$\Delta T_t = 100$ °C (thermal cycle temperature change in test environment: 25 °C to 125 °C)</p>	<p>Coffin Manson</p> $A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ <p><u>Also applicable for Power Temperature Cycle (PTC)</u></p> <p><u>Remark: The use of a Coffin-Manson model may not be appropriate to reflect time dependence of material behavior.</u></p>	<p>$m = 2.5$ (Coffin Manson exponent <u>4</u> is to be used for <u>cracks in hard metal alloys</u>, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)</p>	<p>$n_t = 12,283$ cycles (number of cycles in test)</p> $n_t = \frac{n_u}{A_f}$	<p><u>5000 cycles</u></p>

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Table A7.1: Basic Calculations for AEC-Q101 Stress Test Conditions and Durations (continued)

<u>Loading</u>	<u>Mission Profile Input</u>	<u>Stress Test</u>	<u>Stress Conditions</u>	<u>Acceleration Model</u> (all temperatures in K, not in °C) (K = °C + 273)	<u>Model Parameters</u>	<u>Calculated Test Duration</u>	<u>Q101 Test Duration</u>
Humidity	<p><u>Engine Non-operating:</u> $t_u = 119,400$ hours (average engine off time over 15 years)</p> <p>$RH_u = 75\%$ (average relative humidity in off mode)</p> <p>$T_u = 30\text{ °C}$ (average junction temperature in engine off mode)</p>	H3TRB	<p>$RH_t = 85\%$ (relative humidity in test environment)</p> <p>$T_t = 85\text{ °C}$ (ambient temperature in test environment)</p>	<p>Hallberg-Peck</p> $A_f = \left(\frac{RH_t}{RH_u} \right)^p \cdot \exp \left[\frac{E_a}{k_B} \cdot \left(\frac{1}{T_u} - \frac{1}{T_t} \right) \right]$ <p>Also applicable for Temperature Humidity Bias (THB) and Unbiased Humidity Stress Test (UHST). See Notes.</p>	<p>$p = 3$ Reference Hallberg-Peck (1991)</p> <p>$E_a = 0.9$ eV Reference Hallberg-Peck (1991)</p> <p>$k_B = 8.61733 \times 10^{-5}$ eV/K (Boltzmann's Constant)</p>	<p>$T_t = 413$ h</p> $t_t = \frac{t_u}{A_f}$	1000 hours

Notes:

- Autoclave (121°C/100%RH) is a highly accelerated test using a saturated moisture condition that will tend to uncover failure mechanisms not seen in normal use conditions. For this reason, autoclave is not a test whose test conditions can be derived through models and assumptions. The current test conditions were selected decades ago and the test has been used as part of a standard qualification ever since.
- Most Pressure Pot testing is performed with an Air Pressure Pot. Air purging is done at 100°C boiling water, and with both steam and liquid escaping from the vent. The chamber walls are not independently heated at all. Control of the chamber wall temperature; air purging procedure, during ramp-up; ramp-down temperature and pressure and overall temperature and pressure are key. In addition, when the test is ended the heater is turned off and the vent is opened. It takes about 3 minutes to fully vent the pot. A significant concern is that venting before the pot chamber drops to 100°C, can cause a pressure differential from the >100°C residual hot device and cause any water trapped in device void to create a pop-corning type of delamination.
- Regarding HAST vs. UHAST: bias does have an effect on failure rate and may be used to accelerate if component allows higher bias (e.g., corrosion, mobile ions).

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Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	May 15, 1996	Initial Release
A	May 5, 1999	General Revision - Corrected errors, made clarifications, changed lot requirements. Removed CDF and "Automotive Grade" designations throughout.
B	July 25, 2000	Update signature block on page 1; Removed "Parts must be mounted to test boards." from "Additional Requirements" for Pre-conditioning in Table 1 page 8; Changed "IOL" to "PTC" in "Additional Requirements" for Power and Temperature Cycle in Table 1 page 9; Removed revision from "Reference" for Resistance to Solder Heat in Table 1 page 10 (i.e. B-106-A becomes B-106); Added note U to "Legend for Tables 1 and 2" on page 11.
C	June 29, 2005	Revised table numbers throughout document Section 1.1.2 - Definition of Stress Test Qualification clarification Section 1.2.2 – Delete one, add two Industrial standard references Section 1.2.3 – Delete two, add one AEC standard references Section 1.2.4 – Add two quality standard references Section 2.1 – Define what "AEC Q101 Qualified" means Section 2.3 – Reference to Table 1 Table 1 – Part Qualification/Requalification Lot Requirements Section 2.4.3 - Editorial Section 2.5 – Current leakage measurement accuracy limit Section 3.2 – Requirements of supplier for process changes Section 3.2.1 – Process Change definition Section 3.2.2 – Remove reference Section 4.2 – Family data disallowance clarification Section 4.3 – Charged Device Model limitations Section 4.4 – Reference to TS-16949 Table 2: Qualification Test Definitions Test 2 – PC before PTC required Test 3 – JEDEC reference Test 5 – Ambient/Junction temperature requirements Test 6 - Ambient/Junction temperature requirements Test 7 – Temperature extremes requirement Test 8 – Added note Test 9 – Ambient temperature and test requirements Test 9alt – New alternative test option Test 10 – Test requirement and added note Test 10alt – Test criteria, requirement and added note Test 11 – Criteria for CDM requirement Test 12 – HAST as alternative Test 20 – Allowance for alteration of test method Test 21 – Clarification of test method Legend – 5 new notes to table 2 Table 2A – IOL/PTC cycling requirements per package type Table 2B – Solder conditions per package type Table 3 – New changes and notes added

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<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
C (cont.)		Appendix 2 – Reference to website, clarify requirements Appendix 3 – Reference to website Appendix 4 - Reference to website
D	May 18, 2013	Complete Revision. Revised document title to reflect that the stress test qualification requirements are failure mechanism based. Revised Sections 1.2., 1.2.3, 2.2, 2.3, 2.4.4, 2.5, 2.6, 2.7, 3.1, 3.2, 3.2.1 to 3.2.4, 4.3, Appendix 1, Appendix 2, Appendix 4, Figure A4.1, and Tables 1 to 3. Added Sections 1.2.5, 1.3, 1.3.1 to 1.3.3, 2.4.5, 4.5, Appendix 6, Appendix 7, Figures 1, A7.1, A7.2, and Tables 2A, 2B, A7.1. Deleted Sections 1.1.2, 1.1.3, and 2.1.
<u>E</u>	<u>Mar. 1, 2021</u>	<u>Complete Revision. Revised Sections 1.2.2, 1.2.3, 1.2.4, 1.3.1, 1.3.3, 2.2, 2.4 to 2.7, 3.2.3, 4.2, 4.3.2, 4.3.3, 4.3.3, 4.4, Appendix 7, Table 1, Table 2 (for structure and content), Legend for Table 2, Table 2A, Table 2B, Table 3 (for structure and content), and Table A7.1. Added Sections A7.2.2, A7.3, and Figure 2. Deleted Sections A7.2, A7.3.2, and A7.3.3 to A7.4.</u>