Automotive Electronics Council
Component Technical Committee

ATTACHMENT 1

AEC - Q101-001 Rev-A

HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council
Component Technical Committee

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METHOD - 001

DISCRETE COMPONENT HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for discrete components.

1.2 Reference Documents:

EOS/ESD Association Specification STM5.1
JEDEC Specification EIA/JESD22-A114

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity:

An ESD voltage level resulting in component failure.

1.3.5 ESD Simulator:

An instrument that simulates the human body model ESD pulse as defined in this specification.

1.3.6 Human Body Model (HBM) ESD:

An ESD pulse meeting the waveform criteria specified in this test method.

1.3.7 Maximum Withstanding Voltage:

The maximum ESD voltage at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

1.3.8 PUT:

The pin and/or terminal under test.

1.3.9 Ringing current (IR):

The high frequency current oscillation usually following the pulse rise time.

1.3.10 Worst Case Pin and/or Terminal Pair (WCP):

WCP is the pin and/or terminal pair representing the worst case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent HBM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 1, Figure 2, and Figure 3.

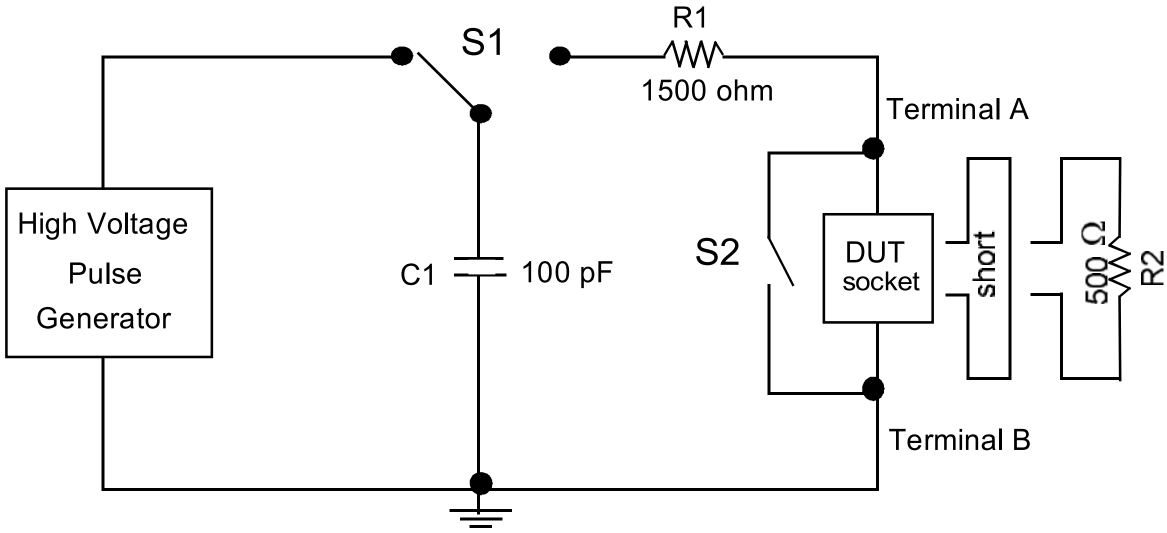


Figure 1: Typical Equivalent HBM ESD Circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
4. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 Volt, 500 ohm resistor with ±1% tolerance.
5. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
6. Reversal of terminals A and B to achieve dual polarity is not permitted
7. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment:

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe:

The current probe shall have a minimum bandwidth of 350 Mhz and maximum cable length of 1 meter (Tektronix CT-1 or equivalent).

2.2.2 Evaluation Loads:

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with + 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst case pin and/or terminal pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope:

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 Mhz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification:

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 1000 volt level using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst case pin and/or terminal pair (WCP) using only the shorting wire per section 2.4.1. The worst case pin and/or terminal pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at either the 1000 or 4000 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure:

a. With the required DUT socket installed and with no component in the socket, attach a shorting wire in the DUT socket such that the worst case pin and/or terminal pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 5 nanoseconds per division or less.

c. Initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

g. Set the horizontal time scale of the oscilloscope at 100 nanoseconds per division or greater and initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

h. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

i. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

j. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

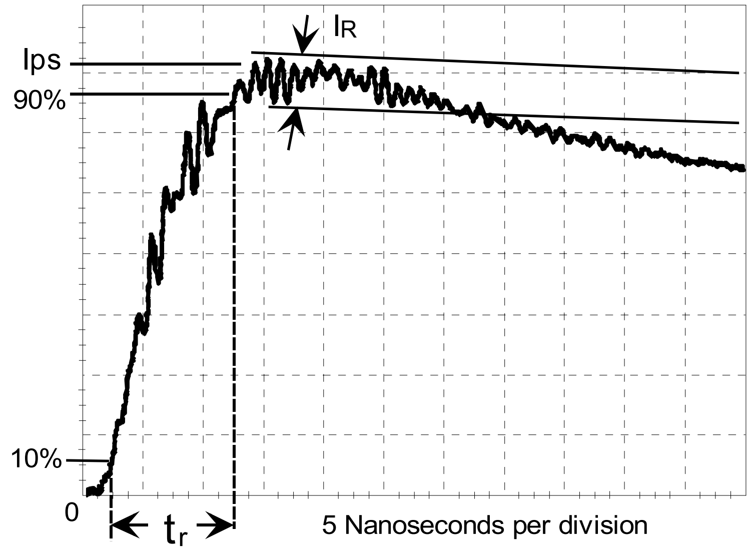
Table 1: HBM Waveform Specification

Voltage Level (V)	Ipeak for Short, I_{ps} (A)	Ipeak for 500 Ohm * I_{pr} (A)	Rise Time for Short, t_r (ns)	Rise Time for 500 Ohm * t_{rr} (ns)	Decay Time for Short, t_d (ns)	Ringing Current I_R (A)
1000	0.60 - 0.74	.375 - .55	2.0 - 10	5.0 - 25	130 - 170	15% of I_{ps} and I_{pr}
2000	1.20 - 1.46	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
4000	2.40 - 2.94	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
8000	4.80 - 5.86	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}

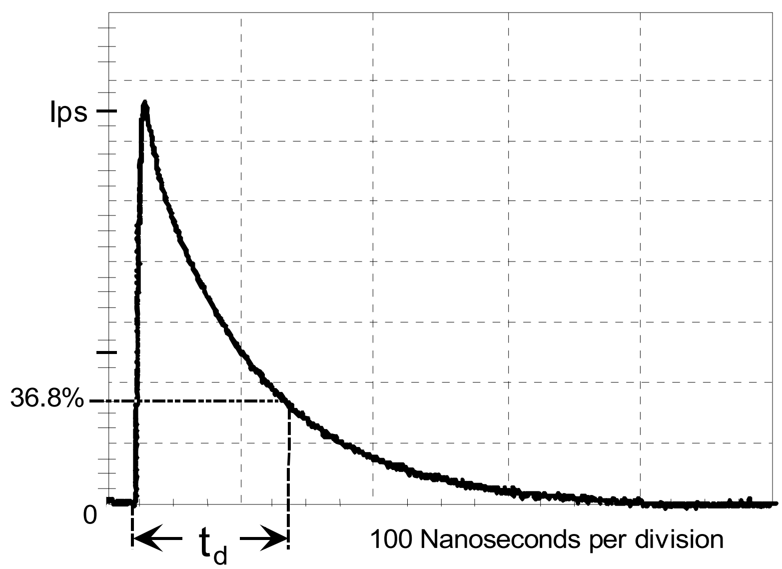
*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

2.5 Automated ESD Test Equipment Relay Verification:

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

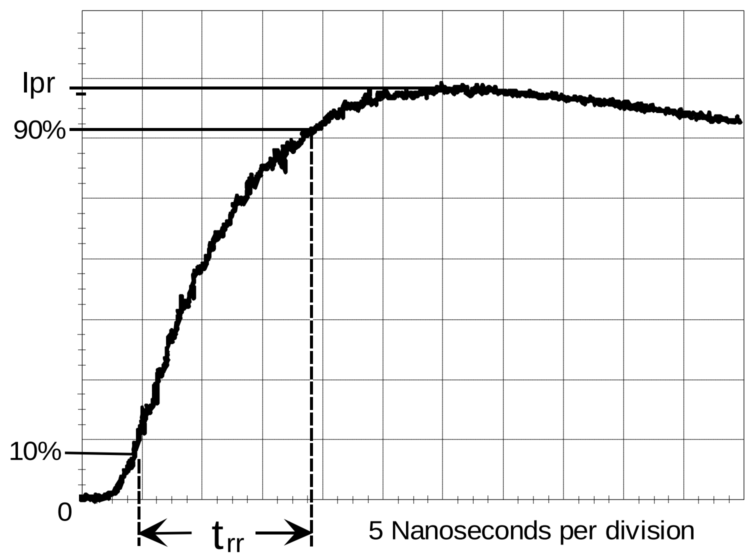


(a) Pulse rise time, (t_r)



(b) Pulse decay time, (t_d)

Figure 2: HBM Current Waveforms through a Shorting Wire



(a) Pulse rise time, (t_{rr})

Figure 3: HBM Current Waveform through a 500 Ohm Resistor *

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

3. TEST PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of ten (10) components per stress voltage level (for a total sample size of 30 components as specified in Table 1 of AEC-Q101). Each sample group shall be stressed at one (1) stress voltage level, following the test flow diagram of Figure 4, using all pin and/or terminal combinations specified in section 3.2. Each stress voltage level requires a new sample group of ten (10) components.

3.2 Pin and/or Terminal Combinations:

Each pair of pins and/or terminals and all combinations of pin and/or terminal pairs for each component shall be subjected to test pulses at each stress voltage polarity following the ESD levels stated in Figure 4. Any pin and/or terminal not under test shall be in an electrically open (floating) state.

3.3 Test Temperature:

Each component shall be subjected to ESD pulses at room temperature.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each component shall be made listing all parameter measurements as defined in Table 2. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of section 4.

3.5 Detailed Procedure:

The ESD testing procedure shall be per section 3.2, Figure 4, and as follows:

a. Follow the recommended test flow diagram of Figure 4.

b Connect a selected PUT (see section 3.2) to terminal B.

c. Connect an individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable, and may be required per user agreement.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable, and may be required per user agreement.

f. Disconnect the PUT from testing and connect the next individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

g. Repeat steps (d) through (f) until every pin and/or terminal not connected to terminal B is pulsed at the specified voltage (see section 3.2).

h. Repeat steps (b) through (g) until all pin and/or terminal combinations have been stressed.

i. Test the next component in the sample group and repeat steps (b) through (h) until all components in the sample group have been tested at the specified voltage level.

j. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the failure criteria requirements specified in section 4. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

k. Using a new sample group, select the next stress voltage level as specified in Figure 4 and repeat steps (b) through (j)

l. Repeat steps (b) through (k) until failure occurs or the maximum withstanding voltage level has been reached.

4. FAILURE CRITERIA:

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift values for the specific key parameters listed in Table 2. Other component parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 2: Key Parameters and Allowable Shift Values

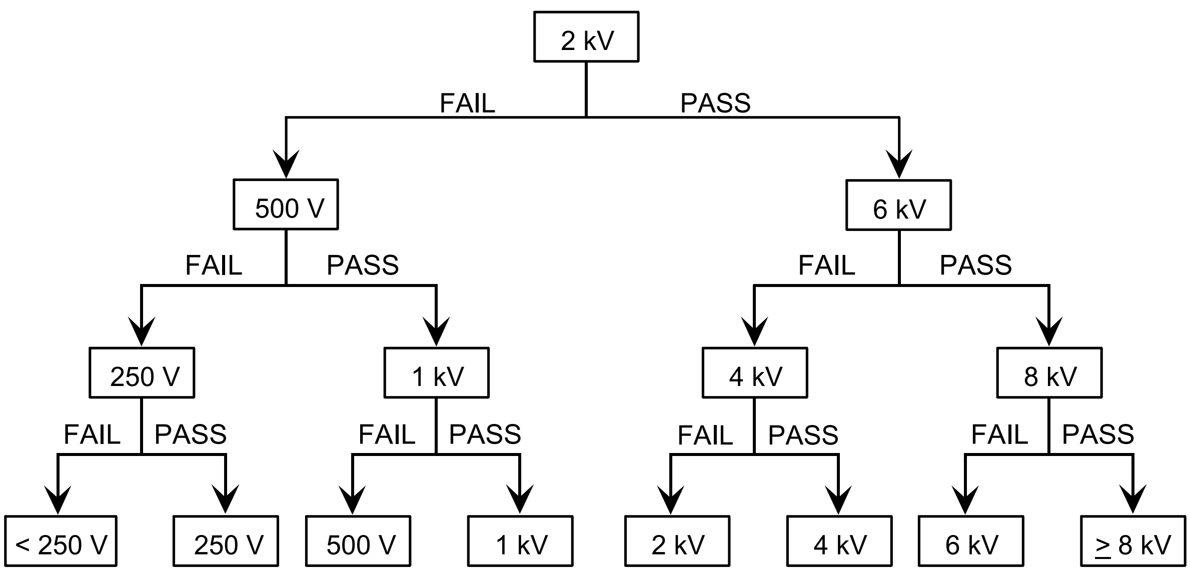
Component Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

5. ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level and below pass. All the samples must meet the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 3, classify the components according to the highest ESD voltage level survived during ESD testing. The ESD withstanding voltage shall be defined for each component by the supplier.

Table 3: Discrete Component HBM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
H0	≤ 250 V
H1A	> 250 V to ≤ 500 V
H1B	> 500 V to ≤ 1000 V
H1C	> 1000 V to ≤ 2000 V
H2	> 2000 V to ≤ 4000 V
H3A	> 4000 V to ≤ 8000 V
H3B	> 8000 V



Note 1: Classify the components according to the highest ESD voltage level survived during ESD testing.

Figure 4: Discrete Component HBM ESD Test Flow Diagram

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	May 15, 1996	Initial Release.
A	July 18, 2005	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (d and e), and 5; Tables 1 and 3; Figure 1. Revision to section 3.5 (d and e) reflects a change from three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses at each stress polarity to one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. This change is required to align with industry standards. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable, and may be required per user agreement. Revision to Table 1 reflects a ±10% tolerance applied to all Ips (Ipeak for short) parameter values.