

ATTACHMENT 11

AEC - Q100-011 Rev-C1

CHARGED DEVICE MODEL (CDM)

ELECTROSTATIC DISCHARGE TEST

Automotive Electronics Council

Component Technical Committee

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-011 Rev-C:

- **Section 1.2, Reference Documents:** Added ANSI/ESD S5.3.1 standard document reference.
- **Section 1.3.9, Corner Pins:** Added new definition for Corner Pins. Provided examples of packages with and without corner pins.
- **Section 3.1, Sample Size:** Allow use of expanded sample group size per voltage step to use partitioned pin group stressing.
- **Section 3.2, Charging and Discharging Methods:** Modified preferred discharge method to be a “non-relay” based method (previously was a “relay” based method).
- **Section 3.2.2, Field Charging Method:** Modified text to reflect recommendation of minimum field plate size of 7X DUT size, rather than requirement (replace “shall” with “should”).
- **Section 3.2.3, Relay Discharge Method:** Replaced Rev-B Section 3.2.3, Direct Discharging Method with new Section 3.2.3, Relay Discharge Method. Added caution regarding additional parasitics and effect on discharge waveform.
- **Section 3.6, Small Package Considerations:** Added new section to reflect challenges of small package CDM testing.
- **Section 3.7, Wafer or Bare Dice Considerations:** Added new section to reflect challenges of wafer or bare dice CDM testing.
- **Section 3.8, Detailed Procedure - step i:** Modified text to reflect recommendation of post-stress ATE testing within 96 hours after stress, rather than requirement.
- **Section 3.8, Detailed Procedure - step j:** Allow use of new sample group per voltage step and smaller pulse voltage increments.
- **Section 3.8.1, Corner Pin Classification Procedure:** Added new section to define procedure for 750 volt classification of corner pins (Table 4, Class C4B).
- **Table 4, Integrated Circuit CDM ESD Classification Levels:** Modified table classification levels and withstand voltage to align with ANSI/ESD S5.3.1.
 - **NOTE (dated March 12, 2013):** *The AEC - Q100-011 document was revised to correct symbol errors that occurred during the conversion to PDF format. The revision only affects Table 4, Component Classification levels C4B and C6, where the \geq symbol was inadvertently replaced with the = symbol. No other modifications have been made to the document.*
- **Section 6, Test Reporting:** Added new section defining contents of test report, including testing performed, detailed results, and any deviations.

METHOD - 011

CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic devices. This test method does not include socketed CDM.

1.2 Reference Documents

ANSI/ESD S5.3.1-2009, Charged Device Model (CDM), Component Level

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Charged Device Model (CDM) ESD

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD event that occurs when a device becomes charged (e.g., triboelectric) and discharges to a conductive object or surface.

1.3.2 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.3 Device Under Test (DUT)

An electronic device being evaluated for its sensitivity to ESD.

1.3.4 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.5 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.

1.3.6 ESD Simulator

An instrument that simulates the charged device model ESD pulse as defined in this specification.

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1.3.7 Pin Under Test (PUT)

The pin under test; this includes all device pins as well as all power supply and ground pins.

1.3.8 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

1.3.9 Corner Pins

Corner pins are pins of an integrated circuit (IC) package that singularly have a higher probability of contact with a grounded surface, based on their package pin geometry. The following leaded package types are expected to have corner pins: Dual in Line (DIP, 4 corner pins), Small Outline Integrated Circuit (SOIC, 4 corner pins), Quad Flat Pack (QFP, 8 corner pins), and Plastic Leaded Chip Carrier (PLCC, 8 corner pins). IC packages for which no pins or balls extend further in the X or Y direction than the package housing, and / or are aligned in an array of equal distribution across a single package surface, may be classified as not having corner pins. Due to the inherent design of the package, QFN (Quad Flat Pack No Lead), WCSP (Wafer Chip Scale Packages) and Ball Grid Arrays (BGAs) with missing pins in the actual corner pin locations do not have corner pins. BGA packages with specific corner pins in the pin array corner are classified as having corner pins (see Figure 1). Engineering judgment shall be made to determine if other packages have corner pins and which pins will be defined as corner pins.

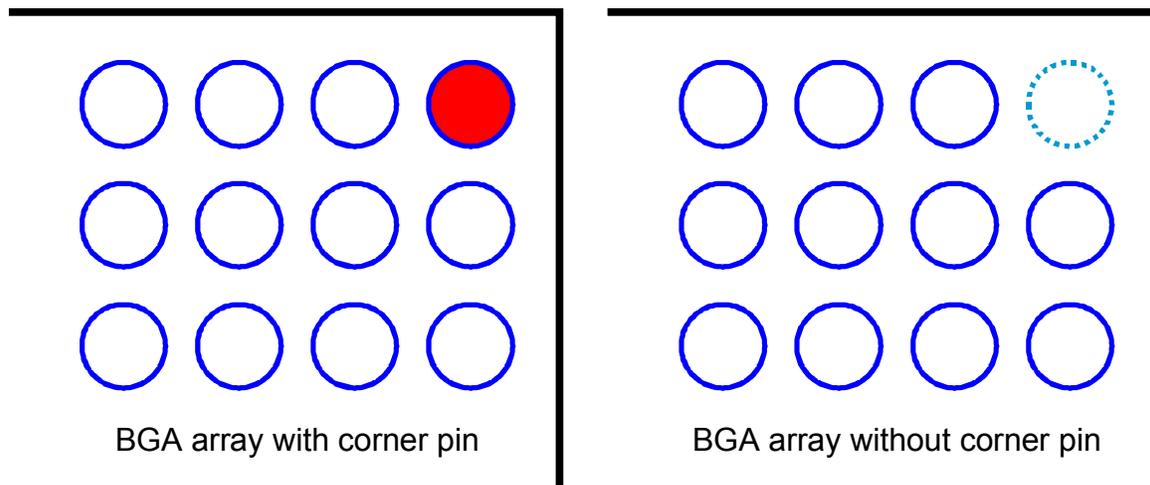


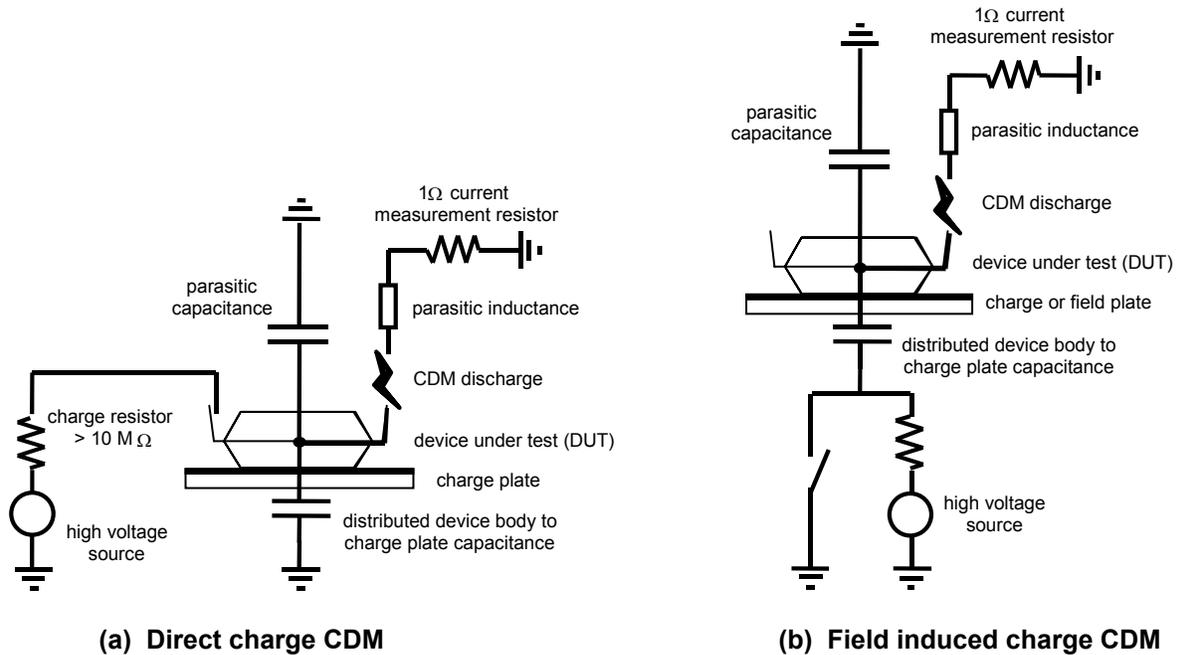
Figure 1: BGA package pin arrays with corner pin (left) and without corner pin (right)

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator; Figure 2 shows a typical equivalent CDM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 2, Table 3, and Figure 4.

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Note: Parasitics in the charge and discharge path of the test equipment can greatly affect test results

Figure 2: Charged Device Model ESD typical equivalent circuit for (a) direct charge and (b) field induced charge

2.2 Measurement Equipment

Equipment shall include an oscilloscope/digitizer, current probe, attenuators, and cable/connector assemblies to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 2, Table 3, and Figure 4.

2.2.1 Oscilloscope/Digitizer

The oscilloscope/digitizer shall have a minimum bandwidth of 1.0GHz and nominal input impedance of 50Ω (Tektronix SCD1000, HP 7104, or equivalent).

2.2.2 Current Probe

The current probe shall be an inductive current transducer or coaxial resistive probe with a minimum bandwidth of 5GHz.

2.2.3 Attenuator

The attenuator, if required, shall be high precision (+0.1dB precision at 1.0GHz) with impedance of 50Ω.

2.2.4 Cable/Connector Assembly

The cable/connector assembly, if required, shall be low loss (less than 0.4dB loss up to 1GHz) with impedance of 50Ω.

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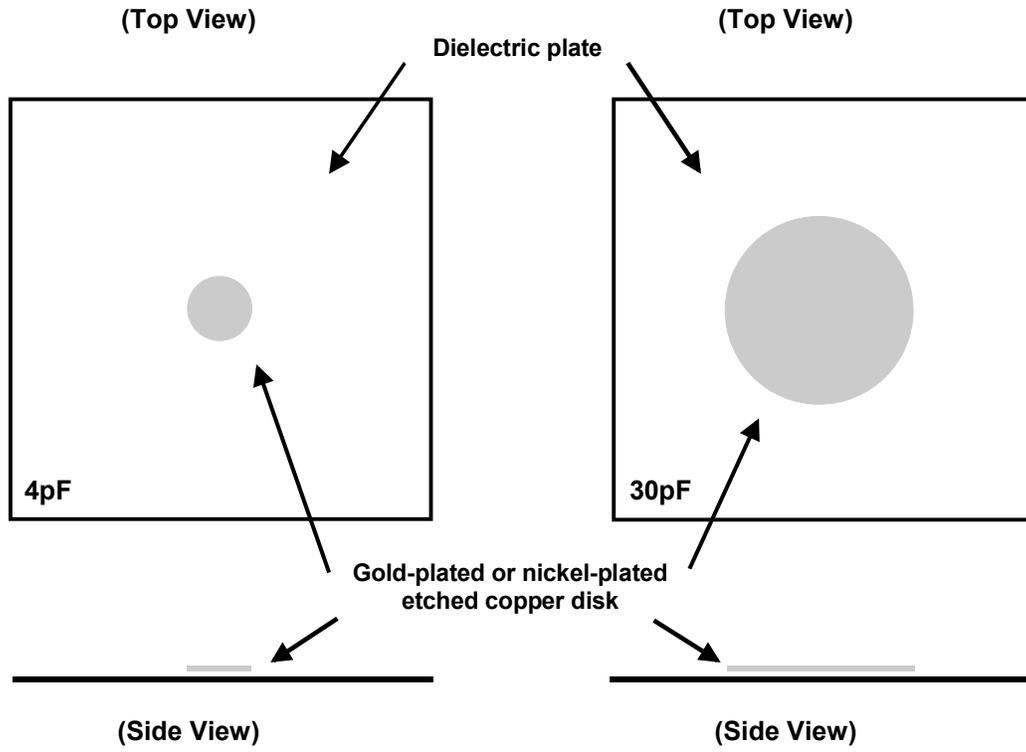
2.2.5 Verification Modules

The two verification modules shall be gold-plated or nickel-plated etched copper disks on single sided FR-4 material (thickness = 0.8mm). The disks shall be: 1) a small disk (diameter approximately = 9 mm) configuration with a capacitance value of 4pF \pm 5% measured at 1MHz, and 2) a large disk (diameter approximately = 26mm) configuration with a capacitance of 30pF \pm 5% measured at 1MHz. Each disk shall be created using an etching process and centered on FR-4 material measuring at least 30mm by 30mm. Capacitance shall be measured with the non-metallized and non-disk side of the verification module in direct contact with the metal surface of a ground plane. Verification module parameters and illustrations are shown in Table 1 and Figure 3.

Table 1: Verification module parameters

Verification Module	Parameter	Accepted Value
4pF	Capacitance	3.8pF to 4.2pF
	Disk diameter	~ 9mm
	FR-4 material size	\geq 30mm by 30mm
	FR-4 thickness	0.8mm
30pF	Capacitance	28.5pF to 31.5pF
	Disk diameter	~ 26mm
	FR-4 material size	\geq 30mm by 30mm
	FR-4 thickness	0.8mm

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(a) 4pF verification module (~ 9mm disk) (b) 30pF verification module (~ 26mm disk)

Figure 3: Verification module illustrations, (a) 4pF and (b) 30pF

2.2.6 Capacitance Meter

The capacitance meter shall have a resolution of 0.2pF when measured at 1.0MHz with 3% accuracy.

2.3 Equipment Calibration and Qualification

All peripheral equipment (including but not limited to the oscilloscope/digitizer, current probe, attenuators, cable/connector assemblies, verification modules, and capacitance meter) shall be periodically calibrated according to manufacturer's recommendations. A period of one (1) year is the maximum permissible time between full calibration tests. Qualification of the CDM simulator must be performed during initial acceptance testing or after repairs that are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 2 and Figure 4 for five (5) consecutive waveforms at all voltage levels using the 4pF verification module shown in Figure 3. Simulators not capable of producing the maximum voltage level shown in Table 2 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 3 and Figure 4 for five (5) consecutive waveforms at the 500 volt level using the 30pF verification module shown in Figure 3. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

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2.4 Verification Module Calibration

The capacitance value of verification modules can be dramatically degraded by excessive use (indentations due to repetitive pogo pin contact, cracks in metallization, warping, etc.). Therefore, to ensure proper capacitance values, it is recommended that module capacitance be verified per section 2.4.1. When modules are degraded to the point they no longer meet the specified capacitance requirements shown in Table 1, they must be replaced.

2.4.1 Verification Module Capacitance Measurement Procedure

- a. Using the 4pF verification module, place the non-metallic side of the module in direct contact with the metallic surface of a ground plane. Capacitance measurements can be affected by air gaps between the module and the ground plane (e.g., due to warping of the FR-4 material, etc.). Therefore, the air space between the module and the ground plane must be minimized. This can be accomplished by applying slight pressure using the capacitance meter probes; care must be taken to avoid damaging the disk metallization.
- b. Using the capacitance meter defined in section 2.2.6, measure the capacitance of the verification module to the ground plane. The capacitance value shall meet the requirements defined in Table 1.
- c. Repeat steps (a) and (b) using the 30pF verification module.

2.5 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified using the 4pF verification module. The waveform verification shall be performed prior to performing CDM testing. If at any time the waveforms do not meet the requirements of Table 2 and Figure 4 at the 500 volt level, the testing shall be halted until waveforms are in compliance.

2.5.1 Waveform Verification Procedure

- a. Prior to performing waveform verification, verification modules and tester components (e.g., pogo pin, charge plate, etc.) must be cleaned with isopropanol (isopropyl alcohol) using a procedure approved by the user's internal safety organization. Once clean, avoid direct skin contact. If handling is required, the use of vacuum tweezers or personnel finger cots is strongly recommended.
- b. Place the 4pF verification module in direct contact with the charge plate of the CDM simulator. If a dielectric film is used during device testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.
- c. Set the horizontal time scale of the oscilloscope at 0.5 nanoseconds per division or less.
- d. Raise the charge plate potential to positive 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.
- e. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 4.

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- f. Raise the charge plate potential to negative 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.
- g. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 4.

Table 2: CDM Waveform Specification for 4pF Verification Module

Voltage Level (V)	1 st peak current for 4pF I_{p1} (A) (±20%)	2 nd peak current for 4pF I_{p2} (A)	3 rd peak current for 4pF I_{p3} (A)	Rise Time t_r (ps)	Full width at half height for 4pF FWHH (ps)
250	2.25	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
500	4.50	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
1000	9.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
2000	18.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600

Table 3: CDM Waveform Specification for 30pF Verification Module

Voltage Level (V)	1 st peak current for 30pF * I_{p1} (A) (±20%)	2 nd peak current for 30pF * I_{p2} (A)	3 rd peak current for 30pF * I_{p3} (A)	Rise Time T_r for 30pF * (ps)	Full width at half height for 30pF * FWHH (ps)
500	14.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 1000

* The 30pF verification module is used only during Equipment Qualification as specified in section 2.3.

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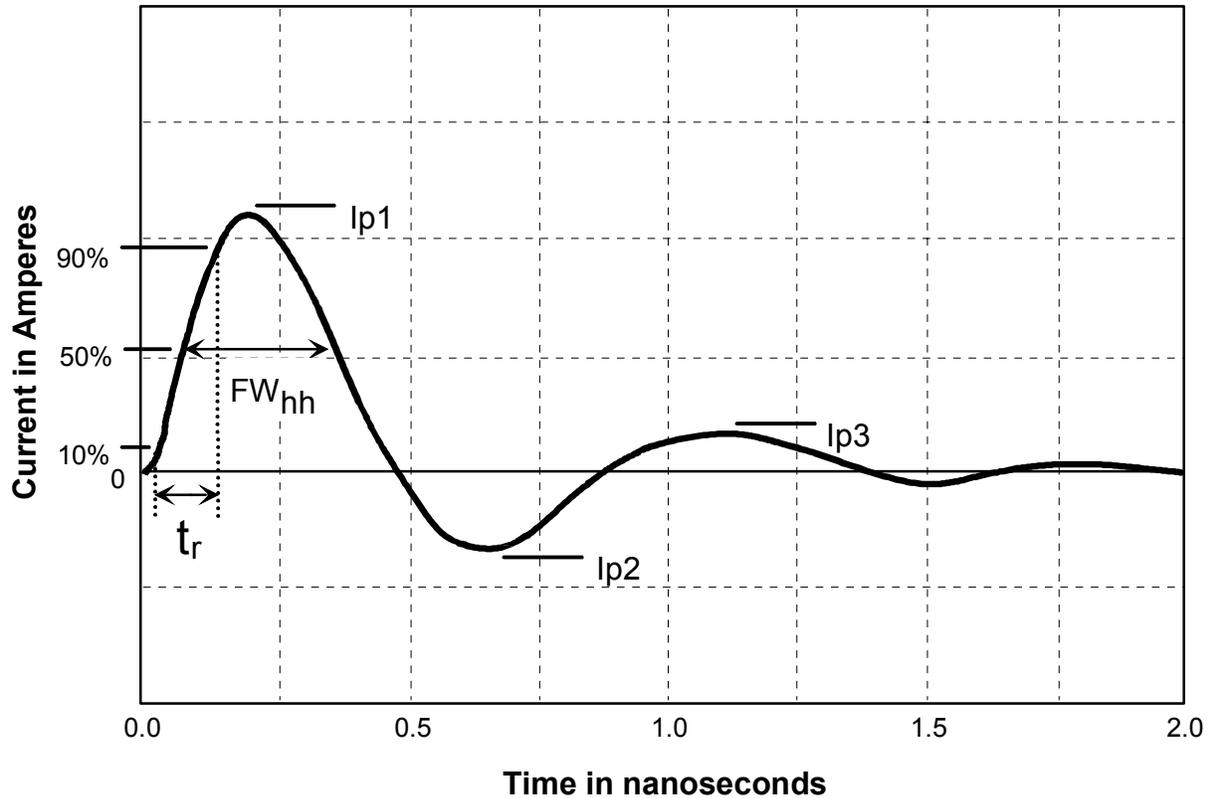


Figure 4: Typical CDM current waveform

3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall have all device pins (including power and ground pins) stressed at one (1) voltage level. It is permitted to use the same sample group for the next higher stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Voltage level skipping is not allowed. Therefore, the minimum number of devices required for ESD qualification is three (3) devices, while the maximum number of devices depends on the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device with a maximum withstanding voltage of 500 volts requires 2 voltage steps of 250 volts each and 3 devices per voltage level for a maximum total of 6 devices.

$$\text{Maximum \# of devices} = (\text{\# of voltage steps required}) \times 3 \text{ devices}$$

It is permitted to expand the sample group size per voltage step to allow partitioned pin group stressing, by either polarity or pin, as long as every pin is stressed three times positively and three times negatively for three equivalent parts in the expanded sample group, as it would be in the regular sample group.

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3.2 Charging and Discharging methods

There are two acceptable methods of charging a DUT: Direct Charging and Field-induced Charging. Either method may be used to perform CDM ESD testing and must be recorded. While several methods exist for discharging a DUT, discharge without use of a relay is the preferred method. A relay-based discharge method produces more repeatable pulses, but the resulting CDM waveform specifications are more difficult to meet. If discharge without a relay is used, the method (single discharge or dual discharge) shall be documented.

3.2.1 Direct Charging Method

The DUT is placed “dead-bug” (upside down with pins pointing up) with device body in direct contact with the charge plate and charged either through the pin(s) providing the best ohmic connection to the substrate of the DUT or through all DUT pins simultaneously (see Figure 2). To prevent damaging the DUT, ensure both the device and charging mechanism are at ground potential prior to initiating the CDM test. Contact to the charging pin(s) must be made prior to raising the charge potential. Once the DUT is charged, a pin under test (PUT) is discharged (except any pin(s) directly connected to the substrate of the DUT). It is permissible to leave the charging probe in direct contact with the charging pin during the discharge event provided the discharge waveform meets the requirements of Table 2, Table 3, and Figure 4. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. Special devices (such as multi-chip modules, hybrids, and sub-assemblies) must be charged through a common power supply/ground pin or a sufficient number of device pins to ensure the charging potential is reached. All charge pins must be recorded.

3.2.2 Field-induced Charging Method

The DUT is placed “dead-bug” (upside down with pins pointing up) with device body in direct contact with the field charging plate and charged by raising the potential of the charge plate (see Figure 2). To prevent damaging the DUT, ensure both the device and charge plate are at ground potential prior to initiating the CDM test. Once the DUT is charged, a pin under test (PUT) is discharged. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. The field charging plate should be at least seven times (7X) larger in area than the DUT and shall meet the requirements of Table 2, Table 3, and Figure 4. If a dielectric film is used during device testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

3.2.3 Relay Discharge Method

CDM testers in which the CDM discharge in Figure 1 occurs within a relay can produce very reproducible results, but the relay can add parasitics which make it difficult to meet the waveform requirements of Table 2, Table 3, and Figure 4.

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

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3.5 Cleaning Method

To avoid charge loss during CDM testing, devices should be cleaned with isopropanol (isopropyl alcohol) using a procedure approved by the local safety organization. Devices should then be handled only by vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers which have been neutralized by holding in an ionized air stream. The CDM tester should be cleaned periodically with isopropanol (isopropyl alcohol) to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe, charging probe, and the charge plate on which the device is placed.

3.6 Small Package Considerations

CDM testing of integrated circuits in small packages is very challenging. The vacuum used to hold the package in place during testing is not effective when the package is under a few square millimeters. The capacitance between the device under test and the field plate is also very small, which results in very fast CDM current pulses. These pulses have non-negligible peak currents, but have very fast rise times and very narrow pulse widths, making the pulses impossible to measure with standard 1 GHz measurement systems. Additionally, the total charge within the pulses is so small that CDM failures of integrated circuits in very small packages have seldom been seen. For these reasons, the testing of integrated circuits in very small packages is often not performed (as agreed between supplier and customer) due to the difficulty of testing and the very low chance of failure. Any device or package that could not be completely CDM stressed due to package size shall be recorded.

3.7 Wafer or Bare Die Considerations

The test methods described in this standard may also be used to evaluate components that are shipped as wafers or bare dice. Standardized CDM stressing of wafers or bare dice is not defined due to equipment limitations. Products shipped as bare dice may be placed in a package for purposes of performing CDM stressing, as determined by package test limitations and agreement between supplier and customer. The package used for this stressing shall be recorded.

3.8 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 5 and as follows:

- a. Place clean DUT “dead-bug” (upside down with pins pointing up) with device body in direct contact with the charge plate.
- b. Set the charge voltage to + 250 volts. Voltage level skipping is not allowed.
- c. Select a charging method and charge the DUT.
- d. Select a PUT and discharge the DUT. After discharging, wait a minimum of 1 second and re-charge the DUT. The use of three (3) discharges at each charge voltage polarity is required.
- e. Set the charge voltage to - 250 volts. Voltage level skipping is not allowed.
- f. Repeat steps (c) through (d) using the same PUT. The use of a new sample group for each stress polarity is also acceptable.
- g. Repeat steps (b) through (f) until every PUT (all device pins, including power and ground pins) is discharged at the specified voltage level and polarity. The use of a new sample group for each PUT is also acceptable.

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- h. Test the next device in the sample group and repeat steps (a) through (g) until all devices in the sample group have been tested at the specified voltage level and polarity.
- i. Submit the devices for complete DC parametric and functional testing (final ATE verification) per applicable device specification and determine whether the devices pass the failure criteria requirements specified in section 4. The devices should be ATE tested within 96 hours of ESD testing. Complete DC parametric and functional testing shall be performed at room temperature followed by hot temperature, unless specified otherwise in the device specification. The functionality of "E²PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.
- j. Using the next sample group, increase the pulse voltage by 250 volts and repeat steps (a) through (i). Voltage level skipping is not allowed. The use of a new sample group is also acceptable. It is permitted to use the same sample group for the next stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level. If device fails at the 250 volt level, decrease the pulse voltage to 125 volts and repeat steps (b) through (i). Use of smaller pulse voltage increments (e.g., 50 volts, 100 volts, etc.) may be required to determine lower withstand levels.
- k. Repeat steps (a) through (j) until failure occurs or the device fails to meet the 125 volt stress voltage level.

3.8.1 Corner Pin Classification Procedure (Table 4, Class C4B)

The class C4B stress procedure is only necessary if classification testing at the C4A level has passed and classification testing at the C5 level results in failures.

- a. To determine the proper CDM classification of corner pins at the C4B level (750V), a minimum of three parts shall be stressed using one of the following methods:
 - Method 1: Stress corner pins only at 750V
 - Method 2: Stress all non-corner pins at 500V, followed by stressing the same three parts for corner pins only at 750V
- b. The C4B stress procedure used shall be reported in the product CDM classification report as either C4B-Method 1 or C4B-Method 2.
- c. If all devices in the sample group meet the acceptance criteria specified in section 5, then the device passes the C4B classification level.

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4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification. Complete DC parametric and functional testing immediately following the ESD test provides worst-case data results. For some devices, parametric and functional characteristics may fall outside specified device specification limits when tested immediately after ESD testing, but slowly drift towards acceptable levels over time. If complete DC parametric and functional testing is delayed, the device may be improperly classified at a higher CDM withstanding voltage.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level and below pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 4, the supplier shall classify the device according to the maximum withstanding voltage level. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or device package may require reclassification according to this test method.

Table 4: Integrated Circuit CDM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
<u>C1</u>	< 125 <u>volts</u>
<u>C2</u>	125 to < 250 <u>volts</u>
<u>C3</u>	250 to < 500 <u>volts</u>
<u>C4A</u>	500 to < 750 <u>volts</u>
<u>C4B</u>	500 to < 750 <u>volts</u> with corner pins ^[1] >= 750 <u>volts</u>
<u>C5</u>	750 V to < 1000 <u>volts</u>
<u>C6</u>	>= 1000 <u>volts</u> ^[2]

[1] Refer to Section 1.3.9 for description of packages with corner pins.

[2] For voltages above 1,000 Volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

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6. TEST REPORTING

Upon completion of the required testing defined herein, a report of the testing performed and detailed results, as defined below, including any deviations, shall be submitted to the user upon request.

a. Sample Details

- Package configuration (e.g., lead pitch, pin count, lead form, etc.)
- Sample sizes

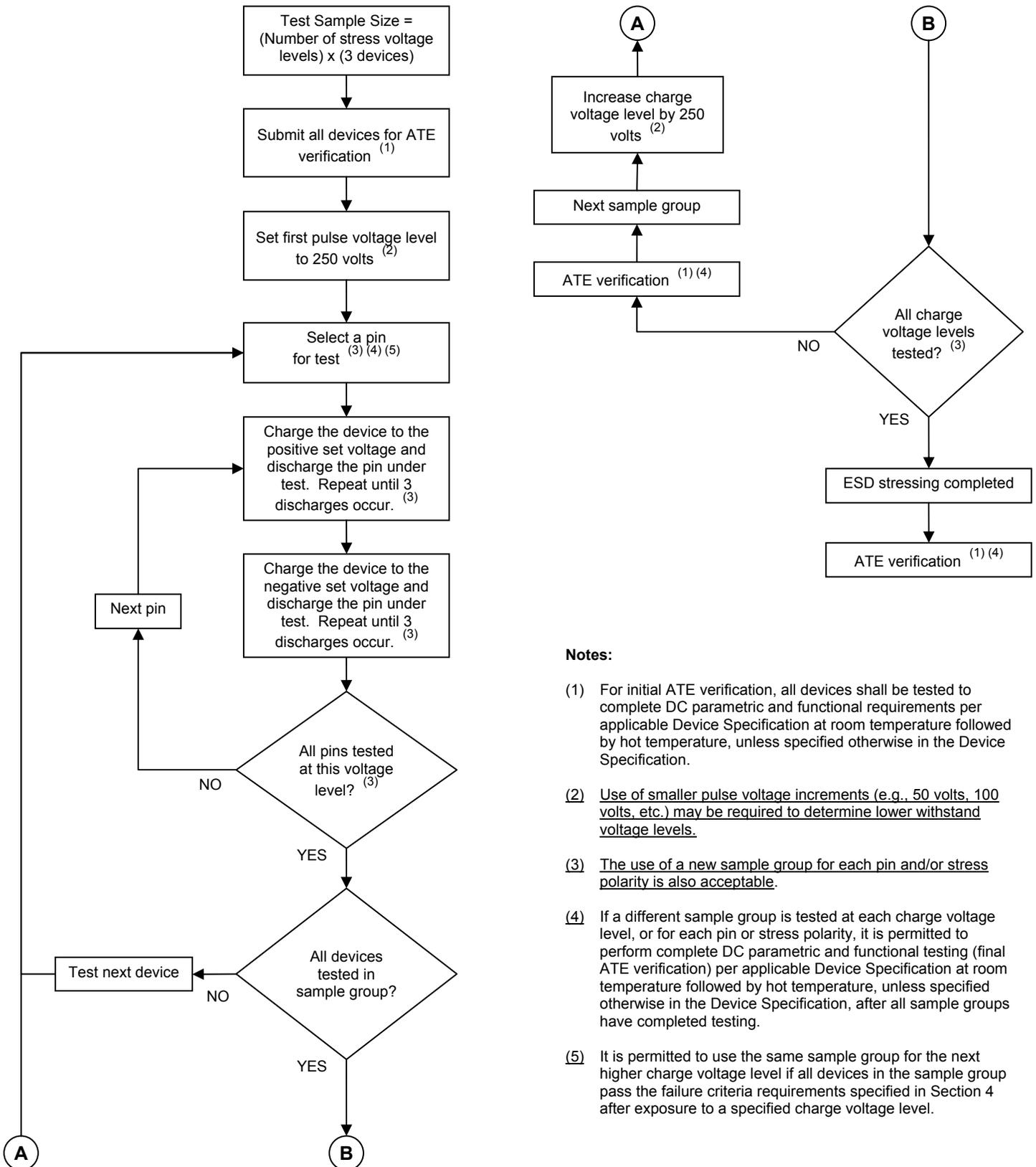
b. Test Details

- Charging/Discharging method
- Stress voltage levels
- Test/Pin partitioning (if applicable)
- Corner Pin test method (if applicable)
- Exceptions to any tests performed
 - Special considerations for small packages
 - Mounting package on a surrogate
 - Wafer/bare die

c. Test Results

- Summary of results

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Notes:

- (1) For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.
- (2) Use of smaller pulse voltage increments (e.g., 50 volts, 100 volts, etc.) may be required to determine lower withstand voltage levels.
- (3) The use of a new sample group for each pin and/or stress polarity is also acceptable.
- (4) If a different sample group is tested at each charge voltage level, or for each pin or stress polarity, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.
- (5) It is permitted to use the same sample group for the next higher charge voltage level if all devices in the sample group pass the failure criteria requirements specified in Section 4 after exposure to a specified charge voltage level.

Figure 5: Integrated Circuit CDM ESD Test Flow Diagram

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Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	Aug. 25, 2000	Initial Release.
A	Jan. 31, 2001	Changed title, revised paragraphs 1.1, 1.2, 3.2, 3.2.1, 3.2.2, revised Table 2 & 3, revised Figure 3.
B	July 18, 2003	Revision to sections 3.6 (j & k) and 5 reflect addition of classification levels for ESD testing and lower voltage step for devices failing 250V. New Table 4 added listing CDM ESD classification levels.
<u>C</u>	<u>July 20, 2012</u>	<u>Complete revision. Revised (and renumbered where appropriate) Acknowledgement and Sections 1.2, 3.1, 3.2, 3.2.3, 3.8 (steps f to j), Table 4, and Figure 5. Added Notice Statement. Sections 1.3.9, 3.6, 3.7, 3.8.1, 6, and new Figure 1. Deleted signature block.</u>
<u>C1</u>	<u>Mar. 12, 2013</u>	<u>Table 4 was revised to correct symbol errors that occurred during the conversion to PDF format. The revision only affects Table 4, Component Classification levels C4B and C6, where the \geq symbol was inadvertently replaced with the = symbol. No other modifications have been made to the document.</u>