

AEC - Q004 - Rev-
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AUTOMOTIVE ZERO DEFECTS FRAMEWORK



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ZERO DEFECTS FRAMEWORK

1. SCOPE

This document provides a framework to be used in the definition of a strategy towards Zero Defects (ZD) of any semiconductor product in the scope of the AEC-Q100, -Q101, -Q102, -Q103, and -Q104 standards and, where applicable, passive components in AEC-Q200. The list of processes, methods and tools in this framework are based on industry best practices and Suppliers may use other internally developed and proprietary methods to reduce defects.

1.1. Purpose

The purpose of this ZD framework is to enable the semiconductor Suppliers to select from a list of best practices, commonly used in the industry, that are appropriate to their products to drive to zero defects through the phases of process design, product design, production, and product/manufacturing Improvement, as depicted in Figure 1.

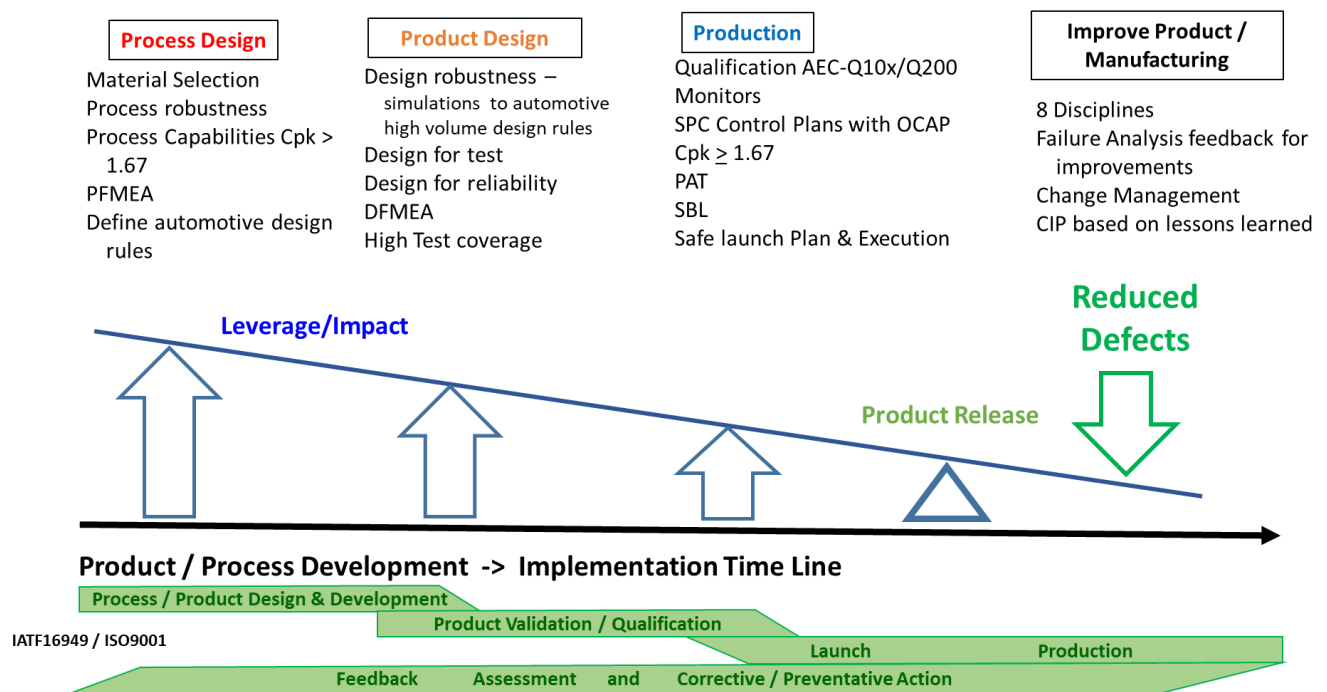


Figure 1: Zero Defects Framework – Progression towards ZD

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1.2. Reference Documents

Table 1: List of references

Document ID	Title	Section
Automotive Electronics Council (AEC) Weblink: http://www.aecouncil.com/		
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits	6.1, 6.2
AEC-Q101	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors	6.1, 6.2
AEC-Q102	Failure Mechanism Based Stress Test Qualification for Discrete Optoelectronic Semiconductors in Automotive Applications	6.1, 6.2
AEC-Q103	Failure Mechanism Based Stress Test Qualification for Sensors in Automotive Applications	6.1, 6.2
AEC-Q104	Failure Mechanism Based Stress Test Qualification for Multichip Modules (MCM) In Automotive Applications	6.1, 6.2
AEC-Q200	Stress Test Qualification for Passive Component	6.1, 6.2
AEC-Q100-007	Fault Simulation and Fault Grading	3.4, 3.8
AEC-Q100-009	Electrical Distribution Assessment	3.9
AEC-Q001	Guidelines for Part Average Testing	5.1
AEC-Q002	Guidelines for Statistical Yield Analysis	5.2
AEC-Q003	Guidelines for Characterizing the Electrical Performance of Integrated Circuit Products	3.9
AEC-Q006	Qualification Requirements for Components using Copper (Cu) Wire Interconnects	6.1, 6.2
Automotive Industry Action Group (AIAG) Weblink: https://www.aiag.org/		
AIAG APQP	Advanced Product Quality Planning & Control Plan	4.3, 6.4
AIAG SPC	Statistical Process Control	4.4
AIAG FMEA	AIAG & VDA FMEA Handbook	3.1, 4.1
AIAG PPAP	Production Part Approval Process	4.4
Electronic Industries Alliance (EIA) Weblink: -		
EIA632	Processes for Engineering a System	6.4
International Automotive Task Force (IATF) Weblink: https://www.iatfglobaloversight.org/		
IATF16949	International Automotive Task Force	4.6
International Organization for Standardization (ISO) Weblink: https://www.iso.org/home.html		
ISO26262	Road Vehicles – Functional Safety	3.2, 6.4
ISO/IEC/IEEE15288	System and Software Engineering – System Lifecycle Processes	6.4
Solid State Technology Association (JEDEC) Weblink: https://www.jedec.org/		
JEP122	Failure Mechanisms and Models for Silicon Semiconductor Devices	3.8
JEP131	Process Failure Modes & Effects Analysis	3.1, 4.1
JEP148	Reliability Qualification of Semiconductor Devices Based Upon Physics of Failure Risks and Applications Assessments	3.7, 3.8
JEP150	Stress Test Drive Qualification of and Failure Mechanisms Associated with Assembled Solid-State Surface Mount Components	6.2
JESD16	Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)	4.5, 5.4
JESD22	Test Methods	6.1, 6.2
JESD46	Customer Notification of Product/Process Changes by Semiconductor Suppliers	7.2

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Table 1: List of references (continued)

Document ID	Title	Section
Solid State Technology Association (JEDEC) Weblink: https://www.jedec.org/		
JESD50	Special Requirements for Maverick Product Elimination	4.5, 5.1, 5.2, 5.4
JESD74	Early Life Failure Rate Calculation Procedure for Electronic Components	4.5, 5.4
JESD88	JEDEC Dictionary of Terms for Solid-State Technology	
JESD94	Application Specific Qualification Using Knowledge Based Test Methodology	6.2
JESD557	Statistical Process Control Systems	4.5
JESD659	Failure Mechanism Driven Reliability Monitoring	7.3, 7.4
JESD671	Component Quality Problem Analysis and Corrective Action Requirements	8.1, 8.2
Military Standards Weblink: -		
MIL-PRF-19500	Performance Specification – Semiconductor Devices – General Specification	5.4
MIL-STD-883	Test Method Standard – Microcircuits	5.4
Society of Automotive Engineers (SAE) Weblink: https://www.sae.org/		
SAE-ARP6338	Process for Assessment and Mitigation of Early Wear out of Life-Limited Microcircuits	3.7
SAE-J1211	Robustness Validation for Electrical/Electronic Modules – section 8 – Modeling Analysis and Simulation	3.7, 6.2
SAE-J1879	Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications	6.1, 6.2
Document ID	Title	Section
SAE-J3083	Reliability Prediction for Automotive Electronics Based on Field Return Data	3.8
Others Weblink: -		
	Automotive SPICE – VDA QMC Automotive SPICE Process Assessment Model	6.4
	<i>Design Structure Matrix Methods and Applications</i> , S.D. Eppinger and T.R. Browning (Feb 2016)	6.4
	<i>Engineering a Safer World: Systems Thinking Applied to Safety</i> , N. Leveson (Jul 2012)	6.4
	INCOSE Systems Engineering Handbook (2015)	6.4
	MITRE Systems Engineering Guide (SEG)	6.4
	NIST/SEMATECH e-Handbook of Statistical Methods	4.2
	<i>Review on Redundancy in Electronics</i> , Mr. Gurudatt Kulkarni and Prof. Mrs. Lalita Wani. International Journal of Engineering and Computer Science, Nov 2013	3.2

1.3. Definitions and Acronyms

1.3.1 Product / Component / Part / Unit / Device / Design / Chip / IC

Interchangeable descriptors frequently used in an informal manner of speaking depicting a physical entity that a semiconductor Supplier conceives and delivers to the general market or to specific Users. It is a solid state based electronic entity that is designed by the Supplier to serve a special purpose, or to perform a unique function is subsequently integrated into a larger electronic system conceived by the User. In the context of this document, the use of the word “*product*” will be standardized as much as possible to aid readability. Where applicable, on an exception basis, the use of other industry accepted synonyms better suited to the specific context may also be used. Commonly found synonyms in titles of other industry standards and methods, or historical references, are retained.

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1.3.2 Safe Launch

Safe Launch is a practice defined for use when a product is introduced into production whether initial ramp by Manufacturer/Supplier or into a new project by User. The Safe Launch plan implements selected temporary controls to establish a baseline to achieve acceptable product quality. These temporary controls are typically more stringent during Safe Launch execution. Data from the Safe Launch execution is collected, monitored, and analyzed, and the Safe Launch plan may be adjusted accordingly.

1.3.3 Data Mining

Automating the process of searching for patterns in a data set (e.g., cluster analysis and data classification).

1.3.4 Degradation or Fatigue Defect

Typically a common cause or intrinsic failure that follows a trend.

1.3.5 Extrinsic defect

Physical structural irregularity (e.g., nodule or particle or void).

1.3.6 Spike

Exclusively used in combination with failure mode descriptions (e.g., electrical signal timing behavior and not for structural irregularities).

1.3.7 NTF – No Trouble Found

Both the Supplier and User could not verify a reported failure; a returned component is deemed good or functional according to specifications.

1.3.8 TNI – Trouble Not Identified

Failure mode still present but the failure mechanism and/or cause could not be isolated; failure mode changed or recovered during analysis so failure mechanism and/or cause of initial failure could no longer be identified.

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Table 2: List of Acronyms

Acronym	Description	Acronym	Description
8D	Eight Disciplines of Problem Solving	JEP	JEDEC Publication
A3/SPS	Structured Problem-Solving Tool	JESD	JEDEC Standard Document
AC	Alternating Current	Leff	Effective Length
AEC	Automotive Electronics Council	MIL-PRF	Military Performance Specification
AIAG	Automotive Industry Action Group	MIL-STD	Military Standard
ANOVA	ANalysis Of Variance	MITRE	Massachusetts Institute of Technology Research & Engineering
AP	Action Priority	MSA	Measurement Systems Analysis
APQP	Advanced Product Quality Planning	NA	Not Applicable
ATE	Automated Test Equipment	NIST	National Institute of Standards and Technology
BIST	Built-In Self-Test	NTF	No Trouble Found
BPT	Bond Pull Test	NVM	Non-Volatile Memory
BST	Bond Shear Test	OCAP	Out of Control Action Plan
BTI	Biased Temperature Instability	PAT	Part Average testing
CAE	Computer Aided Engineering	PCN	Product Change Notification
Cp	Process Capability	PFMEA	Process Failure Mode and Effect Analysis
Cpk	Process Capability Index	PoF	Physics of Fail
DC	Direct Current	Pp	Process Performance
D _{cap}	Drain Capacitance	PPAP	Production Part Approval Process
DfA	Design For Analysis	Ppk	Process Performance Index
DfM	Design For Manufacturability	PPM	Part Per Million
DFMEA	Design Failure Mode and Effect Analysis	QBD	Charge to Breakdown
DfR	Design For Reliability	QMC	Quality Management Center
DfT	Design For Testing	ROM	Read Only Memory
DfX	Design For eXcellence	Rs	Series Resistance
DOE	Design Of Experiment	SAE	Society of Automotive Engineers
DPM	Defects Per Million	SEG	Systems Engineering Guide
EIA	Electronic Industries Alliance	SEMATECH	Consortium for Semiconductor Manufacturing Technology
EM	ElectroMigration	SIMS	Secondary Ion Mass Spectroscopy
EOL	End Of Life	SPC	Statistical Process Control
FA	Failure Analysis	SPICE	Software Process Improvement and Capability Evaluation
FMEA	Failure Mode and Effect Analysis	SRAM	Static Random-Access Memory
GD&T	Geometric Dimensioning and Tolerancing	StDev	Standard Deviation
HALT	Highly Accelerated Life Testing	TDDB	Time Dependent Dielectric Breakdown
HASS	Highly Accelerated Stress Screen	TNI	Trouble Not Identified
HCI	Hot Carrier Injection	UIS	Unclamped Inductive Stress
HTOL	High Temperature Operating Life	VDA	Verband der Automobilindustrie - German Association of the Automotive Industry
HVST	High Voltage Stress Test	VLVT	Very Low Voltage Test
IATF	International Automotive Task Force	V _{max}	Maximum Voltage
IC	Integrated Circuit	V _{min}	Minimum Voltage
IDDQ	Quiescent Supply Current	V _{stress}	Stress Voltage
IEC	International Electrotechnical Commission	V _t	Threshold Voltage
IEEE	Institute of Electrical and Electronics Engineers	V _{tn}	Threshold Voltage NMOST
INCOSE	International Council on Systems Engineering	V _{tp}	Threshold Voltage PMOST
IP	Intellectual Property	V _{typ}	Typical Voltage
ISO	International Organization for Standardization	WLR	Wafer Level Reliability
JEDEC	Solid State Technology Association (Formerly Joint Electron Device Engineering Council)	ZD	Zero Defects

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1.4. Zero defects and Quality Management

An alternative view on a Zero Defects strategy can be depicted with the diagram as shown in Figure 2 below which describes, from a Quality Management point of view, the elements of such a program.

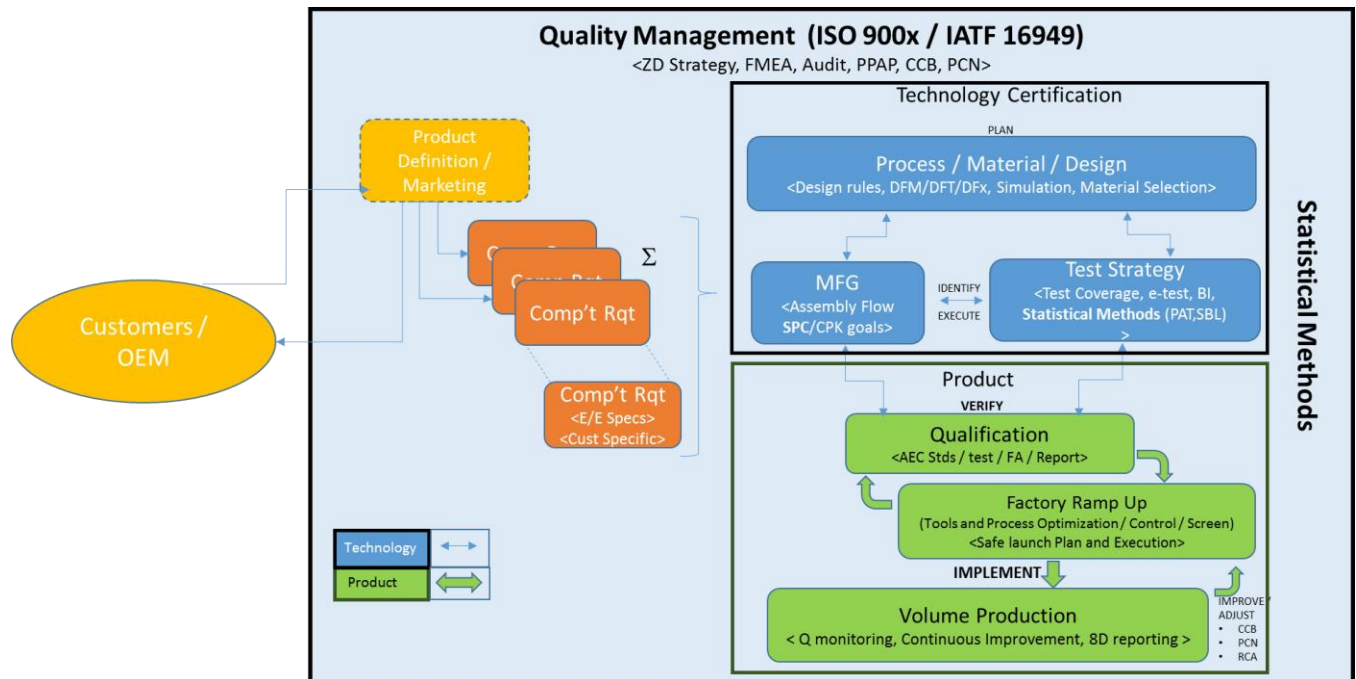


Figure 2: Zero Defects Framework – Functional / Process Flow

2. APPLICATION OF THE ZERO DEFECTS FRAMEWORK

2.1. General

This framework provides a set of established tools that semiconductor Suppliers can utilize for detecting, reducing and eliminating defects as part of their product and service offering. Semiconductor Users may specify certain tools as their expectations in agreement with Suppliers.

The selection of framework elements for combinations of a Supplier part and a User application depends on various considerations. They may include effectiveness, ease of use, availability, training, results and costs.

Table 3 lists several ZD framework elements that can be used for the following specific cases:

- Case 1: new product design in technology under development
- Case 2: new product design on automotive qualified technology
- Case 3: new product design on non-automotive qualified technology
- Case 4: released non-automotive product designated by supplier for automotive application

The template in Table 5 (refer to Section 9) can be used to communicate and document the strategy towards Zero Defects (ZD) for a given semiconductor product.

The ZD framework is built upon 6 pillars: Design, Manufacturing, Test, Application and Applicability, Continuous Improvement Methods, and Problem Solving, as reflected by the chapter structure of this

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document. Each pillar consists of methods and tools proposed to help in the following realms: description, relation to product life cycle, application and relevance, limitations and exceptions, metric and meaning of values, and references; and in some case examples. Organizations may consider applying elements in this framework, as they fit or use others that are not listed, based on the needs in that situation. In addition, all methods and tools in this document are a proposed set to help users navigate their projects, but they are not all inclusive for every situation.

AEC-Q004-001 (to be published) provides further details on how the elements of the ZD framework can be applied.

2.2. Safe Launch

One of the best practices is implementation of Safe Launch plan during the ramp to production phase. The Safe Launch plan can be defined by either the Supplier or the User based on their determination of risk for product introduction. Safe Launch plan uses several tools already included in this ZD Framework document. For example, Suppliers could use Table 3 of this document when asked to support a User Safe Launch initiative (which also can be communicated by using Table 5).

2.3. Cost Benefit Analysis

For some methods and tools, the supplier may have (including cases when products move from other applications/market areas into automotive) already factored in a cost/benefit analysis upon entering the automotive market. For example, the application of FMEAs, Control Plans, MSA studies, PAT, etc. is an inherent part of doing business in automotive. Therefore, these sections do not include a cost/benefit description. Though not all inclusive, cost/benefit considerations are described for methods and tools where measurable investment may be required for effective implementation.

Suppliers may need to do a cost/benefit analysis for planning and executing a Safe Launch initiative.

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Table 3: Zero Defects Framework and Recommendations

Explanation: R = Recommended, U = Useful (and to be considered), N = Not applicable (or not useful)

Clarification: "Design" includes electrical circuitry and package construction / materials

Chapter	Subject	Section	Tool	Case 1 & Case 2	Case 3	Case 4	Remarks
							1. New product design in technology under development 2. New product design on automotive qualified technology 3. New product design on non-automotive qualified technology 4. Released non-automotive product designated by supplier for automotive application
3	Product Design	3.1	Design FMEA	R	R	U	Case 4: design risk review/assessment recommended to find potential weaknesses in relation to the automotive application that may need other actions than re-design
		3.2	Redundancy	U	U	N	Case 4: redundancy at system level may have to be considered
		3.3	Built-in Self-Test (1)	R	R	N	Case 4: if it was not considered before, there is no added value
		3.4	Design for Test (1)	R	R	N	Case 4: if it was not considered before, there is no added value; unless it can be done via software solutions
		3.5	Design for Analysis (1)	R	R	N	Case 4: if it was not considered before, there is no added value
		3.6	Design for Manufacture	R	R	N	Case 4: if it was not considered before, there is no added value
		3.7	Design for Reliability	R	R	N	Case 4: if it was not considered before, there is no added value: reliability assessment recommended to find potential weaknesses in relation to the automotive application that may need other actions than re-design; other tools become more important
		3.8	Simulation and Modeling	R	R	U	Case 4: based on re-specification (aging) simulation can reveal potential weakness mentioned under 3.7; other tools can be used to overcome this
		3.9	Characterization	R	R	R	
4	Manufacturing	4.1	Process FMEA	R	R	R	
		4.2	Statistical Analysis of Variance	U	U	U	
		4.3	Control Plan	R	R	R	
		4.4	Statistical Process Control	R	R	R	
		4.5	Lot Acceptance Gates	R	R	R	
		4.6	Audits (Management System, Manufacturing Process, and Product)	R	R	R	
5	Test	5.1	Part Average Testing	R	R	R	
		5.2	Statistical Bin Yield Analysis	R	R	R	
		5.3	Data Collection, Storage and Retrieval	R	R	R	Retention period to be agreed between User and Supplier
		5.4	Screens	R	R	R	

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Chapter	Subject	Section	Tool	Case 1 & Case 2	Case 3	Case 4	Remarks
							1. New product design in technology under development 2. New product design on automotive qualified technology 3. New product design on non-automotive qualified technology 4. Released non-automotive product as designated by supplier, for automotive application
6	Application and Capability	6.1	Industry Standards	R	R	R	Case 1: only if an existing standard is covering the new technology; if not agreement between Supplier and User is leading (a standard under development may be guideline) Case 3, 4: in case the automotive standard cannot be met an agreement between Supplier and User is needed how to deal with the gap
		6.2	Environmental Stress Testing	R	R	R	Case 1: only if an existing tests and requirements are covering the new technology; if not agreement between Supplier and User is leading (a standard under development may be guideline) Case 3, 4: in case requirements cannot be met an agreement between Supplier and User is needed how to deal with the gap In all cases, it is best practice to use an agreed or even standardized mission profile in this alignment)
		6.3	Stress-Strength Analysis	R	R	U	Case 4: stress-strength assessment considered useful to find potential weaknesses in relation to the automotive application that may need other actions than re-design; other tools become more important
		6.4	Systems Engineering	U	U	N	Case 1,2, 3: only for non-commodities. If applicable: under the condition that it is clear what can be "engineered" still to achieve zero defect Case 4: assess the potential risks on defects from a system perspective and what can be done to mitigate (not applicable to commodities)
		6.5	Product Derating	U	U	U	Based on agreement between Supplier and User for the specific application conditions and parameters
7	Improvement	7.1	Wafer Level Process Monitoring	R	U	U	
		7.2	Process and Product Improvements	R	R	R	PCN process to follow for major changes
		7.3	Product Reliability Monitoring	R	R	R	
		7.4	Defect Monitoring	R	R	R	
8	Problem Solving	8.1	Problem Solving Techniques	R	R	R	
		8.2	Failure Analysis Process	R	R	R	

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3. PRODUCT DESIGN

3.1. Design Failure Mode and Effect Analysis (DFMEA)

3.1.1. Description

DFMEA is a process performed by subject experts that identifies potential failure modes and their effects on the product in the system and its application, estimates their severity, occurrence and detection, and identifies possible causes and controls. The DFMEA document identifies the risks associated with something potentially going wrong (i.e., out of specification condition or loss of functionality) in the design of the product. The FMEA identifies what controls are placed in the design process to catch abnormal conditions with known or potential impact on specification or functionality of the product at various stages on the product development. The DFMEA provides a relative ranking (action priority) based on the risk and effect associated with the severity, occurrence and detection of a particular failure mode that facilitates prioritization of resources in implementation of controls in the design process. In summary, the DFMEA is essentially a collection of expert knowledge and lessons learned from other related processes and products.

3.1.2. Relation to Product Life Cycle

DFMEAs are performed on all new components and systems during design of the product or development and implementation of process flow. DFMEA documents are also updated for all design changes. This is a living document that can change upon new lessons learned and should be periodically reviewed for accuracy or relevance.

3.1.3. Application and Relevance

DFMEAs identify all known potential modes of failure in design, their risks and effects, and how to control them.

3.1.4. Limitations and Exceptions

DFMEA is not applicable to a product that is either fully mature and not changed, or replaced, or discontinued (reaching End-of-Life).

3.1.5. Metrics and Meaning of Values

Action Priority (AP) used to prioritize which failure mode or mechanism is most influential to product failure.

3.1.6. References

- AIAG & VDA: FMEA Handbook
- JEP131: Process Failure Modes & Effects Analysis

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3.2. Redundancy

3.2.1. Description

A parallel system of duplicate cells or components that produces the same functionality and deliver equal performance to replace faulty ones seamlessly during the final test or actual use of a product. Redundancy can greatly increase the system's mean time to failure.

There are four predominant types of redundancy in electronics:

1. Hardware redundancy, such as dual modular redundancy and triple modular redundancy.
2. Information or automated redundancy, such as error detection and correction methods.
3. Time redundancy, performing the same operation multiple times such as multiple executions of a program or multiple copies of data transmitted.
4. Software redundancy such as N-version programming.

The type of redundancy is usually done during the product design phase and, therefore, the trade-off between the added cost of implementation and the benefit to the User has already been considered.

3.2.2. Relation to Product Life Cycle

Used during design and test of semiconductor products.

3.2.3. Application and Relevance

Greatly reduces failure rates via robust design (transparent cell replacement) and may reduce both 0 km and field failure rates. Use for critical memory and application functions or when die size percentage increase is small or low cost vs. benefit.

3.2.4. Limitations and Exceptions

Certain design or performance restrictions may inhibit the use of redundancy.

3.2.5. Metrics and Meaning of Values

System (or aggregate part) yield and number of Customer returns with measurement of instances where redundancy is observed, activated and recorded.

3.2.6. References

- *Review on Redundancy in Electronics*, Mr. Gurudatt Kulkarni and Prof. Mrs. Lalita Wani. International Journal of Engineering and Computer Science, Nov 2013
- ISO26262, Road vehicles – Functional safety

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3.3. Built-in Self-Test

3.3.1. Description

Built-in Self-Test, or BIST, is the practice of designing the circuitry such that inputting a logic solution will allow the product to test itself. It is a technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing. This involves testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE). BIST is a Design-for-Testability (DfT) technique because it makes the electrical testing of a product easier, faster, more efficient, and less costly. Examples of BIST functions can include checkerboard and inverse scan algorithms to detect bit-to-bit shorts and back-to-back reads, address decoder fault algorithms to check for speed fault, SRAM and NVM bitmapping, etc.

Issues that need to be considered when implementing BIST are: 1) faults to be covered by the BIST and how these will be tested for; 2) how much chip area will be occupied by the BIST circuits; 3) external supply and excitation requirements of the BIST; 4) test time and effectiveness of the BIST; 5) flexibility and changeability of the BIST (i.e., can the BIST be reprogrammed through an on-chip ROM?); 6) how the BIST will impact the production electrical test processes that are already in place.

Advantages of implementing BIST include:

1. Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated.
2. Better fault coverage, since special test structures can be incorporated onto the product.
3. Shorter test times if the BIST can be designed to test more structures in parallel.
4. Easier Customer support.
5. In exceptional cases, e.g., as part of a safety concept: capability to perform tests outside the production electrical testing environment; which may allow the consumers themselves to test the product prior to mounting or even after these are in the application boards.

Disadvantages of implementing BIST include:

1. Additional silicon area for the BIST circuits.
2. Reduced access times.
3. Additional pin (and possibly bigger package size) requirements, since the BIST circuitry need a way to interface with the outside world to be effective.
4. Possible issues with the correctness of BIST results, since the on-chip testing hardware itself can fail.

3.3.2. Relation to Product Life Cycle

Built-in Self-Test is designed into the product and used during electrical test.

3.3.3. Application and Relevance

Intended for use with high complexity products. Provides the product with the capability of diagnosing itself for processing errors both in development stage and in mass production. It may also address design errors that are detectable by functions or parameters internal to the product but not accessible from the outside.

3.3.4. Limitations and Exceptions

Not intended for use with low complexity products. May be possible to switch off and not use as the part and process matures. May increase die size and software code.

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3.3.5. Metrics and Meaning of Values

Defect detectability and test coverage.

3.3.6. References

None.

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3.4. Design for Test

3.4.1. Description

The practice of designing the circuitry such that as many nodes as possible can be tested in a reasonable amount of time. Test plan reviews should be conducted to ensure maximum test coverage efficiency. Additional circuitry increases test efficiency by allowing for ability to accelerate a test stress to the element or circuit. In addition, design for test can improve fault coverage by allowing direct access to and control of circuits or elements embedded within the product that cannot be accessed directly through the I/Os. Direct access can also provide ability to better observe the result or impact of the test.

Examples of DfT can include: fault coverage of scan stuck-at and transition faults (AC scan: fault delay tests, transition delay tests, coupling faults), critical timing paths from static timing analysis, functional/speed patterns to test I/O interface, analog I/O patterns for voltage ramps and DC tests, drive strength and slew rates, and Customer application codes (User and Supplier).

Costs may include layout complexity, potential design time increase, and test software development. Benefits may include more efficient defect screening.

3.4.2. Relation to Product Life Cycle

Design for Test can be applied by Supplier and User.

3.4.3. Application and Relevance

Intended for use with high complexity products. Provides the capability for testing as many nodes as possible and, thus, providing maximum fault coverage during test.

3.4.4. Limitations and Exceptions

Not intended for use with low complexity products.

3.4.5. Metrics and Meaning of Values

Test coverage, reduced incidence of NTF/TNI, and improved cycle time.

3.4.6. References

AEC-Q100-007: Fault Simulation and Fault Grading

3.4.7. Examples

Examples include selecting multiple memory array columns during a stress or directly accessing a memory cell to measure the V_t (threshold voltage) of the cell.

Example of a design and test program:

1. Use of Geometric Dimensioning and Tolerancing (GD&T) to provide unambiguous representation of design intent (refer also to Section 3.6.7).
2. Specification of product parameters and tolerances that are within the natural capabilities of the manufacturing process (process capability index C_p and C_{pk}) (refer also to Section 3.6.7).
3. Provision of test points, access to test points and connections, and sufficient real estate to support test points, connections, and built-in test capabilities.
4. Standard connections and interfaces to facilitate use of standard test equipment and connectors and to reduce effort to setup and connect the product during testing.
5. Automated test equipment compatibility.

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6. Built-in test and diagnosis capability to provide self-test and self-diagnosis in the factory and in the field.
7. Physical and electrical partitioning to facilitate test and isolation of faults.

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3.5. Design for Analysis

3.5.1. Description

The practice of designing the circuitry such that failure analysis can be performed as efficiently as possible for elimination of no defect found. These design considerations include modes that allow direct control and observation of embedded circuitry or elements to better electrically isolate the failing circuitry. In addition, for multiple metal layer technologies, probe points can provide access to embedded circuitry or underlying layers for control during physical failure analysis.

Costs may include layout complexity and potential design time increase. Benefits may include easier and more efficient failure analysis.

3.5.2. Relation to Product Life Cycle

Intended for use with all designs having a large number of metal layers or unique interconnection schemes (e.g., chip-on-chip).

3.5.3. Application and Relevance

Intended for use with high complexity products. Provides the capability of a more accurate and accessible analysis of failures which otherwise could be inaccessible either electrically or physically.

3.5.4. Limitations and Exceptions

Not intended for use with low complexity products (few metal levels). If the product offers security features, this may limit the ability to design those features for analysis.

3.5.5. Metrics and Meaning of Values

Reduced cycle time for Failure Analysis (FA) and reduced incidence of TNI.

3.5.6. References

None.

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3.6. Design for Manufacturability

3.6.1. Description

The practice of designing the circuitry so that manufacturing of the part is more repeatable and reproducible via larger design margins. These designs are intended to reduce the effects of extrinsic defects on the device, such as particles and process margins (e.g., lithography definition).

Costs may include increased die area to accommodate design margin techniques (e.g., redundant vias, etc.). Benefits may include reduced manufacturing defects and increased yield.

3.6.2. Relation to Product Life Cycle

Intended for use in new processes or sub-processes, new technology, new material sets or subsets and new fab or assembly sites. Implemented in the design of the product.

3.6.3. Application and Relevance

Design for manufacturability reduces the impact of extrinsic defects on product yield and quality.

3.6.4. Limitations and Exceptions

None.

3.6.5. Metrics and Meaning of Values

Manufacturing yield, process control improvement.

3.6.6. References

None.

3.6.7. Examples

Examples include:

1. Doubling (redundant) vias in areas that are process sensitive (e.g., sparse areas of vias), widening spacing between interconnect lines.
2. Reducing the number of critical timing paths using synthesis tools.
3. Usage of Geometric Dimensioning and Tolerancing (GD&T) to provide unambiguous representation of design intent (refer also to Section 3.4.6).
4. Specification of product parameters and tolerances that are within the natural capabilities of the manufacturing process (process capability index C_p and C_{pk}) (refer also to Section 3.4.6).

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3.7. Design for Reliability

3.7.1. Description

Design for Reliability (DfR) summarizes the efforts within the development process to design products that do not wear out during the entire life of the product where used as specified. This requires a systematic design approach based on awareness and consideration of the real use and accurate application of Physics-of-Failure (PoF). DfR uses a wide range of tools supporting design rules and product and process design, including but not limited to: material selection, computer-aided engineering (CAE) analysis and simulation tools, redundancy in design (e.g., redundant via in metallization) and physical characterization.

Design for reliability can provide the capability to measure and predict product reliability lifetime. Reliability issues can be prevented by designing in margin to the circuit, layout, or construction without sacrificing performance. Silicon level reliability can be monitored by test structures designed into the device or sawing lanes.

Design of Experiments techniques can provide a structured, proactive approach to improving reliability and robustness as compared to unstructured, reactive design/build/test approaches. This is done by understanding the effects of both product and process parameters on the reliability of the product and address the effect of interactions between parameters. From that, the development and use of computer-aided engineering (CAE) analysis and simulation tools at an early stage in the design process can improve product reliability more inexpensively and in a shorter time than building and testing physical prototypes. Examples of processes that DfR can utilize include finite element analysis, fluid flow analysis, thermal analysis and PoF-based.

Costs may include increase die size during development phase. Benefits may include lower risk of fails during later development and in qualification, and of need for late design revisions. Risk for field failures could also be reduced.

3.7.2. Relation to Product Life Cycle

DfR approach is most effective if applied from early concept phase on throughout the whole development process. It is intended for use in any kind of design / development / change of parts, technologies / processes or in the consideration process of products for new applications.

3.7.3. Application and Relevance

The described approach is applicable in development in general for IPs, libraries, components, and technologies for wafer and package.

3.7.4. Limitations and Exceptions

No limitations, but more applicable for high complexity products.

3.7.5. Metrics and Meaning of Values

Lifetime, failure probability, failure rate.

3.7.6. References

- JEP148: Reliability Qualification of Semiconductor Devices Based Upon Physics of Failure Risks and Applications Assessments
- SAE J1211 Robustness Validation for Electrical/Electronic Modules – Section 8 – Modeling Analysis and Simulation
- SAE ARP6338 Process for Assessment and Mitigation of Early Wear-out of Life-Limited Microcircuits

3.7.7. Examples

1. Design based on the specified range of the operating environment (e.g., product is used in a passenger compartment environment vs. engine management).
2. Design to minimize or balance stresses and thermal loads (Optimization of multiple wire bonds of power stage to homogenize the temperature distribution).
3. Add margin in design (e.g., scale-up; increase metal trace width).
4. Provide subsystem redundancy (e.g., double via).
5. Error correction (e.g., NVM, Soft error detection and correction, data retention margins).
6. Use proven elements, materials, IPs & libraries with well-characterized reliability (e.g., reuse of proven I/O cells).
7. Consolidate the number of design elements & interconnections to reduce their failure opportunities.

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3.8. Simulation and Modeling

3.8.1. Description

Simulation is a method to model the device functionality and reliability performance of the finished product or part of it, which uses process element models, package physical and materials models, and design guidelines to validate the product functionality and performance over lifetime.

With increasing complexity and diversity of silicon-based semiconductor products, it becomes virtually unworkable to verify reliability with only stress experiments on products. Simulations can provide orders of magnitude larger parametric variation than validation on actual products only (provided that the technology supports the reliability models). This is due to being able to setup worst case conditions for multiple fail modes for mission profiles.

Costs may include addition of resources for simulation program development or purchase and data analysis. Benefits may include mitigating defects in design that otherwise would promulgate to manufacturing.

3.8.2. Relation to Product Life Cycle

Performed on all products during the design phase and possibly during the evaluation phase. May be used during production to aid in debug or Failure Analysis (FA). Simulation should always be used for every significant silicon pass.

3.8.3. Application and Relevance

Verifies functional operation of the product in addition to highlighting process, voltage and temperature sensitivities related directly to the design and process parametric behavior including margins.

3.8.4. Limitations and Exceptions

In general, not intended for use after the product has been ramped up to full production (i.e., after initial release of the product), except to support Failure Analysis (FA) in some cases.

3.8.5. Metrics and Meaning of Values

Direct simulation of specified parameters, functions and margins, parameter fit to empirical data, confidence bounds, fault coverage values, coverage of requirements and other appropriate metrics.

3.8.6. References

- AEC-Q100-007: Fault Simulation and Fault Grading
- JEP122: Failure Mechanisms and Models for Silicon Semiconductor Devices
- JEP148: Reliability Qualification of Semiconductor Devices Based Upon Physics of Failure Risks and Applications Assessments
- SAE J3083 Reliability Prediction for Automotive Electronics Based on Field Return Data

3.8.7. Examples

Illustrations of device validation coverage challenges, where simulation can add confidence/coverage:

- Electro-migration (EM) cannot be sufficiently accelerated in HTOL to achieve end of life. EM is driven by current and temperature. By the time the temperature objective is reached for equivalent EOL stress, other mechanisms have far exceeded the end of life (i.e., TDDDB and BTI).

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- BTI and Hot Carrier Injection (HCI) have opposite worst-case conditions. BTI is static stimulus and HCI is maximum frequency stimulus (for digital circuits and some analog). For analog, standby or static inputs is often the worst case for BTI whereas mission mode is often worst case for HCI. For some technologies, HCI worst case can be at cold temp while BTI is always at high temp.
- Package and product construction simulations, modeling and virtual prototyping are useful to optimize the design and understand stresses in critical locations. Examples are thermal thermomechanical, and electrical modeling.

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3.9. Characterization

3.9.1. Description

The process of collecting and analyzing data to understand the attributes, behavior and limitations of a process and product. The characterization is performed to generate and validate the product specification or datasheet and process limits. The intent is to look at parametric performance of the product with temperature, voltage, frequency, etc. and determine areas that need continuous monitoring for wafer fab, assembly and test. Characterization needs to be statistically based.

Statistical based characterization needs to be performed to significant high confidence limits. This can be accomplished through understanding the sources of variation of the underlying manufacturing processes. The following considerations are important:

1. Bulk analysis requires very large sample sizes and many lots to include enough sources of variation and events.
2. Alternately, parts subject to characterization can come from intentionally skewed material as a function of process technology or assembly technology corner lots.
3. Also, sub-population of parts sorted to contain extreme parametric values or products sourced from post stress characterizations such as, but not limited to, V_{stress} or unclamped inductive stress (UIS) can also be potential candidates for characterization.

Analysis of the effect may be data driven through accepted statistical methodologies, application level characterizations, or product-level accelerated life or environmental stress testing, to help determine if an opportunity exists to center the technologies, optimize the design, or tighten the limits to sort out the less-than-optimally performing material.

Costs may include additional testing for varying parameters such as temperature, voltage, frequency, etc. Costs may also include the manufacturing of corner lots whilst varying parameters such as V_{tn} , V_{tp} , D_{cap} , R_s , etc. Benefits may include centering of the process and establishing a more accurate process and test limits.

3.9.2. Relation to Product Life Cycle

Typically performed on all new and changed products involving new designs or processes, at wafer probe or final test. Characterization can also be useful in diagnosing low yield trends or performance shift trends.

3.9.3. Application and Relevance

Establishes the functional and parametric performance of the product by determining the electrical and process parametric and performance limits. The "sweet spot" of the process is then fed back into manufacturing where it can be controlled.

Another useful output of characterization is overlapping distribution plots based on temperature, voltage, or other swept conditions/variables. For example, plotting three distribution curves on the same chart, one each for Hot, Room, Cold (or V_{min} , V_{typ} , V_{max}). Analyzing these distributions individually can help when defining temperature-based guard bands, selecting production test conditions, and having a better understanding of the statistical results than lumping all data into one C_{pk} / $StDev$.

3.9.4. Limitations and Exceptions

In general, not intended for use after the product has been ramped up to full production (i.e., after initial release of the product), except to support diagnoses of low yield trends or performance shift trends in some cases.

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3.9.5. Metrics and Meaning of Values

Mean, minimum, maximum standard deviation, sample size, Cp, Cpk vs. datasheet or test limits, temperature, voltage, frequency, and process corner variables (e.g., V_t , L_{eff} , R_s , D_{cap}). Determines capability.

3.9.6. References

- AEC-Q003: Characterization
- AEC-Q100-009: Electrical Distribution Assessment

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4. MANUFACTURING

4.1. Process Failure Mode and Effect Analysis (PFMEA)

4.1.1. Description

A process performed by subject experts that identifies potential failure modes and their effects on the system and User, estimates their severity, occurrence and detection, and identifies possible causes and controls. The PFMEA document identifies the risks associated with something potentially going wrong (creating a defect - out of specification) in the production of the product. The FMEA identifies what controls are placed in the production process to catch any defects at various stages in the process. The PFMEA can also provide a relative ranking (action priority) based on the risk and effect associated with the severity, occurrence and detection of a particular failure mode. This can facilitate prioritization of resources in implementation of controls in the production process. In summary, the FMEA is essentially a collection of expert knowledge and lessons learned from other related processes and products.

4.1.2. Relation to Product Life Cycle

PFMEAs are performed on all new or changed products, processes and systems after the development and before implementation of the process flow. This is a living document that can change upon establishment of new processes, tools, or methods as part of continuous improvement efforts and should be periodically reviewed for accuracy or relevance.

4.1.3. Application and Relevance

PFMEAs identify all the known potential modes of failure in process, their risks and effects, and how to control them.

4.1.4. Limitations and Exceptions

PFMEA is not applicable to a process that is being replaced or discontinued (reaching End-of-Life).

4.1.5. Metrics and Meaning of Values

Action Priority (AP) used to prioritize which failure mode or mechanism is most influential to product failure.

4.1.6. References

- AIAG & VDA: FMEA Handbook
- JEP131: Potential Failure Modes & Effects Analysis (FMEA)

4.2. Statistical Analysis of Variance

4.2.1. Description

Mathematical/statistical procedure for determining the variables in a process (i.e., manufacturing parameters) that is related to one or more specific electrical or other parameters of a given product. It splits the aggregate numeric variability found inside a data set into systematic and random factors.

Costs may include designing and conducting experiments and analyzing the resulting data. Benefits may include improving the product and/or process.

For example, a common tool to use is known under Analysis Of Variance (ANOVA).

4.2.2. Relation to Product Life Cycle

Applicable anywhere in the zero defects flow (see Figure 1) where data is collected (e.g., design of experiments) for variation analysis.

4.2.3. Application and Relevance

Can be used on any group of process parameters or device characteristics with the goal of achieving optimum yield, function, and/or reliability.

4.2.4. Limitations and Exceptions

Not intended for use with a product that is fully mature, if a failure never occurs or is entering obsolescence.

4.2.5. Metrics and Meaning of Values

Hypothesis testing, statistical significance, degrees of freedom, variability analysis.

4.2.6. References

- NIST/SEMATECH e-Handbook of Statistical Methods

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4.3. Control Plan

4.3.1. Description

A control plan outlines the product/process characteristics and the associated process variables to ensure capability (around the identified target or nominal) and stability of the product over time. Cpk of Critical Characteristics of a process, for example, is one method utilized in a Control Plan to measure stability. A Control Plan also includes, for some parameters, an Out of Control Action Plan (OCAP) that describes the required reaction if excursions – so called out-of-control observations – are encountered.

4.3.2. Relation to Product Life Cycle

Performed for all manufacturing processes after the design of component, arrangement of process flow, and completion of the FMEA. This is a living document that can change upon new lessons learned and should be periodically reviewed for accuracy or relevance.

4.3.3. Application and Relevance

Identifies the monitors, tests and screens that measure the performance of the process in the manufacture of the product. Specifies control criteria, methods, equipment and frequency of controls (e.g., use of X-bar-R chart, how to set control limits).

4.3.4. Limitations and Exceptions

None.

4.3.5. Metrics and Meaning of Values

Items to be recorded, observed, and measured, method of data analysis (e.g., Cpk, X-bar-R), equipment used for measurement/test, frequency of test, sample size, and datasheet or Customer spec.

4.3.6. References

- AIAG APQP: Advanced Product Quality Planning & Control Plan

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4.4. Statistical Process Control

4.4.1. Description

Statistical process control (SPC) involves using statistical techniques to measure and analyze the variation in processes. Most often used for manufacturing processes, the intent of SPC is to maintain product quality and parameter stability as a result of statistically controlled processes to justify fixed targets and limits. SPC is used to monitor the consistency of processes used to manufacture a product as designed. It aims to keep processes under control.

4.4.2. Relation to Product Life Cycle

SPC can be used on all hardware components, software, and systems at any point in the manufacturing process where variability exists and needs to be controlled.

4.4.3. Application and Relevance

One goal of SPC is to ensure process capability, which is a measure of the ability to consistently produce to the required specifications without defects. Identification and control of random variation inherent within the process, as well as identification and elimination of special causes from external sources achieve this.

4.4.4. Limitations and Exceptions

Unable to apply to a process that is not in statistical control (i.e., a non-normally distributed process step).

4.4.5. Metrics and Meaning of Values

SPC has many metric values. Most common are the capability indices, Cp, Cpk, Pp and Ppk. Cp and Pp, the process capability (Cp) and process performance (Pp) indices, defines a process in terms of its parameter spread with respect to the defined limits of a specification. The definition of C and P can be found in the AIAG SPC manual. It is a function of two variables, calculated as the width of the specification divided by the process spread. Cpk and Ppk, the location indices, indicates the location of the center of the actual distribution curve with respect to the target value.

4.4.6. References

- AIAG SPC: Statistical Process Control
- AIAG PPAP: Production Part Approval Process
- JESD557: Statistical Process Control Systems

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4.5. Lot Acceptance Gates

4.5.1. Description

Testing or stressing of a sample of finished product from a lot to determine the fitness of that lot for further manufacture or shipment to the User.

Costs may include tested samples, time delay in shipping material until results validated, testing, failure analysis, and test efficiency with sample size. Benefits may include identifying and preventing "catastrophic" issues.

4.5.2. Relation to Product Life Cycle

Intended for use with all products and technologies. Most frequently performed at final test, but also can be performed at the wafer level (e.g., kerf tests, wafer/die sort) and anywhere where a previously discovered and corrected problem needs to be monitored.

4.5.3. Application and Relevance

Potential for detecting and flagging lots exhibiting significant anomalous characteristics at the Supplier, that may cause a higher-than-normal level of failure anywhere in the manufacturing lines at the User or even in the application (generally known as Maverick lots), before they move forward in the material flow. It may be used as part of a control plan for PFMEA or DFMEA item with high AP (Action Priority)

4.5.4. Limitations and Exceptions

May always be used but is much less effective for large lots and/or small samplings.

4.5.5. Metrics and Meaning of Values

Sample size, number of fails, test conditions, and frequency of test.

4.5.6. References

- JESD16: Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)
- JESD50: Special Requirements for Maverick Product Elimination
- JESD74: Early Life Failure Rate Calculation Procedure for Electronic Components

4.5.7. Examples

- Incoming Inspection
- Wafer Acceptance
- Parametric Wafer Test
- Optical Inspection
- Optical Inspection
- Bond Line Thickness
- Electrical Test ATE @ hot, room and/or cold
- Lot Acceptance into Finished Good Stores

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4.6. Audits (Management System, Manufacturing Process and Product)

4.6.1. Description

Audits are checks on whether facilities are managed adequately per industry standards such as IATF16949.

4.6.2. Relation to Product Life Cycle

Audits can be performed at any time. Self-audits can be performed by the Manufacturer/Supplier to determine weaknesses or in preparation for a Customer audit. Customer audits are performed in alignment between Supplier and User on new facilities, as a condition of sale or if there is a failure issue to address.

4.6.3. Application and Relevance

All components and technologies that must go through a manufacturing process. It addresses zero defects by uncovering weaknesses in the quality process for the Manufacturer/Supplier to fix or improve on.

4.6.4. Limitations and Exceptions

Audit results are dependent on the iterative and collaborative rapport between auditor and auditees and availability/completeness of records.

4.6.5. Metrics and Meaning of Values

Audits are summarized by numerical or letter scores to inform the manufacturing site where their progress lies and whether degrees of continuous improvement need to be implemented to satisfy the User.

4.6.6. References

- International Automotive Task Force – IATF16949

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5. TEST

5.1. Part Average Testing

5.1.1. Description

A system for designing, analyzing, and controlling manufacturing and test parameters (electrical and/or physical) of the device to ensure product quality. This method is designed to remove outliers from a given product population. Both real time PAT (probe and final) and statistical post processing (probe and final) are acceptable methods. A robust method should be performed on non-normal parametric distributions.

5.1.2. Relation to Product Life Cycle

Performed on products and technologies at various points within and after the manufacturing process. PAT should be used for electrical parametric testing in wafer probing and packaged final test. Dynamic testing is preferred over static.

5.1.3. Application and Relevance

Eliminates outliers from further production and shipment to Users.

5.1.4. Limitations and Exceptions

PAT can only be effectively performed on test parameters that are stable, in control and ideally normal-distributed, otherwise unexpected consequences impacting yield can occur. Studies show that performing PAT only at wafer probe provides insufficient User protection. Using PAT at wafer probe is the first quality gate, but the rest of the downstream manufacturing process adds potential variability from a myriad of sources - variability that causes more PAT outliers at package test. It is recommended to use PAT on downstream manufacturing processes as well as wafer probe since these steps add variability that can result in PAT outliers.

5.1.5. Metrics and Meaning of Values

(Robust) Mean and (Robust) Sigma.

5.1.6. References

- AEC-Q001: Guidelines for Part Average Testing
- JESD50: Special Requirements for Maverick Product Elimination and Outlier Management

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5.2. Statistical Bin Yield Analysis

5.2.1. Description

A system for analyzing measurements of test parameters/bins with the goal of reducing variation and detecting potential latent defectivity.

5.2.2. Relation to Product Life Cycle

Performed on all products and technologies at wafer probe and package final test.

5.2.3. Application and Relevance

Applies SPC on test parameters/bins to identify maverick lots.

5.2.4. Limitations and Exceptions

None.

5.2.5. Metrics and Meaning of Values

Cpk/Ppk versus the historical (ongoing) bin fallout pattern and looking for a shift in the process, increased variation (mean, sigma), and outliers.

5.2.6. References

- AEC-Q002: Guidelines for Statistical Yield Analysis
- JESD50: Special Requirements for Maverick Product Elimination and Outlier Management

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5.3. Data Collection, Storage and Retrieval

5.3.1. Description

The measurement, storage, archiving, and retrieval of data. This is used for rapid response to faulty quality and reliability metrics, to solve problems possibly related to the product manufacture, or trends over time.

5.3.2. Relation to Product Life Cycle

Intended for use with all products and technologies, anywhere data can be obtained to draw conclusions. Specific areas include spec revisions, qualification/PPAP, quality records, material traceability, process, test and Customer return data.

5.3.3. Application and Relevance

Rapid availability of data will speed up containment of issues, leads to continuous improvement activities, and allows rapid risk assessment. Benchmark for quality improvement.

5.3.4. Limitations and Exceptions

As agreed in Supplier-User Contracts.

5.3.5. Metrics and Meaning of Values

Data collection frequency and duration of data storage.

5.3.6. References

No standard available and specified in Supplier-User Contracts.

5.3.7. Examples

Data centers.

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5.4. Screens

5.4.1. Description

Test screens are tools to guard band device performance and reliability robustness against any defect induced failure mechanism.

Costs may include equipment, yield impact, and more rigorous test development and testing time. Benefits may include better protection of Users from yield degradation and field failures.

5.4.2. Relation to Product Life Cycle

Intended for use with all products and technologies. Most frequently performed at final test, but also can be performed at wafer level and anywhere where a previously discovered and corrected problem needs to be monitored by testing. These can be directly on the product, or test structures and surrogate test vehicles (e.g., sawing lane or gate oxide screens).

5.4.3. Application and Relevance

Screening tests provide parametric and functional compliance after critical processes to provide immediate feedback on opportunities for improvement.

5.4.4. Limitations and Exceptions

Screening may not capture all types of latent defects and is not designed to address - but should not impact - intrinsic reliability margin.

5.4.5. Metrics and Meaning of Values

Number of defects, defectivity (DPM), failure modes (bins), electrical parameter variables, and efficiency.

5.4.6. References

- JESD16: Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)
- JESD50: Special Requirements for Maverick Product Elimination
- JESD74: Early Life Failure Rate Calculation Procedure for Electronic Components
- MIL-PRF-19500
- MIL-STD-883

5.4.7. Examples

- Defect detection via IDDQ leakage test, high voltage stress test (HVST), very low voltage test (VLVT), correlated parameters and burn-in.
- Improvement of effectiveness and efficiency of screens using advanced outlier methods.
- Optical screening by high-speed inspection on 100% of wafers and 100% of die on a few known quality-sensitive layers to identify and disposition individual at-risk wafers or product die.

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6. APPLICATION AND CAPABILITY

6.1. Industry Standards

6.1.1. Description

Agreements among world leaders in part manufacture and use that set benchmarks for testing of products to determine fitness for use.

6.1.2. Relation to Product Life Cycle

Standards apply to many locations within the material/process flow and offline. Intended for use with all wafer fab processes and package technologies.

6.1.3. Application and Relevance

Provides standard methods of testing that is applicable for both Suppliers and Users and offers benchmarks of performance that can be applied across many devices, processes and materials.

6.1.4. Limitations and Exceptions

Not intended for use when there is a need to overstress (i.e., greater acceleration factor) or understress (i.e., product is inherently weak). If the product has features not covered by any current industry standard. Established industry standards benchmark may not fully reconcile with demands from application specific requirements and/or End-User environment. Also, it may not align with some failure mechanisms that fall outside historical data/experience (new technologies/ materials or different acceleration factor, etc.).

6.1.5. Metrics and Meaning of Values

Metrics are as defined in each applicable standard.

6.1.6. References

AEC, JEDEC, AIAG, IEC, SAE, VDA, IATF (refer to Section 1.2)

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6.2. Environmental Stress Testing

6.2.1. Description

A collection of methods and tests designed to ensure that products meet all the quality and reliability requirements agreed by Suppliers and Users. Accelerated tests are used to establish a baseline to assess wear out and defectivity concerns. It also assesses resistance of an individual product to the degrading effects of natural elements and actual conditions that might exist in the field, including physical, mechanical, electrical, and environmental stressing.

For silicon design, defects include unusual temperature dependencies, performance irregularities and marginalities, and functional problems. For wafer fabrication process, defects include time/temperature defects, unanticipated infant mortality issues, latent defects, and wear out mechanisms. For packaging, defects include structural integrity, unusual package related anomalies (delamination, popcorn) and sensitivities, and assembly related defects that affect quality and reliability. Gross issues are detectable.

6.2.2. Relation to Product Life Cycle

Relevant tests performed on all new and changed products either as a part of the initial product qualification by the Supplier, for qualifying process changes, or as an extended qualification (i.e., failure mechanism monitoring).

6.2.3. Application and Relevance

Identifies inherent weaknesses in the design, process, or assembly during qualification of the product. Any or all of these can be corrected prior to release for use. It may also be useful to assess issues during full production.

6.2.4. Limitations and Exceptions

None.

6.2.5. Metrics and Meaning of Values

Number of fails vs. sample size, stress test parameters (e.g., temperature, voltage, current). Data can be used to pareto the common failure mechanisms. Can also be used to justify improvements in design, process, and packaging.

6.2.6. References

- AEC-Q10x Standards, AEC-Q200
- JESD22 Test Methods
- JESD94: Application Specific Qualification Using Knowledge Based Test Methodology
- JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid-State Surface Mount Components
- SAE J1879 Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
- SAE J1211 Handbook for Robustness Validation of Automotive Electrical/Electronic Modules

6.2.7. Examples

Example of a test list e.g., AEC-Q100/101 Table 2: Qualification Test Methods.

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6.3. Stress-Strength Analysis

6.3.1. Description

The analysis of the probability of failure based on the stress exceeding the strength of a given part.

Stress-Strength Analysis is a method that uses test-to-fail principles and the analysis of the resulting failure distribution data. Emphasis is on stress-to-fail rather than time-to-fail, e.g., HASS, HALT, BST, BPT. In that sense it is different from environmental stress testing and intrinsic wafer level reliability tests (TDDB, QBD, HCI, BTI, EM), where always time-to-fail is included.

Costs may include testing, material costs, statistical software and data analysis resources. Benefits may include design margin knowledge and robustness validation.

6.3.2. Relation to Product Life Cycle

Used for all products and technologies at any stage during the development. It can also be modeled in the design phase if enough information regarding stress and strength distribution is available upfront (e.g., via generic data).

6.3.3. Application and Relevance

Determines the amount of design or process margin for a given application to indicate the potential probability of failure.

6.3.4. Limitations and Exceptions

Usually not needed for already characterized industry standard commodity products and for products that are mature. It can still be useful in case of unexpected/unknown failure modes.

6.3.5. Metrics and Meaning of Values

Design margin for specific and critical stress parameter derived from the mission profile and/or DFMEA. This can be a numerical factor regarding the product specification or an overall all robustness assessment (e.g., in HASS, HALT).

6.3.6. References

None

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6.4. Systems Engineering

6.4.1. Description

An approach to align the system design with the User application. The practice of systems engineering involves translating User needs into system requirements that can then be realized through architecture and design. A system consists of a set of entities and their relationships. Electronic components within an automotive system may themselves be complex products requiring system engineering practices. These complex systems may be decomposed into entities which involve individual requirements. A process of integration, verification, and validation is then employed at each level. For example, individual entities may include hardware and/or software.

Costs may include engineering resources for both User and Supplier throughout the product life cycle. System engineering activities to incorporate “off the shelf” products are reduced in time and concentrated at or after the “off the shelf” product development. Benefits may include co-operative analysis and/or development to drive (or choose) the individual sub-components of the system such that the system will meet its requirements.

6.4.2. Relation to Product Life Cycle

Systems engineering activities apply to all aspects of the product lifecycle from concept to production, to use life and finally disposal. This may include but is not limited to hardware requirements, design, software requirements and development, characterization, verification that the product requirements have been met, and validation that the product achieves and maintains its purpose in the larger automotive system.

6.4.3. Application and Relevance

To achieve the zero defects goal includes consideration of system-level architecture to incorporate Design For Reliability (DfR), Design For Manufacturability (DfM) and Design For Test (DfT). Early in development, product specifications and verification plans must ensure that system requirements will be met. In addition, products with Functional Safety Requirements have standards defined that incorporate systems engineering (Reference: ISO26262). Collaboration between system developers and product providers can improve the overall system quality. Areas such as lifetime, performance, and safety can be considered.

Joint development between system developer and product Supplier can include co-engineering activities to cooperatively define and validate a product for use in a specific automotive system design. Joint development is defined as a system-specific development project where the system developer translates the system requirements to advise the product Supplier on the features and datasheet requirements for a new product and often supplies funding for the development. For joint development, the product Supplier should:

- Consider the system mission profile and application lifetime for a product Design For Reliability (DfR) and reliability assessment.
- Incorporate the requirements for the system use conditions in the design and/or validation of the product’s performance.
- Incorporate requirements for safety including jointly defined safety mechanisms that can be used to detect and alert the system of the product’s random faults.

Automotive systems can also incorporate “off the shelf” products. An “off the shelf” product is one that was not specifically designed for or with a system designer for their specific use. For “off the shelf” product use in an automotive system, when the system designer provides information on system requirements for an “off the shelf” product, the product Supplier can:

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- Analyze the product lifetime against the mission profile and application lifetime for the system.
- Provide the datasheet specification.
- Provide information on safety mechanisms that can be used to detect and alert the system of product's random faults.

6.4.4. Limitations and Exceptions

May not be needed for industry standard commodity products, low-complexity products, or mature products.

6.4.5. Metrics and Meaning of Values

Key metrics encompass the effectiveness of the system with respect to the needs, requirements, and mission accomplishment. Six sigma and/or statistical design tolerances may be applied to performance attributes, product development goals, and learnings may contribute to enhancing next products under development.

6.4.6. References

- AIAG APQP: Advanced Product Quality Planning & Control Plan
- ISO/IEC/IEEE15288
- EIA632 Processes for Engineering a System (2015)
- INCOSE Systems Engineering Handbook, MITRE Systems Engineering Guide (SEG)
- ISO26262 Road Vehicles – Functional Safety
- Automotive SPICE– VDA QMC Automotive SPICE Process Assessment Model
- *Design Structure Matrix Methods and Applications*, S.D. Eppinger and T.R. Browning
- *Engineering a Safer World: Systems Thinking Applied to Safety*, N. Leveson

6.4.7. Examples

The System Engineering V-Model is a fundamental principle of Systems Engineering, in the form of a conceptual diagram which shows:

- The various sets of information which are necessary for system development
- The relative relationships between the sets of information

It is intended to support understanding of requirements, specifications and the various tests which are necessary to develop complex system products.

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6.5. Product Derating

6.5.1. Description

The practice of using a product in a narrower environmental and/or operating envelope than its Manufacturer/Supplier designated limits. Derating can be employed to achieve various goals. The method of derating may need to be adjusted depending on the goal as well.

Maintain an appropriate balance between application design cost and derating limits. While design margin is desirable, stacking of multiple sources of margin can result in high costs and lost opportunities.

6.5.2. Relation to Product Life Cycle

Performed on all products, technologies, and applications. Focus is application design, depending on many application requirements including reliability, criticality, functional performance needs, etc.

6.5.3. Application and Relevance

This practice has been used to provide greater functionality margin within the Manufacturer's/Supplier's specifications, and with the assistance of the Manufacturer/Supplier, potentially extend useful life or increase reliability.

6.5.4. Limitations and Exceptions

Only intended for use with mature products in a mature application. Derating can be implemented with detailed alignment between User and Supplier.

6.5.5. Metrics and Meaning of Values

Operating conditions such as temperature, humidity, power consumption, operating voltage, and output current or fan out. NVM erase and write cycles.

6.5.6. References

None.

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7. CONTINUOUS IMPROVEMENT METHODS

7.1. Wafer Level Process Monitoring

7.1.1. Description

The kerf or sawing lane (space between die on a wafer) contains a multitude of structures that serve different purposes during wafer production. Among these are structures that are needed for the wafer processing itself (inline), such as lithography alignment structures and structures for measuring layer thicknesses. It also contains structures for physical analysis of the processing, like critical topography structures for construction analysis and fields for measurement of the doping profiles (e.g., by SIMS). Representative structures for electrical analysis of the processing are used for characterization on the wafer. These structures are used, for instance, for measuring sheet resistances and transistor parameters. The kerf also contains special structures for reliability monitoring of the process with fast WLR (wafer level reliability) of mechanisms like TDDB, QBD, HCI, BTI, EM.

Costs may include designing and testing monitors and yield loss. Benefits may include early detection of potential problems, analysis and control of specific failure mechanisms and providing a statistical basis for analysis and screening.

7.1.2. Relation to Product Life Cycle

Performed on all major wafer fab process steps and new technologies. The kerf is part of the chip design and is tested during various points in wafer fabrication.

7.1.3. Application and Relevance

Able to rapidly test for specific failure mechanisms early in manufacture so that faulty wafers or lots can be fixed or scrapped.

7.1.4. Limitations and Exceptions

None.

7.1.5. Metrics and Meaning of Values

Kerf or test pattern time to fail or degree of degradation, sample size, frequency of test, and pareto.

7.1.6. References

None.

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7.2. Process and Product Improvements

7.2.1. Description

Changes to the manufacturing process, product design (including firmware modifications to address any type of bugs or application issues), materials, construction and testing that improve the product functionality, manufacturability, testability and/or reliability.

Costs may include validation testing, User validation and implementation of the change. Benefits may include improved product functionality, quality, cost and/or delivery.

7.2.2. Relation to Product Life Cycle

Applies to all products and technologies, anywhere in the flow where agreed major changes are made (e.g., design, manufacture, test).

7.2.3. Application and Relevance

Change in material or process or embedded software (firmware), either to address a root cause issue or as an evolution of a process or design, to improve product function, yield and/or reliability. Attention should be paid to change control and risk management (e.g., FMEA update).

7.2.4. Limitations and Exceptions

Not intended for use with a product that is fully mature or is entering obsolescence.

7.2.5. Metrics and Meaning of Values

Cost save, cycle time reduction, implementation time, and quality/reliability improvement.

7.2.6. References

- JESD46 Customer Notification of Product/Process Changes by Semiconductor Suppliers
(Note: Customer specific requirements for change management always have to be considered)

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7.3. Product Reliability Monitoring

7.3.1. Description

Periodic reliability testing of a sample of representative products or test vehicles with the purpose of monitoring whether a process excursion occurred to create a defect that could be seen in the field. Verify that the process is in control.

Costs may include material, labor, equipment, overhead, and failure analysis. Benefits may include feedback to fix potentially ongoing product/process issues.

7.3.2. Relation to Product Life Cycle

Post-production test sampling for all products and technologies.

7.3.3. Application and Relevance

Ongoing evaluation of reliability capability in order to fix any issues that can be applied to subsequent manufactured product.

7.3.4. Limitations and Exceptions

Not intended for use when the process and/or product are mature.

7.3.5. Metrics and Meaning of Values

Number of fails, sample size, test frequency, and test conditions.

7.3.6. References

- JESD659: Failure Mechanism Driven Reliability Monitoring

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7.4. Defect Monitoring

7.4.1. Description

Achieving zero defects is dependent upon the combined efforts of all Suppliers at the semiconductor product level. Detecting defects through monitoring and eliminating them before they are incorporated into any finished goods is key to any successful ZD program.

Defect monitoring is the systematic process of periodically observing or checking the quality of production materials. Defect monitors can include electrical measurements, visual inspections, physical inline or de-processed analysis, etc. and can be performed on a sampling of products or structures or bare test wafers.

Defects could be introduced in the manufacturing processes by many diverse influences, including process, equipment, environment and human factors. A portion of these defects may pass electrical test and burn-in but fail in the field when activated by the environment. Test screens are described in Section 5.4.

Defect inspection is applied to production products at critical stages throughout the production flow. Tool monitoring inspections are implemented based on time interval or usage frequency.

Costs may include equipment and defect inspection, potential scrap of material. Benefits may include yield and reliability improvements, especially reduction of early field failures.

7.4.2. Relation to Product Life Cycle

Applies to all products and technologies. Defects have an impact on yield and reliability and therefore control and reduction of defects is mandatory for zero defects. Defect reduction decreases the probability of defect related reliability fails. Fabs at mature yields primarily experience baseline random defects and from excursions (e.g., particles) contributed by the environment or an out-of-control process tool. Devices developed under advanced design rules may show significant changes in sensitivity for defect types and contributing sources, or in spatial signatures. This will depend on process maturity.

7.4.3. Application and Relevance

Detectability is limited by several factors, including capability of equipment, available capacity and sampling rate and defect characteristics (e.g., size and shape and surrounding structures).

Using statistical methods, like PAT, allow for identification of dies with outlier defectivity that have a greater likelihood of containing defects. The outlier die data can be used to reject dies or to merge with traditional PAT techniques for electrical test data to further reduce reliability escapes (refer to Section 5.1).

7.4.4. Limitations and Exceptions

Detectability is limited by several factors, including capability of equipment, available capacity, sampling rate and defect characteristics (e.g., size and shape and surrounding structures).

7.4.5. Metrics and Meaning of Values

Defects can be of random, systematic or latent nature. Typical metrics include: defect type pareto, defect wafer map, defect density, kill ratios, SPC charts and outlier die.

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7.4.7. References

- JESD659: Failure Mechanism Driven Reliability Monitoring

7.4.8. Examples

A robust monitoring strategy in the wafer fab may consist of several overlapping components.

- Line Monitoring uses sensitive module-level inspections and review on product wafers to accomplish defect discovery, defect reduction DOE and yield learning. The output is a Pareto of the defect population types at critical steps.
- Excursion Monitoring is a higher sampling-rate product wafer inspection used on layers at risk to periodic out-of-control defect populations to establish traceability and keep non-conforming material from entering the supply chain. The output is an SPC chart.
- Tool Monitoring is the frequent and routine validation of the cleanliness and proper function of individual process tools and chambers. It can be conducted using bare test wafer inspections or on product wafers. The results are plotted on an SPC chart and are used to isolate tools that are producing defects, to identify the best performing tools and for continuous improvement of fab defectivity.
- Periodic reticle inspection monitors for contamination defects that can become repeating lithographic defects printed in every shot.
- Process controls in the back-end of assembly lines: e.g., inspection of the six sides of the final package.

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8. PROBLEM SOLVING

8.1. Problem Solving Techniques

8.1.1. Description

A problem-solving methodology for product and process improvement. It is a team-oriented approach used to identify root cause, contain and correct the problem, verify the problem is understood and solved, and prevent its recurrence. It is also used as a reporting tool to document the issue for a User. The list in Table 4 gives examples of available tools.

Table 4: Example Tools for Problem Solving

Tool/ method	Description
8D	Tool for structured approach and recording results of problem-solving process.
Is / Is Not	Method for defining in a structured manner the problem definition.
Fishbone/Ishikawa	tool for brainstorming and identifying potential problem root causes, particularly useful when a problem has a combination of root causes.
A3/SPS	Structured problem solving and continuous improvement approach. It provides a simple and strict approach systematically leading towards problem solving. Useful in that everything is on a single A3 page Includes fishbone and 5 whys/ is/is-not.
5 Why	5 Whys is an iterative interrogative technique used to explore the cause-and-effect relationships underlying a particular problem. The primary goal of the technique is to determine the root cause of a defect or problem by repeating the question "Why?" Each question forms the basis of the next question.
Fault Tree Analysis	Fault tree analysis is a logical, structured process that can help identify potential causes of system failure before the failures actually occur. Fault trees are powerful design tools that can help ensure that product performance objectives are met. Can help to ensure that root cause is identified.

8.1.2. Relation to Product Life Cycle

This discipline can be used on all products and technologies throughout the manufacturing process at the Supplier or User.

8.1.3. Application and Relevance

By identifying and correcting the real root causes, with the results to be applied to similar products/processes. Lessons learned should be considered at key stages of the product development process.

8.1.4. Limitations and Exceptions

Which tool should be used strongly depends on the individual case and cannot be covered by a general recommendation.

8.1.5. Metrics and Meaning of Values

Cycle time, effectiveness of resolved corrective/preventive action, and field/warranty return rates.

8.1.6. References

- JESD671: Component Quality Problem Analysis and Corrective Action Requirements

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8.2. Failure Analysis Process

8.2.1. Description

Failure analysis is the process of collecting and analyzing material and data to determine the cause of a failure. The output is often a determination of root cause and corresponding containment and corrective action.

When a failure occurs within all tiers of automotive manufacturing or in the field, a User may request Failure Analysis (FA) of its Supplier. User may request FA of the Supplier that is time-bounded based on urgency to reduce impact and protect supply continuity and field reliability. However, there are certain widely used guidelines in the industry for a successful failure analysis, such as described below.

The (FA flow is influenced by a multitude of factors: the device, the application, the device stresses within the application, the point of failure, the failure rate, the failure mode, the failure attributes, the toolset available for FA, and the failure mechanism. A standard failure analysis FA flow cannot be recommended due to the myriad of combinations. However, a number of recommended steps are given below.

First, the non-destructive failure analysis should be performed, starting with electrical verification of the failure within the Supplier's test environment to insure reproducibility. If the failure cannot be reproduced at the Supplier, collaboration between User and Supplier may be necessary to better align the test environment to the application, or agreement that the issue did not originate with the Supplier. Once the failure is confirmed, it should be electrically characterized to understand influencing factors and symptoms to narrow down the root cause.

After the electrical analysis is completed, the product can undergo physical failure analysis, beginning with fault isolation. This portion of the failure analysis is often destructive. The goal is to reveal the defect or non-conformity that was the root cause of the issue. Once the Supplier determines it is the source of the issue, the Information gathered during electrical and physical failure analysis should be used in creation of an 8D corrective action plan, including root cause corrective actions and containment of the issue, where possible.

For multiple failures with the same failing signature, if agreed upon between a Supplier and User, signature analysis may be utilized in lieu of multiple failure analyses. Signature analysis is the application of only the non-destructive failure analysis for a previously identified symptom with known failure mode or mechanism to confirm the electrical signature matches this known failure mechanism.

8.2.2. Relation to Product Life Cycle

Intended for use with all products and technologies, anywhere in the material flow where there is fallout that requires obtaining more information about the failure.

8.2.3. Application and Relevance

Physically determining the root cause of an issue via product de-processing and chemical/structural analysis provides the organization guidance on how to permanently resolve the issue and limit the impact to User(s).

8.2.4. Limitations and Exceptions

Not intended for use if a failure never occurs. Physical analysis is not needed if a failure is connected to firm ware bug or application issue.

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8.2.5. Metrics and Meaning of Values

Cycle time, cost, equipment availability and utilization, and backlog. The amount of time to complete the initial FA and full FA, and the containment and corrective action are as agreed upon between the Supplier and the User. JEDEC JESD671 provides guidelines for these timeframes.

8.2.6. References

- JESD671: Component Quality Problem Analysis and Corrective Action Requirements

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9. DOCUMENTATION

The User and Supplier should jointly determine the usefulness of each tool per product case. To that extent, Table 5 provides a template for the Supplier to document the tool kit used for a particular product case, which can be used to communicate and document the strategy towards Zero Defects (ZD). If the case deviates from the four covered in Table 3, the template provides a possibility to describe this.

Table 5: Zero Defect Toolkit Overview Template

ZERO DEFECTS TOOLKIT OVERVIEW					
Product					
Case	(1, 2, 3, 4, other)	Describe (if other than case 1, 2, 3, 4)			
Area	Tool	Section	Entry from Table 3 (if applicable)	Applied (Y/N/NA)	Comments
Design	Design FMEA	3.1			
	Redundancy	3.2			
	Built-in Self-Test	3.3			
	Design for Test	3.4			
	Design for Analysis	3.5			
	Design for Manufacture	3.6			
	Design for Reliability	3.7			
	Simulation and Modeling	3.8			
	Characterization	3.9			
Manufacturing	Process FMEA	4.1			
	Statistical Analysis of Variance	4.2			
	Control Plan	4.3			
	Statistical Process Control	4.4			
	Lot Acceptance Gates	4.5			
	Audits	4.6			
Test	Part Average Testing	5.1			
	Statistical Bin Yield Analysis	5.2			
	Data Collection, Storage and Retrieval	5.3			
	Screens	5.4			
Application and Capability	Industry Standards	6.1			
	Environmental Stress Testing	6.2			
	Stress-Strength Analysis	6.3			
	Systems Engineering	6.4			
	Product Derating	6.5			
Improvement	Wafer Level Process Monitoring	7.1			
	Process and Product Improvements	7.2			
	Product Reliability Monitoring	7.3			
	Defect Monitoring	7.4			
Problem Solving	Problem Solving Techniques	8.1			
	Failure Analysis Process	8.2			

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Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	Feb. 26, 2020	Initial Release.