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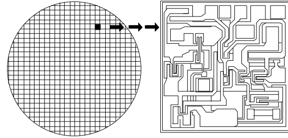
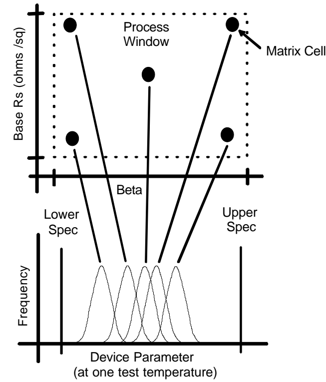
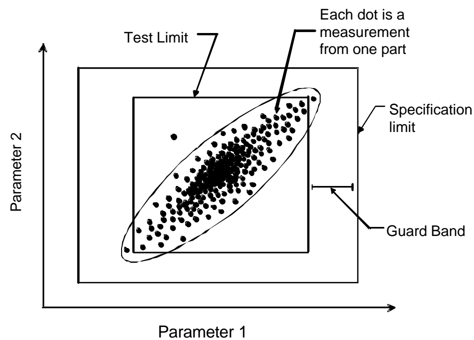
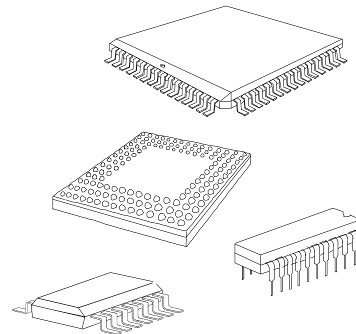




GUIDELINE FOR CHARACTERIZATION OF INTEGRATED CIRCUITS





Automotive Electronics Council
Component Technical Committee

Acknowledgment

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Guideline For The Characterization of Integrated Circuits

1. PURPOSE:

The characterization of ICs is an extremely important function during the development of a new IC or the modification of an existing IC. The purpose of this document is to provide guidance by highlighting important considerations that should be evaluated during development of a characterization procedure. This document is not intended to be a specification on how to perform a characterization. To ensure consistent characterization every company should have a structured and documented characterization procedure. The characterization process should be used to ensure that the design & wafer fab/assembly processes being utilized demonstrate sufficient capability of providing a part that meets the requirements of the customer. The results of every characterization should be documented in a Characterization Report.

2. SCOPE:

This guideline document provides the basis for establishing a procedure for characterizing the electrical performance of Integrated Circuit products. This characterization procedure should be used for new technologies, new wafer fabrication processes, new product designs and significantly modified ICs.

3. DEFINITIONS:

3.1 Device Electrical Parameters

Electrical measurements specified in the part specification for the device, and / or other measurements as indicated by engineering experience for the technology involved.

3.2 Characterization

The process of determining the fundamental electrical and physical characteristics (voltage, frequency, and temperature behavior) of a device based on statistical analysis of experimental data or modeling. This includes the distribution of an electrical parameter as a function of other parameter(s) variation. The graphical presentation of the characterization for a typical electrical parameter is a multivariate hyper - ellipsoid, see Figure 1 (frequently called a Schmoo Plot).

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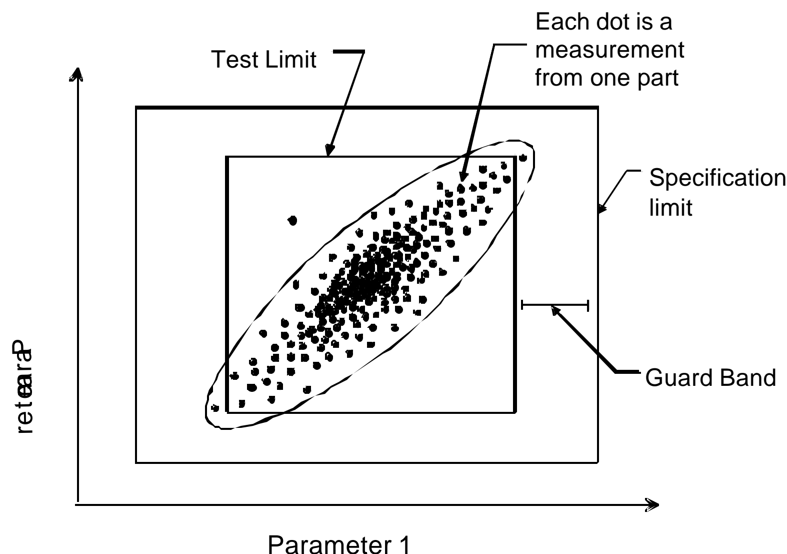

Figure 1 Schmoo Plot

3.3 Criteria For Characterization

A device that meets the following criteria should be considered a candidate for characterization. This criteria should not be considered a limitation but a starting point for factors to consider.

- new chip layout or changes to an existing die that could impact electrical parameters (e.g., die shrink)
- new cell structure(s) which have not been used in production components
- new processing methods or materials
- new operating bias condition requirements (re-characterize at new bias extremes)
- significant increase in operating environmental condition requirements (re-characterize at new environmental extremes)

3.4 Specification Limits (e.g., data sheet limits):

Numerical values of maximum, minimum, and typical electrical parameters specified in the customers part specification or the supplier data sheet. These values are used to determine pass / fail criteria for the characterization.

3.5 Guard Bands:

The difference between test limits and specification limits. Test limits are generally tighter than specification limits to account for tester inaccuracies and other sources of variation.

4. CHARACTERIZATION PROCEDURE:

This guideline is not intended to establish the characterization process / procedure, but is intended to provide an outline of factors that should be considered when establishing a characterization procedure. Every supplier should establish a characterization procedure. The characterization procedure should include the following major activities for the device to be characterized:

- Review of PFMEA (process FMEA), DFMEA (design FMEA) and the related Control Plans or equivalent methods that link failures to the manufacturing process and design process.
- Determination of the characterization method to be used.
- Establishment of the parameters to be characterized.
- Completion of a characterization report.

4.1 Device Characterization:

The characterization of new parts requires a procedure that provides in-depth information about the capability of the part design / process to produce the part. Before beginning the characterization procedure review the Characterization Checklist, see Appendix 1. This characterization procedure should include measuring to the part specification requirements across the operating voltages, frequencies, and temperatures or the use of documented simulation methods. (**Note**: Although not included in the characterization, it is important to determine the ESD, Latch-up, and Generic Leakage capability of a part early in the development cycle as these parameters could have a significant impact on the performance of the part.) The characterization methods used (see Appendix 2, and 3) should be clearly documented in a Characterization Report.

4.2 Characterization Report

The characterization report should include the following:

1. A summary of the PFMEA (Process FMEA) and DFMEA (Design FMEA) and the related Control Plans or equivalent methods that link failures to the manufacturing process and design process.
2. A detailed discussion of the characterization methods used (see Appendixes 1, 2, and 3).
3. A listing of all critical parameters monitored during the characterization. A listing of all critical parameters that do not show a Design Index of 1 or greater (see Appendix 4) or a Cpk of 1.33 to the specification test limits.
4. Discussion of device weaknesses and corrective actions, both design and process related.
5. Containment plans for handling uncorrected part weaknesses and reliability concerns. (*e.g.*, voltage stress test or burn-in to contain gate oxide defects.)
6. The report should be approved by a responsible supplier representative.

The results of the characterization should be shared with the customer (at the discretion of the supplier this sharing may include a hard copy of the characterization report or selected portions of the characterization report).

APPENDIX 1

Characterization Checklist

The following points should be evaluated during the planning stage for product characterization:

- Have all the cell structures used in this product been characterized?
- Has the wafer fab process changed since the cell structure characterizations?
- If the wafer fab process has changed, do the simulation models that will be used for characterization account for all wafer fab process changes?
- If matrix devices will be needed, which process windows should be involved in the matrix? What is the worst case variation in these process windows? (**Note**: The worst case processing variation should be based on the worst case conditions observed during the last six months or expected during normal manufacturing.) Who should participate in making these decisions?
- Are there matrix cell interactions that should be considered?
- How can simulation models be used to simplify and expedite the characterization process? How good are the available simulation models? What is the confidence in the simulation models? What are the risks if the available simulation models are used?
- Have the drift characteristics of the cell structures been characterized? Is a device parameter drift analysis needed as part of this characterization?
- Are there stresses associated with the product package that could affect the initial and late life electrical parameters of the product?
- If matrix units are required, how many (sample size) from each matrix cell? How many process variations need to be characterized? Will the product be characterized beyond the required part specification requirements (hotter or colder temperatures, higher or lower frequencies, higher or lower bias voltages)? Will the software required for the characterization be available when needed?
- Do we know the junction temperatures (hot and cold) that must be evaluated in this characterization? Have the thermal characteristics of the measurement system(s) been considered, see Appendix 3?
- What form will matrix devices be in for the characterization – packaged? .. wafer level? Have packaging requirements been included in the characterization plan?
- Will the ESD, Latch-up, and Generic Leakage capability be evaluated early in the development cycle?
- Are DFMEAs and PFMEAs available for other products manufactured with the same Process Control Limits? Is a new DFMEA and PFMEA required for this product? Who should be involved in the team preparing the DFMEA and PFMEA for this product?

APPENDIX 2

Test Die Selection

One goal of characterization is to discover potential problems during early development when changes can be made quickly, easily, and less expensively. Therefore, caution should be exercised so that pre-testing before characterization is minimized, since it has the possibility of truncating the normal matrix cell distribution and hiding potential problems.

The recommended pre-testing approach is to only eliminate non-functional devices from the characterization sample.

Examples to help define non-functional - the following would be considered test limits for functional devices:

1) Override specification required parametric failures and only perform relaxed spec functional tests (EZ-functional).
2) Widen all specification required parametric limits by a significant digit.

The method of selecting die can have a large effect on the amount of inherent process variation that is included in the data. The main concern is to understand and design for the largest sources of inherent process variation. Due to the number of different process technologies it is the responsibility of the supplier to develop a combination of lots, wafers, and die locations that will provide the inherent process variation.

A thorough analysis of sample size should also consider the following:

1) Which wafers are selected for a cell?
2) Which die locations are selected on a wafer?

APPENDIX 3

Characterization Testing

The die selected for characterization shall be tri-temperature tested. Test temperatures need to be established for room, hot, and cold test. The test setup temperature extremes should be able to duplicate worst case product application junction temperatures.

It should be stressed that the junction temperature of the device in the selected operating condition is the actual characterization target. For example, a low test temperature limit of -55ºC might be required for a -40ºC instantaneous customer need (i.e. operate on cold wake-up) to account for a 15ºC steady state heating during testing. Likewise, a high test temperature limit of 135ºC might be required for a 150ºC instantaneous package test to account for a 15ºC steady state heating during testing.

The bias conditions and subsequent power consumption will determine if there is sufficient energy dissipation to necessitate the need for test temperature correction(s). In some situations an instantaneous condition is assumed that would null the effects of thermal dissipation, while in other conditions a high energy steady-state condition is assumed that would necessitate the use of temperature correction(s).

Example:

Simulate a Customer Junction Temperature of 155ºC -

If the starting temperature of a customer system is ………125ºC
And a thermal gradient (w/bias condition) causes a
temperature increase of ……………………………… 30ºC
Then the customer junction temperature requirement
is …………………………………………………….. 155ºC

Characterization Test Temperature -

The junction temperature to simulate is ………………….. 155ºC
If the steady state heating during testing causes a
thermal gradient (w/bias condition) that
results in a temperature increase of ……………… 15ºC
Then, the required final test setup temperature
(Characterization test temperature) is …………….. 140ºC *

*Note: Additional temperature may be added to this value for guard banding.

APPENDIX 4

Design Index

The idea of representing the goodness or badness of a product's Device Parameter performance (over the worst case expected variation in Key Fab Process limits) with a single value is the reason for establishing a Design Index (DI). A Design Index of 1 or greater for a particular parameter requirement means that the device meets that parameter requirement at all matrix points. (**Note**: A Design Index of less than 1 indicates that a particular parameter will probably cause a higher yield loss during normal production.) This section will discuss the theory behind the DI and how to use it.

In a matrix characterization (or simulation), processing variables are forced to certain values (to form matrix cells) and the product performance is evaluated. The goal of the characterization is to determine if the device performance will stay within specification limits when processing variables are forced to their worst case values, see Appendix 1.

The Device Parameters are the values measured (or modeled), or tests performed, to ensure that the device meets all of the electrical requirements defined in the Part Specification. In general, the Device Parameters measured on parts taken from different cells of the matrix will have different values. Each part parameter, then, will have a performance range, the result of parts being tested from different cells of the matrix, see Figure 4 - 1.

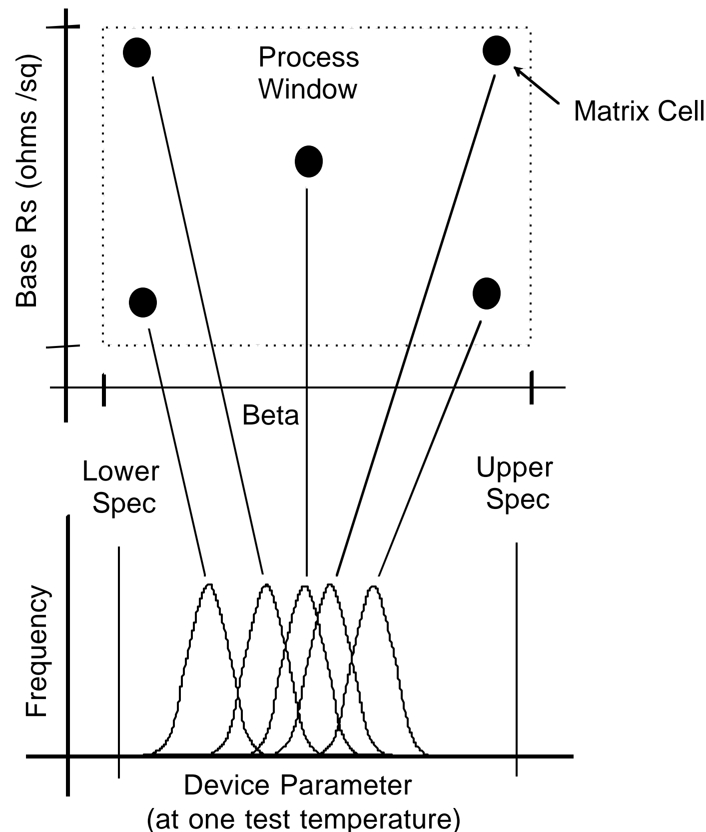

Figure 4 - 1 Typical Matrix Parameter Range

In defining the DI it is assumed that the Device Parameter population that is sampled in each matrix cell is normally distributed and independently distributed. The index also assumes that the product would yield equally well when processed at any point within the Design / Process window. Thus, there is no weighting of the matrix data.

The actual definition of DI is very similar to that of the Cpk index. The important difference is that the Cpk is based on a single normal distribution (grouping all matrix cells into one distribution) while the DI is based on the worst case of several individual matrix distributions, see Figure 4 - 2.

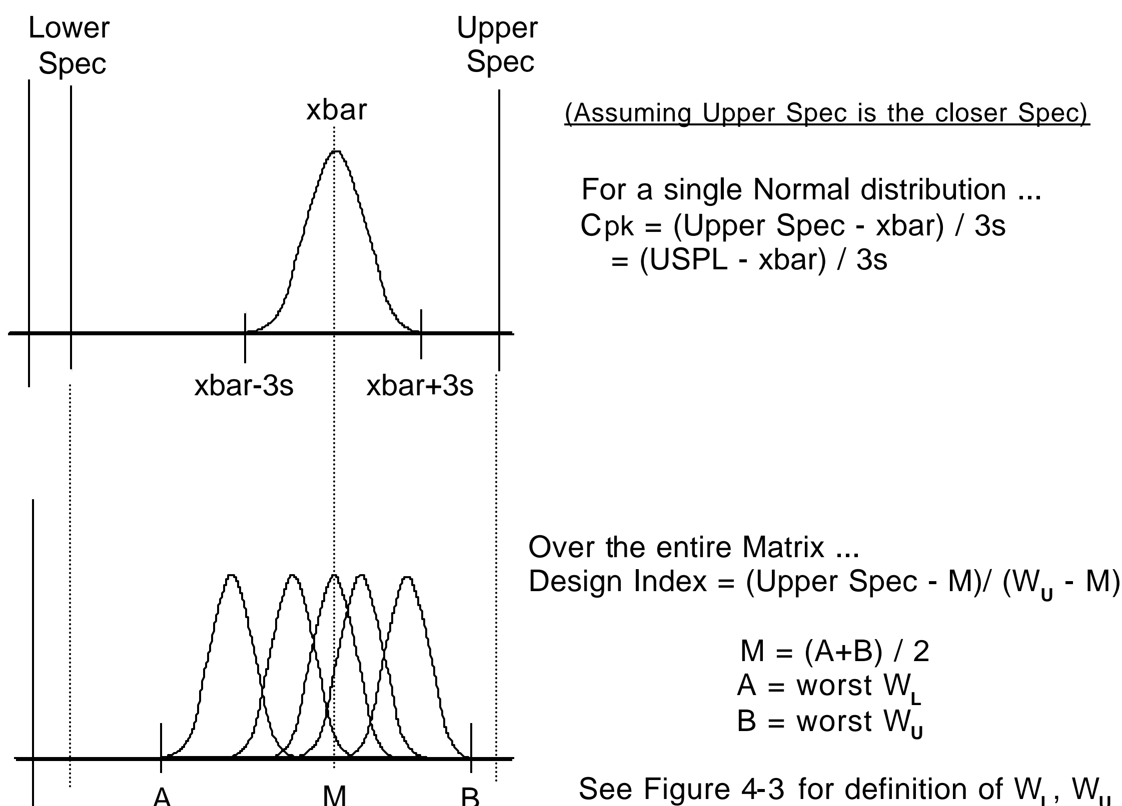

Figure 4 - 2 Comparison of Cpk and Design Index

The DI (one number for each Device Parameter upper and lower specification limit) is determined as follows:

1. Statistically analyze the electrical distribution characteristics for each matrix cell, device parameter, and test temperature. (The statistical analysis should include an estimation of the mean and the worst case edges for each distribution, and should be based on the confidence interval (ci) on the estimated mean, see Figures 4 – 3.) For example, if there are 5 matrix cells (as shown in Figure 4 -1) and three test temperatures, there will be 15 distributions (5 at each temperature) for each Device Parameter, see Figure 4 - 4.
2. Using the Extreme W_L (A) and Extreme W_U (B), as shown in Figure 4-3, calculate the mean [M = (A + B) / 2].
3. Then, determine the DI values (DI lower and DI upper) for each parameter) as shown in Figure 4-4.

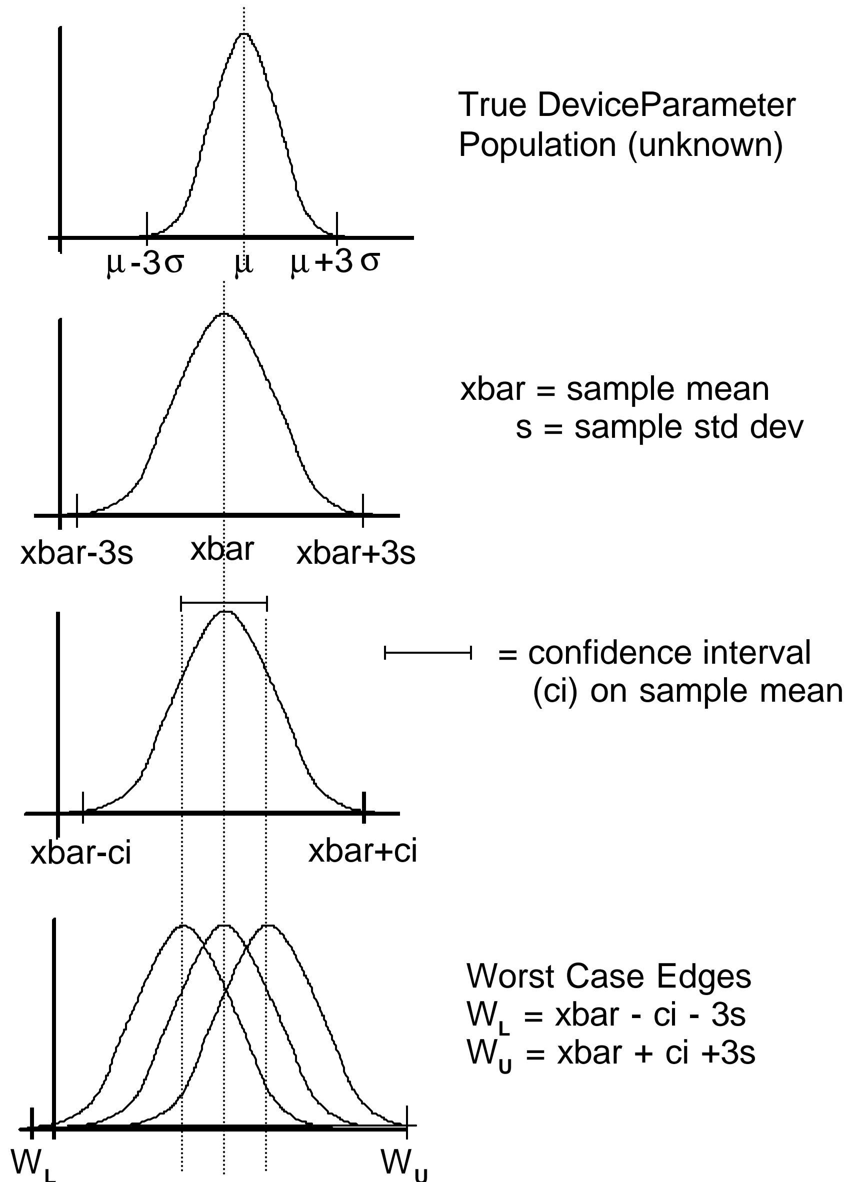

Figure 4 - 3 Statistical Analysis Including The Confidence Interval

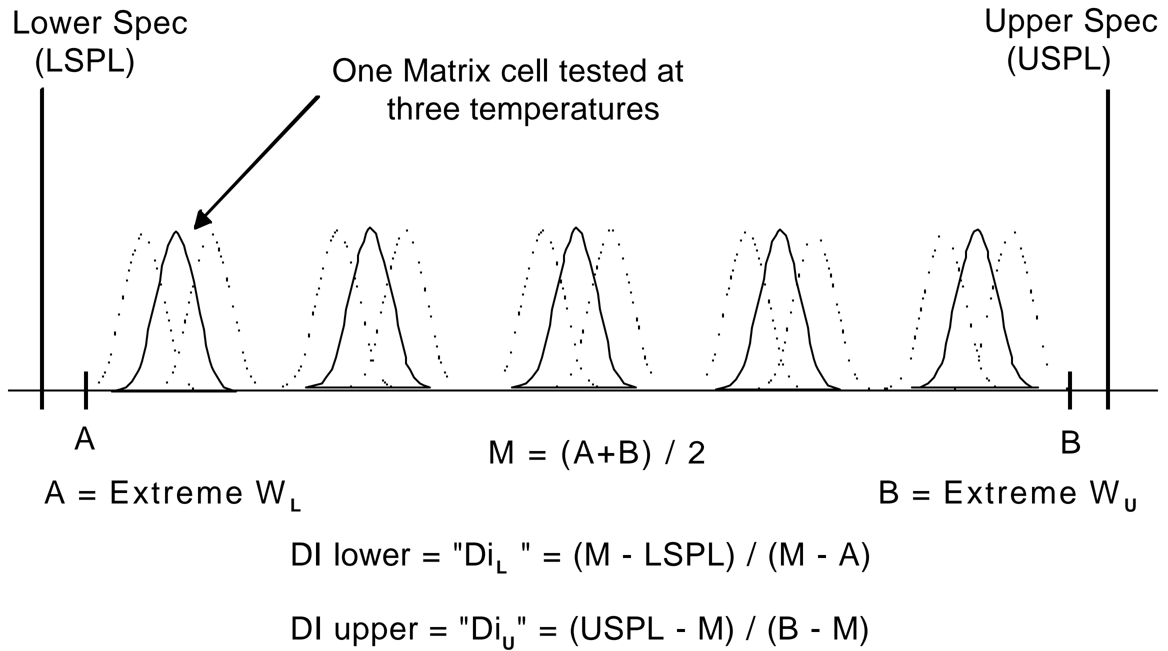

Figure 4- 4 Analysis of Five Matrix Cells at Three Temperatures

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Revision History

Rev #	Date of change	Brief summary listing affected sections
--	July 31, 2001	Initial release