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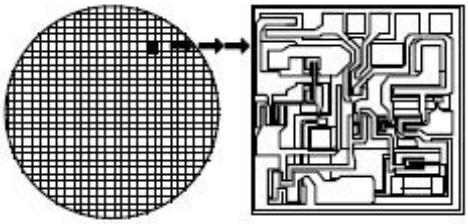
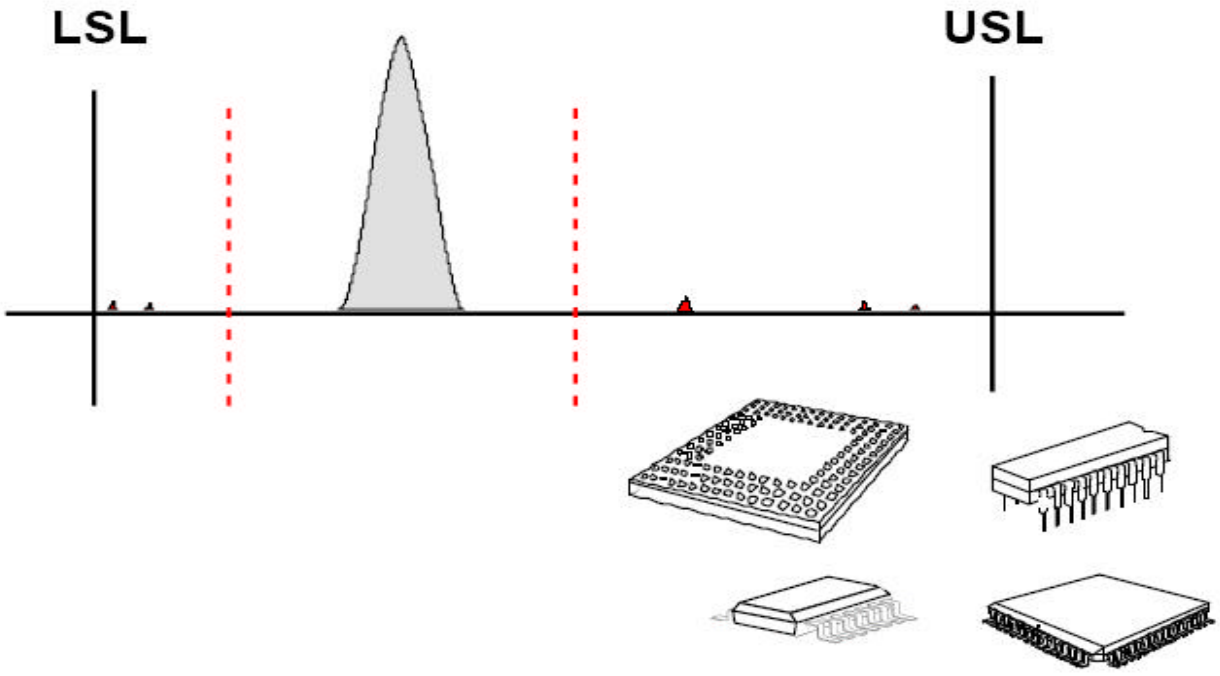
Automotive Electronics Council
Component Technical Committee



GUIDELINES FOR PART AVERAGE TESTING



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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Counsel would especially like to recognize the following significant contributors to the development and release of this document:

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GUIDELINES FOR PART AVERAGE TESTING

Text enhancements and differences made since the last revision of this document are shown as underlined text.

1. SCOPE

This guideline presents a statistically based method, called part average testing (PAT), for removing parts with abnormal characteristics (outliers) from the semiconductors supplied per AEC-Q100 and AEC-Q101. The test limits used in PAT are established based on a sample of the electrical test results for that particular part with its unique design and processing. Each part design and its associated processing will show a unique distribution of test results for each test requirement and this data is the basis for establishing PAT limits. The principles described in this guideline are applicable to packaged or unpackaged die. For a further discussion of PAT and its possible use to provide Known Good Die, see Appendix 1.

1.1 Purpose

This guideline is intended to provide a general method for removing abnormal parts and thus improve the quality and reliability of parts supplied per AEC-Q100 and AEC-Q101. PAT and AEC-Q002 (Statistical Yield Analysis) are not intended to be a requirement. The exact methods applied may vary from what is described in this guideline, specifically if distributions are non-normal. Such derived methods may be employed with good statistical justification. The supplier shall be prepared to justify the statistical approach used.

History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems. Use of this technique will also flag process shifts and provide a source of rapid feedback that should prevent quality accidents.

1.2 References

AEC-Q100 Stress Test Qualification for Integrated Circuits
AEC-Q101 Stress Test Qualification for Discrete Semiconductors
AEC-Q002 Guidelines for Statistical Yield Analysis

2. DEFINITIONS

2.1 Important Characteristics

Device characteristics that could impact product quality and reliability. Characteristics that provide the most significant information about a part's capability of working properly under defined user conditions. For examples of important characteristics, see Appendix 2.

2.2 Known Good Die (KGD)

Unpackaged semiconductor devices that are at least as good as an equivalent packaged part.

2.3 Lower Specification Limit (LSL)

Lower specification limit specified on the device specification.

2.4 Robust Mean and Robust Sigma

Statistics calculated excluding outlying data. Outlying data is generally considered to be data that is more than 6 standard deviations away from the mean of the main distribution.

An example of one generalized method of doing this is as follows:

The usual Mean and Sigma can be poor statistics because they are very sensitive to outliers. The use of the term "Robust" is to indicate statistics that are insensitive to outliers. Robust mean and Sigma analysis exclude outliers by estimating the location and spread of only the main distribution of parts. The definitions below are true for a normal or Gaussian distribution (of the main population).

Robust Mean = Q2 [the median]

Note 1: Q2 (Quartile 2) is the middle data point, if the sample size is an odd number. If the sample size is an even number, Q2 is the average of the two middle data points.

Robust Sigma = (Q3 - Q1) / 1.35

Note 2: The 1.35 number is inexact for sample sizes less than 20. Q1 is the point 1/4 of the way through the ranked data and Q3 is the point 3/4 the way through the ranked data.

2.5 Upper Specification Limit (USL)

Upper specification limit specified on the device specification.

3. PROCEDURE

3.1 Setting The Test Limits

Test limits may be set in either a static or dynamic manner. The static limits are established based on an available amount of test data and used without modification for some period of time. The dynamic test limits are based on the static limits, but are established for each lot (or wafer in a lot) and continuously modified as each lot (or wafer) is tested. New PAT limits (both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made. PAT limits may be considered for all electrical tests where distribution is appropriate for outlier analysis. Appendix 2 provides guidance for tests for 'important characteristics' believed most likely to provide quality and reliability benefit. PAT test limits shall not exceed the device specification limits.

3.1.1 Static PAT limits

Collect test data from at least six part lots that have passed the test limits as defined by the device specification. Determine the robust mean and sigma values per test by randomly selecting the test data from a minimum of 30 parts from each lot (see Figure 1). If test data is wafer level data, select data from at least 5 die located in different areas of each wafer (at least 30 die per lot). Early in production of a part, when data from six lots is not available, data from characterization lots may be used. This data shall be updated as soon as production data is available. Set the test limits as follows:

Static PAT Limits = Robust Mean $\pm$ 6 Robust Sigma

For data which clearly deviates from normal, the supplier shall use other suitable means and be prepared to defend the resulting method to the customer.

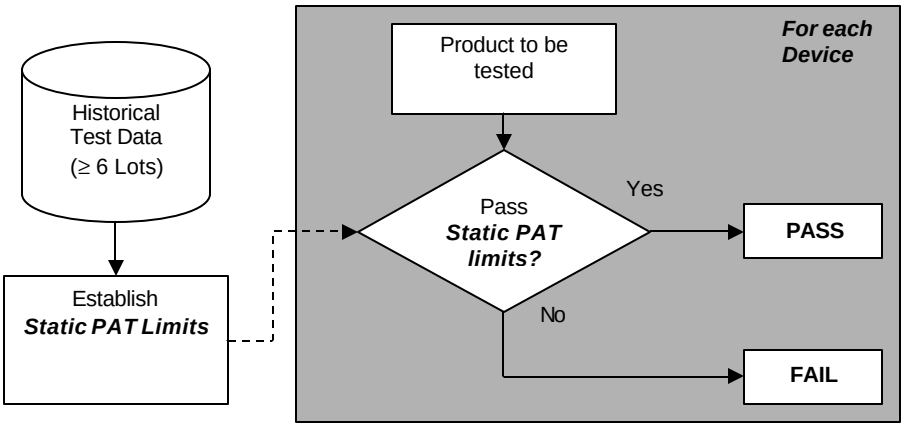

Figure 1: Determining Static PAT Limits

3.1.1.1 The static PAT limits shall be reviewed and updated as required using current data during the first 6 months of production or at least 8 wafer lots, whichever occurs first. Older data shall not be used.

3.1.1.2 After 6 months, the static PAT limits shall be reviewed on a semi-annual basis and updated as needed.

3.1.2 Dynamic PAT limits

Dynamic PAT Limits are preferred over Static PAT Limits because the reference population is the same as the parts being tested. Dynamic PAT can provide tighter limits without causing rejection of good parts because it does not have to consider the lot-to-lot variation that is part of Static PAT Limits. Dynamic PAT limits are determined in the same manner as static PAT limits except that the limits are established using the data from the current lot (or wafer) of parts under test that have passed. To use this method, after the lot (or wafer) of parts have been tested to the static limits they must be held in a manner that allows the application of the newly defined dynamic PAT limits. These limits are defined by further statistical analysis of the test data, which establishes new tighter test limits for that particular lot (or wafer) and removes additional outliers (see Figure 2). Set the test limits as follows:

Dynamic PAT Limits = Robust Mean ± 6 Robust Sigma (see Appendix 1)

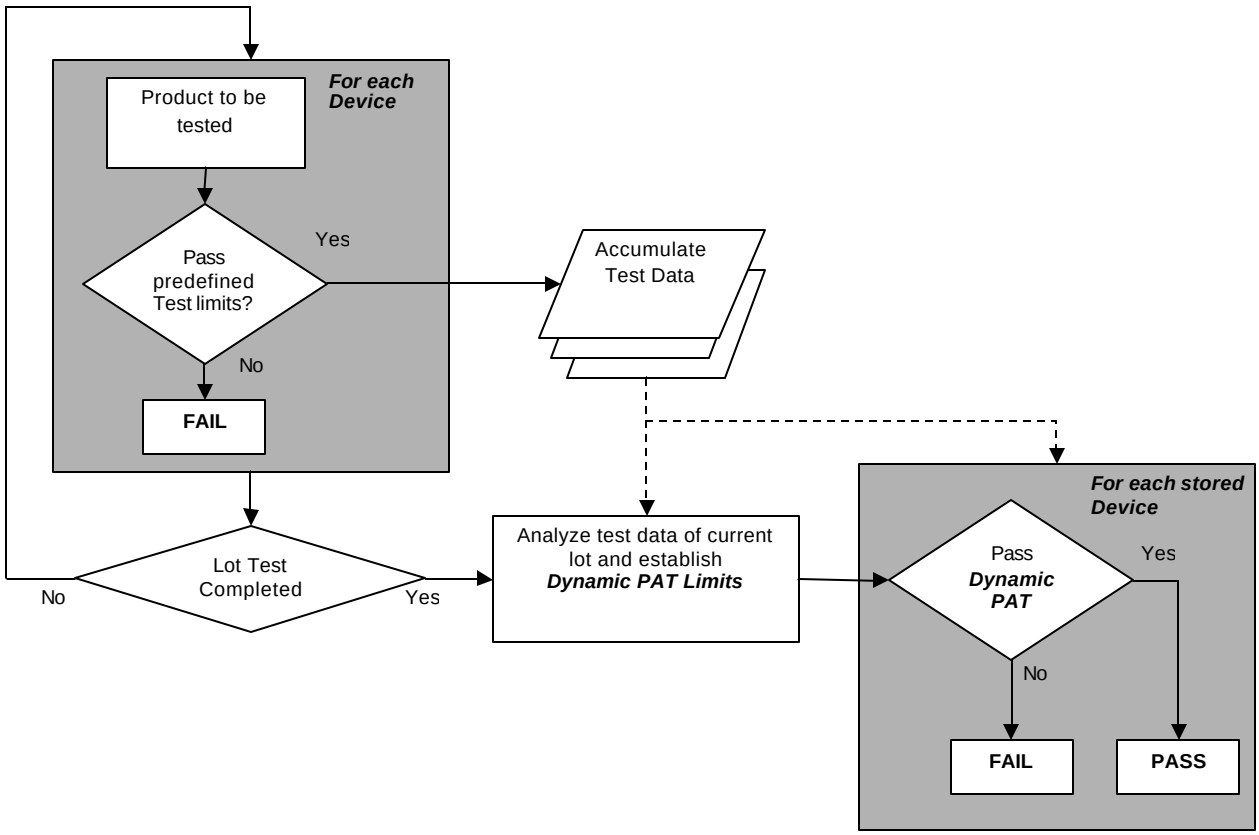

Figure 2: Determining Dynamic PAT Limits (Probe or Serialized)

This illustrated PAT is readily applicable to wafer probe or to final test for devices that maintain traceability. For devices that cannot maintain traceability at the final stage, the application of dynamic PAT would require retests of the thus far passing units.

3.1.2.1 Other Types of Dynamic PAT limits

One variation of performing dynamic PAT and to avoid retesting of packaged product is illustrated in Figure 3. The dynamic limits would be applied to the population in the same lot, but not to the units that produced the data used to establish the dynamic PAT limits.

Initially, static PAT limits may be used to test a pre-defined population of N units (N = 500 or 1000, for instance). Using the data generated, lot specific PAT limits will be established. These generated static limits will become the new test limits (the counter will be reset to zero) to test the following samples in the group. Once the counter reaches N again, the analysis process will be repeated until all samples in the lot are tested.

Another variation of performing dynamic PAT is to take a random sample of the first N components and circulate the limits for the lot based on this sample.

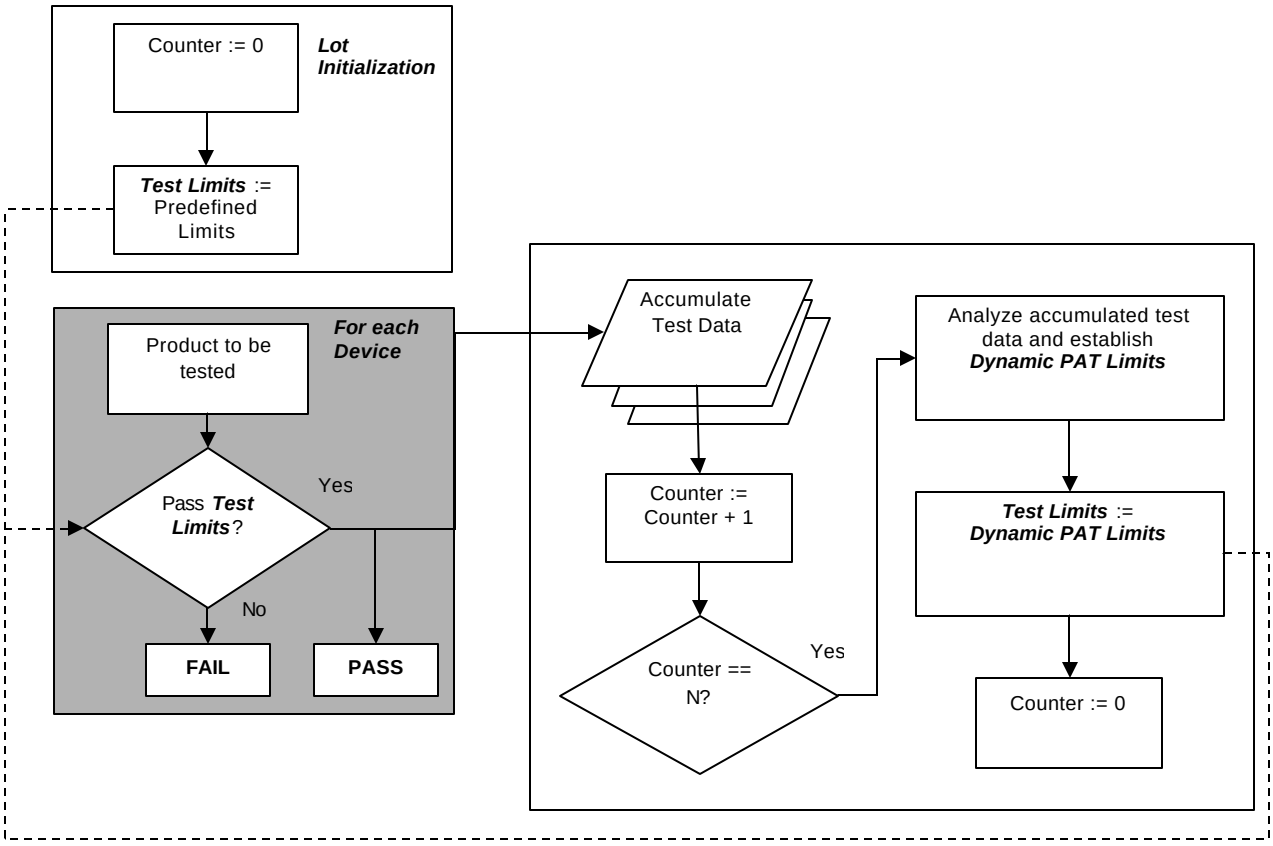

Figure 3: Dynamic PAT Application for Packaged Product Tests

APPENDIX 1: PART AVERAGE TEST LIMITS

A1. Part Average Test (PAT) Limits represent the application of statistical techniques for the removal of abnormal parts during part level testing (see Figure 3). A device specification defines the requirements needed for the part to work properly in the application. Every part (part as used here refers to a supplier part number) is built with a particular design and SPC controlled process that, if processed correctly, will yield a certain consistent set of characteristic test results. PAT uses statistical techniques to establish the limits on these test results. These test limits are set up to remove outliers (parts whose parameters are statistically different from the typical part) and should have minimal yield impact on correctly processed parts from an SPC controlled process. This test methodology is not limited to the standard device specification tests, but may also include extended operating tests (tests beyond the device specification requirements) to improve the ability to detect special abnormal conditions and increase the sensitivity of this testing technique. The only restriction on extended operating tests is that the test shall not reduce the reliability of the parts that pass the test.

A1.1 The intent of PAT is to increase the quality and reliability of AEC-Q100 and AEC-Q101 parts by removing abnormal parts as early in the part manufacturing sequence as possible (preferably at wafer test). This should minimize costs related to customer support and failure analysis, and provide early feedback to prevent the occurrence of quality accidents.

A1.2 This method, if utilized to its full capability (with statistical limits for all part level electrical tests and proper extended operating condition tests), is capable of providing “electrically” Known Good Die for most semiconductor technologies. It should also be remembered that Known Good Die (as defined in section 2) requires more than part level electrical testing. It requires careful control of all other assembly processes such as wafer sawing, die handling, packaging, ESD, etc.

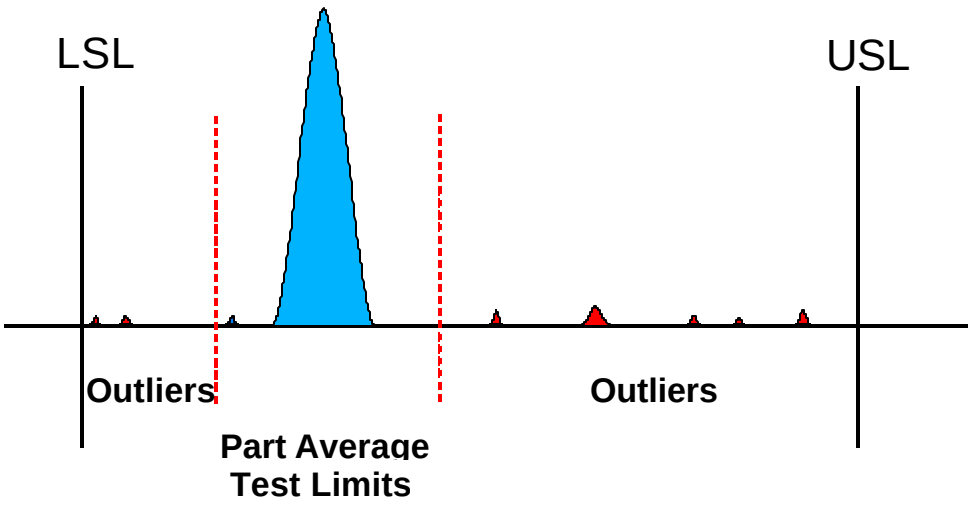

Figure 4: Graphical Representation of Part Average Test Limits and Outliers

APPENDIX 2: ELECTRICAL TESTS

This is not a comprehensive list, and is offered only as a suggested list to be considered. Other tests deemed more important or more relevant to a particular device should also be included in Part Average Testing.

A2.1 Tests Required For All Devices Types

To meet the requirements of this procedure, the following tests shall use PAT limits during ATE testing.

A2.1.1 Pin Leakage Test

This is an example of where PAT can be used. This test will verify that the device pins have normal junction characteristics with respect to substrate and with respect to V_{DD} in the case of CMOS components.

A2.1.2 Standby Power Supply Current (I_{DD} or I_{CC})

A2.1.3 IDDQ testing

This test is applicable for those devices that are capable of being IDDQ tested

A2.1.4 Output breakdown voltage (BV_{CES} or BV_{DSS}), Output leakage (I_{CES} or I_{DDS} - measured at 80% of the breakdown voltage value), Output current drive (I_{OUT}) and Output voltage levels (V_{OUT})

These tests are applicable to Linear and BiCMOS devices.

A2.1.5 Over-Voltage Stress Test

This test forces failures in silicon MOS type devices (e.g., NMOS, PMOS, CMOS, and DMOS, etc.) that have gate oxide and other related defects. The PAT limits may be applied to measured characteristics such as active current or to other items. Also, statistical bin limits may be applied here.

A2.1.6 Low Level Input Current (I_{IL}), High Level Input Current (I_{IH}), Low Level Output Voltage (V_{OL}), High Level Output Voltage (V_{OH})

This test indicates the functionality of the transistors in the design. Enforcing PAT limits on these tests can catch weak transistors.

A2.1.7 Propagation Delay or Output Response Time, Rise/Fall Times

This test indicates the functionality of the transistors in the design. Enforcing PAT limits on these tests can catch weak transistors.

A2.1.8 Extended Operating Tests

Extended operating tests are tests beyond the device specification requirements intended to increase the effectiveness of PAT. These are the type of tests that, combined with PAT testing of more device characteristics, can make part level testing capable of providing parts with very high quality and reliability (Known Good Die). PAT limits may be established for various measured characteristics after each extended operating test is applied. The following are some examples of extended operating tests:

- Low/High temperature
- Low/High voltage operation
- Dwell time at high voltage
- Operating frequencies above/below specification requirements
- For power devices, demonstration of safe operating capability (60% of safe operating limit) followed by leakage testing, etc.

Note 3: The only restriction on these tests is that it must be demonstrated that the test does not adversely affect the reliability of the part. The reliability of the part can be demonstrated by passing the electrical qualification tests as specified in AEC-Q100 (for ICs) and AEC-Q101 (for discrete semiconductors).

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	July 31, 1997	Initial Release.
A	Oct. 8, 1997	Paragraph 2.1 revised, Figure 2 changed, Appendix 2 added new paragraph 2.1, added Appendix 3.
B	Aug. 25, 2000	Revised 1.2.2, 3.1, 3.1.2, Appendix 1, and Appendix 3.
C	July 18, 2003	Corrected formatting errors. Removed Appendix 3 and references to DE Histograms.
D	Dec. 9, 2011	Complete Revision. Revised Acknowledgement and Sections 1.1, 1.2, 2.1, 2.4, 3.1, 3.1.1, 3.1.1.1, 3.1.1.2, 3.1.2, A1.1, Appendix 2, A2.1.1, and A2.3.8. Added Notice Statement, Sections 3.1.2.1 and A2.1.3 to A2.1.7, and new Figures 1, 2, and 3. Deleted signature block and Sections 1.2.2 and A2.2 to A2.3.7.