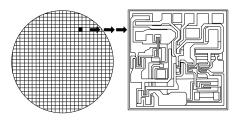
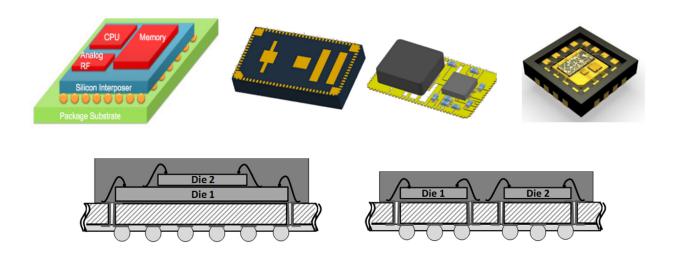
AEC - Q104 - Rev-September 14, 2017



FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR MULTICHIP MODULES (MCM) IN AUTOMOTIVE APPLICATIONS



Automotive Electronics Council Component Technical Committee

Component Technical Committee

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FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR MULTI-CHIP MODULES (MCM)

1. SCOPE

This document contains a set of failure mechanism based stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of multichip modules (MCM). A single MCM consists of multiple electronic components enclosed in a single package (refer to Section 1.3.5) that perform an electronic function.

This document applies only to MCMs which are designed to be soldered directly to a printed circuit board assembly.

MCM types not included in the scope of this document include the following:

- Two assembly components or MCMs that a Tier 1 / original equipment manufacturers (OEM) assembles onto a system.
- Light Emitting Diodes (LEDs), which are covered by AEC-Q102.
- MEMs, which are covered by AEC-Q103 Qualification document.
- Power MCMs may require specific considerations and qualification test procedures that are outside the scope of this document. A power MCM consists of multiple active power devices (i.e., IGBTs, power MOSFETs, diodes) and, if necessary, additional passive devices (e.g., temperature sensors, capacitors), which are integrated on a substrate.
- Solid State Drives (SSD).
- MCMs with exterior connectors that are not soldered to a board or other assembly.

For MCM with embedded firmware, the firmware is considered an integral part of the MCM. As such, it is qualified as part of the overall system methodology, which is dependent on the type of MCM. Standalone qualification of the firmware itself is not in the scope of this document.

1.1 Purpose

The purpose of this specification is to determine that a MCM is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Automotive

AEC-Q100 AEC-Q100-001 AEC-Q100-004	Failure Mechanism Based Stress Test Qualification for Integrated Circuits Wire Bond Shear Test IC Latch-up Test
AEC-Q100-005	Non-Volatile Memory Program/Erase Endurance, Data Retention and
	Operational Life Test
AEC-Q100-007	Fault Simulation and Fault Grading
AEC-Q100-009	Electrical Distribution Assessment
AEC-Q100-010	Solder Ball Shear Test
AEC-Q101	Failure Mechanism Based Stress Test Qualification for Discrete
	Semiconductors

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	AEC-Q200 AEC-Q001 AEC-Q002 AEC-Q003 AEC-Q005	Guideli Guideli Guideli	Test Qualification for Passive Components les for Part Average Testing les for Statistical Yield Analysis les for Characterizing the Electrical Performance Requirements								
1.2.2	Military										
	MIL-STD-883 MIL-STD-1580B	Destruc	ethods and Procedures for Microelectronics ctive Physical Analysis for Electronic. Electromagnetic and mechanical Parts								
1.2.3	Industrial										
	ANSI/ESDA/JEDEC JS	-001	ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) Component Level								
	ANSI/ESDA/JEDEC JS	-002	ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing -Charged Device Model (CDM) - Device Level								
	JEDEC JEP001		Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites)								
	JEDEC JESD22 JEDEC JESD78 JEDEC JESD89		Reliability Test Methods for Packaged Devices Latch-up Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices								
	JEDEC JESD89-1 JEDEC JESD89-2 JEDEC JESD89-3 IPC/JEDEC J-STD-002		System Soft Error Rate (SSER) Test Method Test Method for Alpha Source Accelerated Soft Error Rate Test Method for Beam Accelerated Soft Error Rate Solderability Test for Component Leads, Terminations, Lugs,								
	IPC/JEDEC J-STD-020		Terminals and Wires Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices								
	IPC/JEDEC J-STD-046		Customer Notification Standard for Product/Process Changes by Electronic Product Suppliers								
	IPC/JEDEC-9702 IPC-9701		Monotonic Bend Characterization of Board-Level Interconnects Performance Test Methods and Qualification Requirements for								
	ISO 16750-4		Surface Mount Solder Attachments Road Vehicles – Environmental Conditions and Testing for Electrical and Electronic Equipment – Part 4: Climatic Loads								

1.3 Definitions

1.3.1 AEC Q104 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the MCM is "AEC-Q104 qualified". For ESD, it is **highly recommended** that the passing voltage be specified in the supplier datasheet with a footnote on any pin exceptions. This will allow suppliers to state, e.g., "AEC-Q104 qualified to ESD Classification 2".

This document focuses only on qualification of the completed MCM component. It does not address the qualification of each subcomponent used to create the MCM. However, MCM manufacturers are encouraged to leverage AEC qualified sub-components, when available, to promote best MCM quality.

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1.3.2 AEC Certification

Note that there are no "certifications" for AEC-Q104 qualification and there is no certification board run by AEC to qualify MCM. Each supplier performs their qualification to AEC standards, considers customer requirements, and submits the data to the customer to verify compliance to AEC-Q104.

1.3.3 Approval for Use in an Application

"Approval" is defined as customer approval for use of a MCM in their application. The customer's method of approval is beyond the scope of this document.

1.3.4 Assembly Lot

An assembly lot as used in this document is a batch of MCMs that are grouped together through the same process steps (i.e., through the same machines with same material set through completion of the MCM). The assembly lot includes all process and test steps. The same material set includes a traceable combination of multiple sub-component lots. A representative flow is shown below in Figure 1.

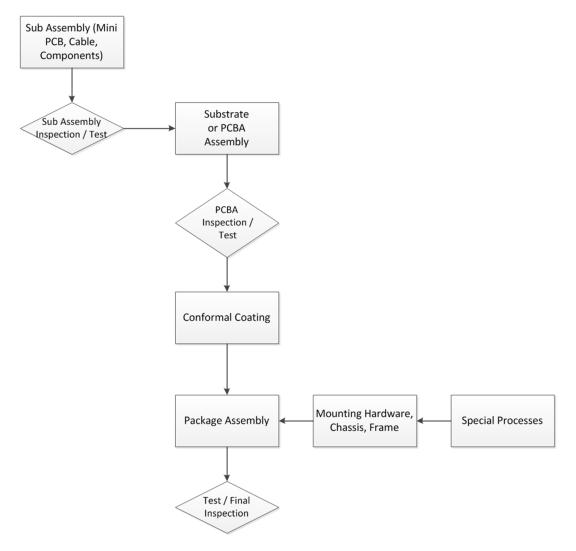


Figure 1: General MCM Manufacturing Process Flow

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1.3.5 Multichip Module (MCM)

Multiple active and/or passive sub-components interconnected to create a single complex circuit within a single MCM package that is intended for reflow solder attachment to a printed circuit board. Sub-components may be molded and/or unmolded (die) combined into a single hermetic or non-hermetic package. Bare die (unmounted) is outside the scope of this document.

Note: Multi-chip and Multichip are both accepted in the industry literature.

1.3.6 MCM Operating Temperature Range

Typical ambient operating temperature ranges for sub-components are defined in AEC-Q100, AEC-Q101, and AEC-Q200. Supplier shall document the specific operating temperature range for the MCM in their datasheet and qualification report.

1.3.7 Process Capability Index Measurement (Cpk)

Refer to AEC-Q003 Characterization to understand how the Cpk measures will be used in this standard.

1.3.8 Subcomponent

A subcomponent is any element – integrated circuit, discrete, passive, printed circuit board or interconnect – included in the MCM construction.

1.3.9 System in a Package (SiP)

A System in Package (SiP) is an assembly of electronic components and associated interconnection in a package configuration that is also intended to be used as a single die package assembly. Therefore, it can be qualified within the scope of AEC-Q100 per Section 2.1. An example of a SiP is multiple die in a BGA package, where the die are assembled in a stacked or side-by-side configuration.

2. GENERAL REQUIREMENTS

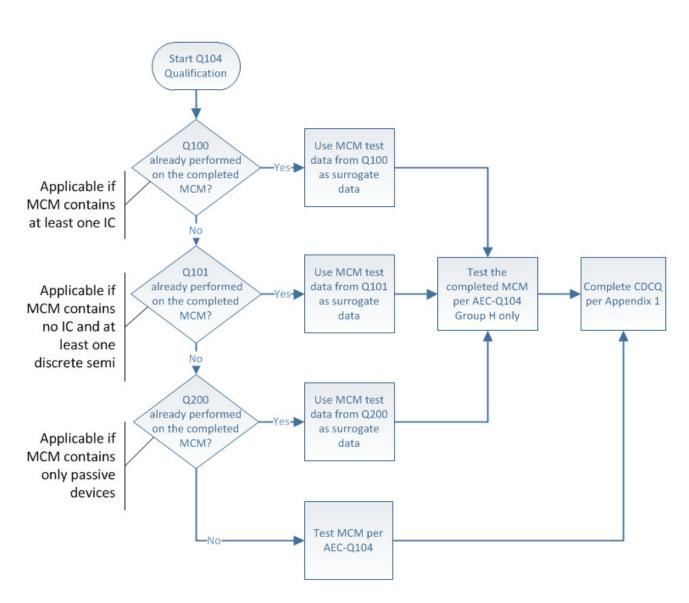
2.1 AEC-Q104 Applicability

The ratings of each subcomponent used in the MCM construction should meet or exceed the MCM ratings, including the operating temperatures used by the end user application. The selected subcomponent should be capable to withstand the temperature, voltage, current, etc. of the MCM, and operate after final testing without degradation.

Use this document for MCMs that cannot be qualified completely using one of the following:

- AEC-Q100 Failure Mechanism Based Stress Test Qualification for Integrated Circuits
- AEC-Q101 Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors
- AEC-Q200 Stress Test Qualification for Passive Components

When feasible, the reliability test methods for MCM can leverage the existing guidelines established in AEC-Q100, AEC-Q101, or AEC-Q200. However, additional testing per AEC-Q104 Group H must be considered, see Figure 2 below. Feasibility is based mainly on MCM complexity, technology, and/or package type, but consideration with respect to cost can be applicable with customer agreement. This document focuses only on qualification of the completed MCM component. It does not address the qualification of each sub-component used to create the MCM. However, MCM manufacturers are encouraged to leverage AEC qualified sub-components, when available, to promote best MCM quality.



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Figure 2: Qualification test method options for the MCM

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2.2 AEC-Q104 Objective

These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to stimulate / precipitate failures in an accelerated manner compared to application conditions. This set of tests should not be used indiscriminately. Each qualification project should be examined for:

- a. Any potential new and unique failure mechanisms as determined through a Failure Mode Effects Analysis (FMEA).
- b. Any situation where these tests/conditions may induce failures that would not be seen in the application.
- c. Any extreme use condition and/or application that could adversely reduce the acceleration and, therefore, lifetime coverage of the stress test.

Use of this document does not relieve the supplier of their responsibility to meet their own company's internal qualification program.

In this document, "user" is defined as all customers using a MCM qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document.

Supplier should document ambient operating temperature range for the MCM per Section 1.3.6.

2.3 Precedence of Requirements

In the event of conflict in the requirements of this standard and those of any other documents, the following order of precedence applies:

- a. The purchase order (or master purchase agreement terms and conditions)
- b. The (mutually agreed) individual device specification
- c. This document
- d. The reference documents in Section 1.2 of this document
- e. The supplier's data sheet

For the MCM to be considered a qualified part per this specification, the purchase order and/or the individual MCM specification cannot waive or detract from the requirements of this document.

2.4 Use of Generic Data to Satisfy Qualification and Requalification Requirements

2.4.1 Definition of Generic Data

For simple MCMs (i.e., an encapsulated plastic MCM) that can be qualified by AEC-Q100, AEC-Q101, or AEC-Q200, use those documents for the definition of generic data.

The use of generic data to simplify the qualification process is strongly encouraged. Generic data can be submitted to the user as soon as it becomes available to determine the need for any additional testing. To be considered, the generic data must be based on a matrix of specific requirements associated with each characteristic of the MCM and manufacturing process. If the generic data contains any failures, the data is not usable as generic data unless the supplier has documented and implemented corrective action or containment for the failure condition that is acceptable to the user.

It is the supplier's responsibility to present rationale for why any of the recommended tests need not be performed.

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The data on silicon with known fab process identification (i.e., internal fab site) is valid. For third party silicon where the fab process is not known, the supplier must rely on the subcomponent manufacturer to provide "fab" data. There are no hard and fast rules but a set of general guidelines can be generated. Recommended guidelines for grouping of similar MCMs for the purpose of generic reliability data are as follows:

MCMs may leverage generic reliability data from:

- MCMs with the same substrate base material (laminate) type, trace metal & trace plating. A significant change to the substrate, such as a change to the schematic, is considered a fundamental change to the MCM and requires extensive re-evaluation.
- MCMs with same or greater number of printed circuit board layers.
- MCMs with same or smaller feature size of substrate or printed circuit board.
- MCMs with the same outer configuration package/lid/housing.
- MCMs with the same series or types of subcomponents including integrated circuits, discrete and passive elements.
- MCMs with silicon from known same fab processes.
- MCMs with the same assembly process materials such as solder, adhesives, epoxies, under-fill and encapsulant.
- MCMs assembled at the same assembly subcontractor qualified for the given technology to be qualified.

2.4.2 Acceptance of Generic Data

Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a MCM in the same qualification family. Potential sources of data could include any customer specific data (withhold customer name), process change qualification, and periodic reliability monitor data (see Figure 3).

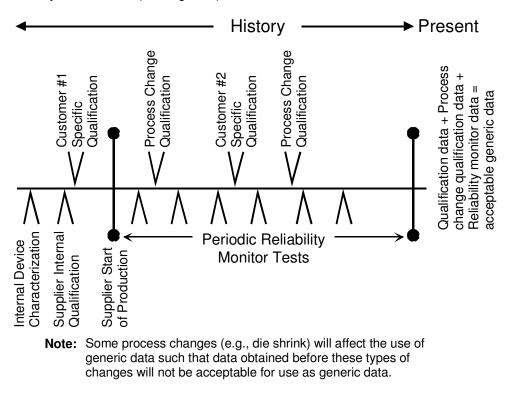


Figure 3: Generic Data Acceptance Considerations

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2.5 Test Samples

2.5.1 Lot Requirements

Test samples shall consist of a representative MCM from the qualification family. Where multiple lot testing is required due to a lack of generic data, test samples as indicated in Table 1 should be composed of approximately equal numbers from non-consecutive sub-component lots, assembled in non-consecutive molding lots. That is, they should be separated in the fab or assembly process line by at least one non-qualification lot. Any deviation from the above requires technical explanation from the supplier. It is recommended that lots are separated by at least one calendar week.

2.5.2 **Production Requirements**

All qualification MCMs shall be produced on tooling and processes at the manufacturing site that will be used to support MCM deliveries at production volumes. Other electrical test sites may be used for electrical measurements after having met the same qualification requirements.

2.5.3 Reusability of Test Samples

MCMs that have been used for nondestructive qualification tests may be used to populate other qualification tests. MCMs that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.5.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 1.

If the supplier elects to use generic data for qualification, the specific test conditions and results must be recorded and available to the user. Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.3 for each test requirement in Table 1. MCM specific qualification testing should be performed if the generic data does not satisfy these requirements.

2.5.5 Pre- and Post-stress Test Requirements

End-point test temperatures (e.g., room, hot and/or cold) are specified in the "Additional Requirements" column of Table 1 for each test.

2.6 Definition of Test Failure after Stressing

Test failures are defined as those MCMs not meeting the individual MCM specification, criteria specific to the test, or the supplier's data sheet, in the order of significance as defined in Section 2.3. Any MCM that shows external physical damage affecting form, fit and function of the final product shipped or attributable to the environmental test is also considered a failure. If the cause of failure is due to mishandling during stressing or testing such as EOS or ESD, or some other cause unrelated to the component reliability, the failure shall be discounted, but reported as part of the data submission.

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3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New MCM

The stress test requirements for qualification of a new MCM is shown in Figure 4 with the corresponding test conditions defined in Table 1. For each qualification, the supplier must have data available for all of these tests, whether it is stress test results on the MCM to be qualified or acceptable generic data. A review shall also be made of other MCMs in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the customer.

For each MCM qualification, the supplier must have available the following:

- Certificate of Design, Construction and Qualification (see Appendix 1). The AEC-Q104 CDC Template is available from the AEC website at http://www.aecouncil.com.
- Stress Test Qualification data (see Table 1)
- Data indicating the level of fault grading of the software / firmware used for qualification (when applicable to the MCM type) per AEC-Q100-007 that will be made available to the customer upon request.

An AEC-Q104 Qualification Test Plan template, to aid in qualification planning, is available from the AEC website at http://www.aecouncil.com.

3.2 Requalification of a Changed MCM

Requalification of a MCM is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the MCM (see Table 2 for guidelines).

There are a variety of different changes to a MCM:

- The least impact would be a qualified subcomponent change with no change in the critical characteristics of the subcomponent. For a simple non-risk change, a simple confirmation of the operating characteristics of the MCM is sufficient.
- If critical characteristics change (e.g., the device creates more heat, its resistance changes, etc.), then a more thorough evaluation is necessary.
- If it is a significant change to the substrate, such as a change to the schematic, it is a fundamental change to the MCM and requires extensive re-evaluation.
- If the change to the substrate is a minor change in manufacturing, less evaluation is possible.

3.2.1 Process Change Notification

The supplier will meet IPC/JEDEC J-STD-046 or agreed user requirements for product/process changes.

3.2.2 Changes Requiring Requalification

As a minimum, any change that is within customer change requirements or any major change to the MCM affecting form, fit and function requires performing the applicable tests listed in Table 1, using Table 2 to determine the requalification test plan. Table 2 should be used as a guide for determining which tests are applicable to the qualification of a particular change or whether equivalent generic data can be submitted for that test(s).

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3.2.3 Criteria for Passing Requalification

All requalification failures shall be analyzed for root cause. Only when corrective and preventative actions are in place, the MCM may then be considered AEC-Q104 qualified again.

3.2.4 User Approval

A change may not affect a MCM's operating temperature range, but may affect its performance in an application. Individual user authorization of a process change will be required for that user's particular application(s), and this method of authorization is outside the scope of this document.

3.2.5 Qualification of a MCM Requiring Pb-Free Board Attach

Added requirements needed to address the special quality and reliability issues that arise when Lead (Pb)-Free processing is utilized is specified in AEC-Q005 Pb-Free Requirements. Materials used in Pb-Free processing include the termination plating and the board attach (solder). These new materials usually require higher board attach temperatures to yield acceptable solder joint quality and reliability. These higher temperatures may adversely affect the moisture sensitivity level of plastic packaged semiconductors. As a result, new, more robust mold compounds may be required. If an encapsulation material change is required to provide adequate robustness for Pb-Free processing of the MCM, the supplier should refer to the process change qualification requirements in this specification. Preconditioning should be performed at the Pb-Free reflow classification temperatures described in IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices before environmental stress tests.

4. QUALIFICATION TESTS

4.1 General Tests

Test flows are shown in Figure 4 and test details are given in Table 1. Not all tests apply to all MCMs. For example, certain tests apply only to ceramic packaged MCMs, others apply only to MCMs with NVM, and so on. The applicable tests for the particular MCM type are indicated in the "Note" column of Table 1. The "Additional Requirements" column of Table 1 also serves to highlight test requirements that supersede those described in the referenced test method. Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

4.2 MCM Specific Tests

The following tests must be performed on the specific MCM. Generic data is not allowed for these tests.

- 1. Electrostatic Discharge (ESD) All product MCMs.
- Latch-up (LU) All MCMs that include active sub-components. See JESD78 appendix for details.
- 3. Electrical Distribution The supplier must demonstrate, over the operating temperature range, voltage, and frequency, that the MCM is capable of meeting the parametric limits of the MCM specification. This data must be taken from at least three lots, or one matrixed (or skewed) process lot, and must represent enough samples to be statistically valid, see AEC-Q100-009. It is strongly recommended that the final test limits be established using AEC-Q001 Guidelines for Part Average Testing.

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4.3 Wearout Reliability Tests

Testing for the failure mechanisms listed below must be available to the user whenever a new technology or material relevant to the appropriate wearout failure mechanism is to be qualified. The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new MCM, but should be available to the user upon request.

- Electromigration
- Time-Dependent Dielectric Breakdown (or Gate Oxide Integrity Test) for all MOS technologies
- Hot Carrier Injection for all MOS technologies below 1 micron
- Negative Bias Temperature Instability
- Stress Migration

ENVIRONMENTAL MECHANICAL ESD / EMC/ LU High Temp Mechanical Low Temp High Temp Power High Temp мсм Mechanical Constant Temp High Pb Free ESD Shock Cavity Storage Storage Temp Operating Drop Test Shock Acceleration Cycle Humidity (LF) (HBM/CDM) (LTSL) Drop Test (HTSL) Cycle Life (MCM DROP) (MS) (CA) (TC) (UHAST (DROP) (PTC) (HTOL) or AC or TH) Variable Physical Frequency Electromagnetic Dimensions Vibration Compatability (PD) (VFV) (EMC) High Temp Early Life Board Level Humidity Thermal Startup Reliability Failure Wire Bond Solder Ball Cycling Shock Test Rate Die Shear (STEP) Pull and Solderability X- Ray (HAST or (TS) Shear (BLR) (ELFR) Latch- Up (DS) Shear (SD) (XRAY) SBS) THB) (WBP/WBS) (LU) Internal Visual Gross / Fine Acoustic Lead Temperature Water Lid Torque Inspection for Leak Integrity Microscopy Steps Vapor (LT) Migration (GFL) (LI) (AM) (STEP) (IWV) (VISM)

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Note: Pre-conditioning (PC) to simulate customer manufacturing and rework processes is required for the package accelerated environmental stress tests (test group A). See Tables 1 & 2 for applicability of each test.

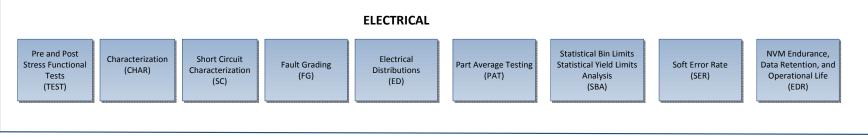


Figure 4: Qualification Test Flow

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Table 1: Qualification Test Methods

	TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS													
STRESS	ABV # LEVEL TO TEST NOTES SAMPLE SIZE NUMBER OF LOTS			ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS								
Preconditioning	PC	A1	Apply to MCM	P, B, S, N, G	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	3	0 Fails	IPC/JEDEC J-STD-020 JEDEC JESD22-A113	Performed on surface mount MCMs only. PC performed before THB/HAST, AC/UHST, TC, and PTC stresses. It is recommended that J-STD-020 be performed to determine what preconditioning level to perform in the actual PC stress per JESD22-A113. The minimum acceptable level for qualification is level 3 per JESD22-A113. Where applicable, preconditioning level and peak reflow temperature must be reported when preconditioning and / or MSL is performed. Delamination from the die surface in JESD22-A113/J-STD-020 is acceptable if the MCM passes the subsequent qualification tests. Any replacement of MCM must be reported. TEST before and after PC at room temperature.					
Temperature- Humidity-Bias or Biased HAST	THB or HAST	A2	Apply to MCM	P, D, G	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	3	0 Fails	JEDEC JESD22-A101 or A110	For surface mount MCMs, PC before THB (85°C/85%RH for 1000 hours) or HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). TEST before and after THB or HAST at room and hot temperature.					
Autoclave or Unbiased HAST or Temperature- Humidity (without Bias)	AC or UHST or TH	A3	Apply to MCM	P, B, D, G	Per AEC- Q100/101/Q200 minimum 30/lot or negotiated with Customer	3	0 Fails	JEDEC JESD22-A102, A118, or A101	For surface mount MCMs, PC before AC (121°C/15psig for 96 hours) or unbiased HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). For MCMs sensitive to high temperatures and pressure (e.g., BGA and complex MCMs), PC followed by TH (85°C/85%RH) for 1000 hours may be substituted. TEST before and after AC, UHAST or TH at room temperature.					

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			TEST (- ACCELERA	TED ENVIROI	NMENT STRE	SS TESTS (CON	TINUED)
STRESS	STRESS ABV # LEVEL TO TEST NOTES SAMPLE SIZE / LOT NUMBER OF LOTS		ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS				
Temperature Cycling	тс	Α4	Apply to MCM	D, G	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	3	0 Fails	JEDEC JESD22-A104	 For surface mount MCMs, PC before TC. 1000 cycles across ambient operating temperature range. TEST before and after TC at hot temperature. For encapsulated packages, include pre- and post-Acoustic Microscopy (see AM). Note: At the MCM level, "fast TC" that is quick transition between hot maximum to cold minimum cycling can be referred to as a "Thermal Shock" (similar to MIL-STD-883, test method 1010). After completion of TC, decap five MCMs from one lot and perform WBP and WPS tests on corner bonds (2 bonds per corner) and one mid-bond per side on each device. See AEC-Q100 Appendix 3 for preferred decap procedure to minimize damage and false data.
Power Temperature Cycling	РТС	A5	Apply to MCM	D, G	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	1	0 Fails	JEDEC JESD22-A105	PC before PTC for surface mount MCMs. Test required only on MCM with maximum rated power \geq 1 watt or $\Box T_J \geq 40^{\circ}$ C or MCM designed to drive inductive loads. Thermal shut-down shall not occur during this test. TEST before and after PTC at room and hot temperature.
High Temperature Storage Life	HTSL	A6	Apply to MCM	D, G, K	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	1	0 Fails	JEDEC JESD22-A103	1000 hours at max ambient operating temperature. TEST before and after HTSL at room and hot temperature.

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	TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS											
STRESS	STRESS ABV # LEVEL TO TEST NOTES SAMPLE SIZE NUMBER OF LOTS					ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS				
High Temperature Operating Life	HTOL	B1	Apply to MCM	D, G, K	Per AEC- Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	3	0 Fails	JEDEC JESD22-A108	1000 hours at maximum ambient operating temperature. Voltage at Vcc maximum. TEST before and after HTOL at room, cold, and hot temperature, in that order.			
Early Life Failure Rate	ELFR	B2	Apply to MCM	N, G	231	1	0 Fails	See appendix 2 in this document	 48 hours at maximum ambient operating temperature. Voltage at Vcc maximum. The electrical verification testing needs to be completed within 48 hours of the end of stress. MCM that pass this stress can be used to populate other stress tests. Generic data is applicable. TEST before and after ELFR at room temperature. See Appendix 2 for details. 			
NVM Endurance, Data Retention, and Operational Life	EDR	В3	MCM or Individual sub- component level per AEC-Q100	D, G, K	Per AEC-Q100 minimum 30/lot or negotiated with Customer	3	0 Fails	AEC Q100-005	 TEST per AEC-Q100 requirements. Note for memory cells that may be sensitive to X-rays, an X-ray stress may be applicable. For controller-firmware-managed MCMs, the endurance and operating life portions can be performed in MCM qualification according to AEC Q100-005. Data retention can be performed on the individual components in accordance with AEC-Q100. 			

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TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS												
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS			
Wire Bond Shear	WBS	C1	Apply to Wires Within MCM	D, G	30 bonds from a devic Samples from	ces. each wire to	С _{РК} >1.67	AEC Q100-001 AEC Q003	At appropriate time interval for each bonder to be used.			
Wire Bond Pull	WBP	C2	Apply to Wires within MCM	D, G	subcomponent b MCM constru sampled. Ea composition, wir silicon metal i generate a u structure. Dupli structures need	ction is to be ch bond wire e diameter and nterface can inique bond cate wire bond	С _{РК} >1.67 or 0 Fails after TC	MIL-STD-883 Method 2011 AEC Q003	Condition C or D. Note: Wire Bond Pull/Wire Shear is not required for wire bonds that have been previously qualified inside a package. The intent is to evaluate additional wire bonds produced during the manufacture of the MCM.			
Solderability MCM External Leads	SD	C3	Apply to External Leads / Balls of MCM	D, G	15	1	>95% external lead coverage of the MCM	JEDEC J-STD-002	If burn-in screening is normally performed on the MCM before shipment, samples for SD must first undergo burn- in. Perform 8 hour steam aging prior to testing (1 hour for Au-plated leads). The customer can request justification for using dry bake in place of steam aging. Note there are circumstances that the Board Level Reliability testing per IPC-9701 can replace this test.			
Physical Dimensions	PD	C4	Apply to MCM	D, G	10	3	С _{РК} >1.67	JEDEC JESD22-B100 and B108 AEC Q003	See applicable JEDEC standard outline and/or individual MCM spec for significant dimensions and tolerances.			
Solder Ball Shear	SBS	C5	Apply to External MCM Solder Balls	В	5 balls each from a min. of 10 MCM	3	С _{РК} >1.67	JEDEC JESD22-B117	Precondition per JESD22-A113.			
Lead Integrity	LI	C6	Apply to MCM Leads / Pins	D, G	10 leads from each of 5 MCMs	1	No lead breakage or cracks	JEDEC JESD22-B105	Not required for surface mount MCMs. Only required for through-hole MCM.			
X-Ray	XRAY	C7	Apply to MCM		5 MCM for each lot				Required to document MCM construction. Not a qualification test.			
Acoustic Microscopy	АМ	C8	Apply to MCM	Ρ	10 MCM for each lot	3			Only required for surface mount MCMs that have monolithic construction as included in IPC/JEDEC J-STD- 020. Perform delamination check after TC. AM with 10 samples per lot. Delamination is not allowed, if it occurs in the area of wire bond interconnects or if it changes the thermal behavior of the MCM in a way, that it is out of specification.			

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				TES	T GROUP D –	DIE FABRICA	TION RELIA	BILITY TESTS	
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Electromigration	EM	D1	Apply to Die					JEDEC JEP001	Consult with supplier on its wafer level process characterization and/or die-level qualification data (test method, sampling, criteria).
Time Dependent Dielectric Breakdown	TDDB	D2	Apply to Die					JEDEC JEP001	Consult with supplier on its wafer level process characterization and/or die-level qualification data (test method, sampling, criteria).
Hot Carrier Injection	HCI	D3	Apply to Die					JEDEC JEP001	Consult with supplier on its wafer level process characterization and/or die-level qualification data (test method, sampling, criteria).
Negative Bias Temperature Instability	NBTI	D4	Apply to Die					JEDEC JEP001	Consult with supplier on its wafer level process characterization and/or die-level qualification data (test method, sampling, criteria). Note: Positive bias may be applicable as well.
Stress Migration	SM	D5	Apply to Die					JEDEC JEP001	Consult with supplier on its wafer level process characterization and/or die-level qualification data (test method, sampling, criteria).
				TE	EST GROUP E	- ELECTRICA	L VERIFICAT	TION TESTS	
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Pre- and Post-Stress Function/Parameter	TEST	E1	Apply to MCM	N, G	All	All	0 Fails	Test program to supplier data sheet or user specification	Test is performed as specified in the applicable stress reference and the additional requirements. All electrical tests before and after the qualification stresses are performed within the MCM specification and temperature range values.
Electrostatic Discharge Human Body Model	НВМ	E2	Apply to MCM	D	See Test Method	1	Target: 0 Fails ≥1000V	AEC Q100-002 or ANSI/ ESDA/ JEDEC JS-001	TEST before and after ESD at room and hot temperature. MCM shall be classified according to the maximum withstand voltage level. HBM < 1000V require customer notification.
Electrostatic Discharge Charged Device Model	CDM	E3	Apply to MCM	D	See Test Method	1	Target: 0 Fails <u>></u> 500V	AEC Q100-011 or ANSI/ESDA/ JEDEC JS-002	TEST before and after ESD at room and hot temperature. MCM shall be classified according to the maximum withstand voltage level. CDM < 500V require customer notification.

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TEST GROUP E – ELECTRICAL VERIFICATION TESTS (CONTINUED)												
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS			
Latch-Up	LU	E4	Apply to Active Devices	D	6	1	0 Fails	AEC Q100-004 JESD78	TEST before and after LU at room and hot temperature. See JESD78 applicability for pins to be Latch-up tested at device level.			
Electrical Distributions	ED	E5	Apply to MCM Function	D	30	3	Where applicable, C _{PK} >1.67	AEC Q100-009 AEC Q003	Supplier and user to mutually agree upon electrical parameters to be measured and accept criteria. TEST at room, hot, and cold temperature.			
Fault Grading	FG	E6	Apply to MCM Function				AEC Q100- 007 unless otherwise specified	AEC Q100-007	For production testing, see Q100-007 for test requirements. In a controller-managed MCM, FG of the controller covers the MCM.			
Characterization	CHAR	E7	Apply to MCM Function					AEC Q003	Characterization over MCM data sheet voltage / temperatures for critical performance parameters.			
Electromagnetic Compatibility	EMC	E8	Apply to MCM Function		1	1		SAE J1752/3 – Radiated Emissions	This test and its accept criteria are per agreement between user and supplier on a case-by-case basis. See AEC-Q100 Appendix 5 for details.			
Soft Error Rate	SER	E9	Apply to MCM or can be extrapolated from sub- component data	D, G	3	1		JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3	Applicable to MCM with SRAM and or/ DRAM based memory sizes ≥ 1 Mbits. Either test option (un- accelerated or accelerated) can be performed, in accordance to the referenced specifications. For controller-managed MCMs, the MCM fail rate can be determined from sub-component data (un-accelerated or accelerated) taking into account the ability of the firmware/controller to mask failures. This test and accept criteria are per agreement between user and supplier on a case-by-case basis. Final test report shall include detailed test facility location and altitude data.			
Lead (Pb) Free	LF	E10	Apply to MCM	L	See Test Method	See Test Method	See Test Method	AEC-Q005	Applicable to ALL Pb-Free MCM.			

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TEST GROUP F – DEFECT SCREENING TESTS													
STRESS			ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS								
Part Average Testing	PAT	F1	Apply to Individual Sub- components or MCM Function					AEC Q001 These tests are intended for MCMs					
Statistical Bin/Yield Analysis	SBA	F2	Apply to Individual Sub- components or MCM Function					AEC Q002	The supplier must perform some variant of PAT and SBA that meets the intent of the guideline.				
TEST GROUP G – CAVITY MODULE INTEGRITY TESTS													
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS				
Mechanical Shock	MS	G1	Apply to MCM	H, D, G	15	1	0 Fails	JEDEC JESD22-B110	Y1 plane only, 5 pulses, 0.5 msec duration, and 1500 g peak acceleration. TEST before and after at room temperature.				
Variable Frequency Vibration	VFV	G2	Apply to MCM	H, D, G	15	1	0 Fails	JEDEC JESD22-B103	20 Hz to 2 KHz to 20 Hz (logarithmic variation) in >4 minutes, 4X in each orientation, 50 g peak acceleration. TEST before and after at room temperature.				
Constant Acceleration	СА	G3	Apply to MCM	H, D, G	15	1	0 Fails	MIL-STD-883 Method 2001	Y1 plane only, 30 K g-force for <40 pin packages, 20 K g- force for 40 pins and greater. TEST before and after at room temperature.				
Gross/Fine Leak	GFL	G4	Apply to MCM	H, D, G	15	1	0 Fails	MIL-STD-883 Method 1014	Any single-specified fine test followed by any single- specified gross test. For hermetic sealed packaged cavity MCMs only.				
Mechanical Shock Cavity Device Drop	DROP	G5	Apply to MCM	H, D, G	5	1	0 Fails	JEDEC JESD22-B110	A MCM shall be defined as a failure if hermeticity requirements cannot be demonstrated. Mechanical damage, such as cracking, chipping or breaking of the package will also be considered a failure provided such damage was not caused by fixturing or handling and the damage is critical to MCM performance in the specific application.				
Lid Torque	LT	G6	Apply to MCM	H, D, G	5	1	0 Fails	MIL-STD-883 Method 2024	For ceramic packaged cavity MCMs only.				

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TEST GROUP G – CAVITY MODULE INTEGRITY TESTS (CONTINUED)													
STRESS	ABV	#	LEVEL TO TEST	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS				
Die Shear	DS	G7	Apply to Die	H, D, G	5	1	0 Fails	MIL-STD-883 Method 2019	To be performed before cap/seal for all cavity MCMs.				
Internal Water Vapor	IWV	G8	Apply to MCM	H, D, G	5	1	0 Fails	MIL-STD-883 Method 1018	For hermetically sealed packaged cavity MCMs only.				
TEST GROUP H – MODULE SPECIFIC TESTS													
STRESS	STRESS ABV # LEVEL TO TEST NOTES SAMPLE SIZE NUMBER OF LOTS ACCEPT CRITERIA TEST METHOD ADDITIONAL REQUIREMENTS												
Board Level Reliability	BLR	H1	Apply to MCM	D, G	Per IPC-9701	1	Report initial and 50% failure cycles per IPC-9701	IPC-9701 Chose the TC level and NTC requirements based on intended use environment	Temperature cycling test, state the used IPC-9701 test condition. Note: the TC cycle condition used needs to align with the MCM expected use condition (e.g., an under the hood use may dictate a TC3 or TC4). Likewise the number of thermal cycles (NTC) needs to align with the intended use environment. The ramp rate, dwell time, and test duration defined per IPC-9701. The MCM may be used in lieu of the IPC-9701 daisy chain requirement if the MCM corner solder attachments and a representable sample outer rows and solder attachments under or near major die locations can be electrically measured.				
Low Temperature Storage Life	LTSL	H2	Apply to MCM	H, P, B, D, G, K	Per Q100/Q101/Q200 minimum 30/lot or negotiated with Customer	1	0 Fails	JEDEC JESD22-A119	1000 hours at minimum ambient operating temperature. Test after LTSL at the MCM data sheet (low, high and room temperature) temperatures.				
Start Up and Temperature Steps	STEP	H3	Apply to MCM		5 MCMs	1	0 Fails	ISO 16750-4	Start up at cold and hot temperature and ramp in 10 °C increments. Confirm functionality at each step within the device specified operating range.				
MCM Drop Test	MCM DROP	H4	Apply to MCM	D, G	6 MCMs	1	0 Fails	JEDEC JESD22-B111	Condition B (1500 G, 0.5 ms half-sine pulse, equivalent drop height 112 cm), as listed in JESD22-B110B. For referencing purposes, 30 of drops are recommended.				
Destructive Physical Analysis	DPA	H5	Apply to MCM	D, G	5 MCMs	1		MIL-STD-1580	After MCM thermal cycling exposure, check key risks based on the MCM DFMEA and PFMEA.				
X-ray	XRAY	H6	Apply to MCM		5 MCM for each lot				X-ray test not required if X-ray test is done in Test Group C. See Test Group C X-ray (XRAY) for details.				
Acoustic Microscopy	AM	H7	Apply to MCM	P, G	10 MCM for each lot				Acoustic Microscopy test not required if Acoustic Microscopy test is done in Test Group C. See Test Group C Acoustic Microscopy (AM) for details.				

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Legend for Table 1

- Notes: Required for hermetic packaged MCMs only. н
 - Ρ Required for plastic packaged MCMs only.
 - в
 - Required Solder Ball Surface Mount Packaged (BGA) MCMs only. Nondestructive test, MCMs can be used to populate other tests or they can be used for production. Ν
 - Destructive test, MCMs are not to be reused for qualification or production. D
 - Required for surface mount plastic packaged MCMs only. S
 - G Generic data allowed.
 - Use method AEC-Q100-005 for preconditioning a stand-alone Non-Volatile Memory integrated circuit or an integrated circuit with Κ a Non-Volatile Memory MCM.
 - L Required for Pb-Free MCMs only.

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Table 2: Process Change Qualification Guidelines for the Selection of Tests

- A2 Temperature Humidity Bias or HAST A3
- C1 Wire Bond Shear C2 Wire Bond Pull
- Autoclave or Unbiased HAST
- A4 Temperature Cycling
- A5 Power Temperature Cycling
- A6 High Temperature Storage Life
- B1 High Temperature Operating Life
- B2 Early Life Failure Rate
- B3 NVM Endurance, Data Retention
- Solderability C4 Physical Dimensions

C3

- C5 Solder Ball Shear
- C6 Lead Integrity
- C7 X-ray / CŠAM

- E2 Human Body Model ESD E3
 - Charged Device Model ESD
- E4 Latch-up
- E5 Electrical Distribution
- E6 Fault Grading
- E7 Characterization Electromagnetic Compatibility
- E8 E9 Soft Error Rate

Note: A letter or "•" indicates that performance of that stress test should be considered for the appropriate process change. Reason for not performing a considered test should be given in the qualification plan or results.

	Test #	A2	A3	A4	A5	A6	B1	B2	B3	G	C2	ប៊	C4	C5	C6	C7	E2	E3	E4	E5	EG	E7	E8	E9
	Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	Ъ	SBS		XRAY	HBM	CDM	LU	Ē	EG	CHAR	EMC	SER
Change Type	Change Impact																							
Any	Critical characteristics of module are affected	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	М
Substrate change affecting module schematic	Critical characteristics of module are affected		•	•			•	•									•	•	•	•	•	•	•	М
Substrate change affecting module schematic	Critical characteristics of module are not affected			•			•										•	•	•	•	•	•		М
Change that adds or subtracts sub-components from the module BOM	Any		•	•			•	•									•	•	•	•	•	•	•	М
Change to the processes used in during module assembly (e.g., pick & place, reflow, encapsulation, singulation)	Any	•		•						•	•		•	•		•								
Change to testing platform	Any																			٠				
Change to testing location	Any																			٠				
Change to assembly location	Any	٠	٠	•	•		٠	•		•	•	•	•	•	•					•				
Change to materials used in module assembly (e.g., adhesive, underfill, encapsulant, solder, epoxy)	Any	•		•						•	•	•	•	•	•					•				М
Change from an AEC Qualified sub-component to a Non-AEC Qualified sub-component	Any	•	•	•	•	•	•	•	•								•	•	•	•	•	•	•	М
Change from a Non-AEC Qualified sub-component to another Non-AEC Qualified sub-component	Any	•	•	•	•	•	•	•	•								•	•	•	•	•	•	•	М
Change from one AEC Qualified sub-component to another AEC Qualified sub- component	Critical characteristics of sub-component are affected						•		•								•	•	•	•	•	•	•	М
Change from a Non-AEC Qualified sub-component to an AEC Qualified sub-component	Any						•		•								•	•	•	•	•	•	•	М
Change from an AEC Qualified sub-component to another AEC Qualified sub-component	Critical characteristics of sub-component are <u>not</u> affected																					•	•	
Change within an AEC Qualified sub-component that has been requalified	Critical characteristics of sub-component are affected						•		•								•	•	•	•	•	•	•	М
Change within an AEC Qualified sub-component that has been requalified	Critical characteristics of sub-component are <u>not</u> affected																			•			•	

M - Applicable for subcomponents with > 1M SRAM or DRAM per AEC-Q100

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Appendix 1: Q104 Certificate of Design, Construction and Qualification. Template shown below is for example only. Refer to released AEC-Q104 Multi-Chip-Module CDC Template available from the AEC website at http://www.aecouncil.com

Item Name	Supplier Response
M1. User's Module Part Number:	
M2. Supplier's Module Part Number/Data Sheet:	
M3. Module Description:	
M4. Included ICs:	
Device name/description and AEC-Q100 status (Y/N):	
a. Sub-IC #1:	#1:
	#1 AEC-Q100: Yes No
b. Sub-IC #2:	#2:
5. Oub-10 #2.	#2 AEC-Q100: Yes No
c. Sub-IC #3:	#3:
	#3 AEC-Q100: Yes 🗌 No 🗌
M5. Included Discretes:	
Device name/description and AEC-Q101 status (Y/N):	
a. Sub-Discrete #1:	#1:
	#1: AEC-Q101: Yes No
b. Sub-Discrete #2:	#2:
	#2 AEC-Q101: Yes No
c. Sub-Discrete #3:	#3: #3 AEC-Q101: Yes 🗌 No 🗍
	#3 AEC-Q101: Yes No 4
d. Sub-Discrete #4:	#4. #4 AEC-Q101: Yes No
M6. Included Passives:	
Device name/description and AEC-Q200 status (Y/N):	
	#1:
a. Sub-Passive #1:	#1 AEC-Q200: Yes No
	#2:
b. Sub-Passive #2:	#2 AEC-Q200: Yes No
	#3:
c. Sub-Passive #3:	#3 AEC-Q200: Yes 🗌 No 🗌
	#4:
d. Sub-Passive #4:	#4 AEC-Q200: Yes 🗌 No 🗌
M7. Module Assembly Location & Process ID:	
a. Facility name/plant #:	
b. Street address:	
c. Country:	
M8. Module Quality Control A (Test) Location:	
a. Facility name/plant #:	
b. Street address:	
c. Country:	
M9. Module Packaging System:	
a. Type of package (e.g., laminate, leadframe, etc.):	
b. External ball/lead count:	
c. JEDEC designation (e.g., MS029, MS034, etc.):	
d. Lead (Pb) free (< 0.1% homogenous material):	
e. Package outline drawing:	See attached Not available

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Appendix 2: MCM Early Life Failure Rate (ELFR)

A2.1 SCOPE

This test method is applicable to Multichip Modules (MCM) qualifications. In the case of many MCMs, generic data (see AEC-Q104, Section 2.4 may fulfill the requirements of this test method. If the supplier is qualifying a MCM for which no generic data is available (unproven technology or design rules) for general use, then the requirements of this test method should be utilized to meet the requirements of AEC-Q104. If the supplier is qualifying a MCM for a single user, that user may optionally designate the implementation of AEC-Q001 as a substitute for ELFR. All parts used for such a qualification must have been evaluated to AEC-Q001 tests and limits approved by the user. If AEC-Q001 is utilized, the user shall review and approve of the particular tests and the method used to determine test limits. (Note: The failures from ELFR and AEC-Q001 do not always show a 1:1 correlation.)

A2.1.1 Description

This MCM Early Life Failure Rate (ELFR) establishes the testing method for evaluation of early life failure characteristics on MCMs that are utilizing new or unproven processing technology or design rules where generic data is not available. This would include MCMs for which there is no prior usage information or generic data. Unsatisfactory results in this evaluation indicate that corrective action is required and the MCMs may require processing changes, design changes, burn-in, more aggressive burn-in, or application of statistical part test limits (see AEC-Q001).

A2.1.2 Reference Documents

AEC-Q001 Guidelines for Part Average Testing JEDEC JESD22-A108 Bias Life

A2.2 PROCEDURE

A2.2.1 Sample Size

The sample size shall be per Table 1 of AEC-Q104. In the case of MCMs that are deemed too expensive, the requirement for use of this test method and the sample size will be based upon agreement between the user and supplier.

A2.2.2 General ELFR Procedure

The MCM shall be tested per the High-Temperature Operating Life (HTOL) requirements in JEDEC JESD22-A108 with the following special condition. The ambient test temperature shall be per the applicable operating temperature grade as defined in AEC-Q104 Section 1.3.6 for 48 hours.

A2.2.3 Acceptance Criteria

The MCM shall be functionally tested within 48 hours after completion of high temperature exposure. Testing shall be at room temperature. Failures during this test are not acceptable and indicate that corrective action must be taken. The supplier shall notify all interested users of this non-conforming condition and the corrective action that has / will take place. The user(s) must approve of the corrective action for the MCM to be qualified.

A2.2.4 Sample Disposition

MCMs that pass electrical testing after this test can be used to populate other non-operating tests. These MCM can also be supplied as production material if agreed to by the user.

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Revision History

Rev #Date of changeBrief summary listing affected sections

- Sept. 14, 2017 Initial Release.