# Automotive Electronics Council

## Component Technical Committee

# Technical Session Abstracts

*(Agenda subject to change)*

## 2018 - Twentieth Annual Automotive Electronics Reliability Workshop

## April 24, 25, & 26

## Novi, MI
## Sheraton Detroit Novi Hotel

**1.1 Tantalum Capacitor Technology Update & Comparison**

*C. Reynolds, AVX*

Tantalum capacitors have evolved from their initial form of MnO2 based technology, to self-healing Niobium Oxide devices and now AEC Q200 qualified Tantalum Polymer capacitors. This presentation will briefly look at the electrical and environmental performance properties of all technologies relative to one another. End user storage & process conditions will be presented in comparative tables. Performance characteristics will be compared to Aluminum Electrolytic Capacitors and high C/V MLCCs. Future applications, such as critical safety and priority data circuits will be briefly discussed with the capacitors impacts upon circuit performance identified. Circuit use recommendation will be made based upon capacitor performance. Predictions of future products will be made based upon current R&D efforts.

**1.2 Passive Components for More Efficient Wide Band Gap Power Conversion**

*P. Blais, KEMET*

Wide Band Gap semiconductor based inverters and power conversion impose new demanding challenges for the capacitors and magnetics used in these circuits ranging from temperature, frequency and efficiency. KEMET will discuss Class 1 ceramic technology and TLPS developed to address these needs along with magnetics.

**1.3 Tantalum Polymer Surface Mount Capacitors: New Solutions for Automotive Applications**

*K. Moore, KEMET*

The usage of legacy MnO2 tantalum capacitors in automotive applications has had its past challenges. The industry's transition from a single source to multiple sources of ore has addressed the concerns with supply. Technical breakthroughs allowing full AEC-Q200 qualification of tantalum polymer caps have addressed the concerns with safety. Alleviation of these concerns have come at a time when market drivers such as connectivity and self-driving functionality are requiring better capacitance solutions for the various CPU, logic, and input rails. In addition to providing a safe-failure mode, tantalum polymer capacitors provide better capacitance stability, better capacitance retention, lower ESR, higher ripple handling, and long life. In this presentation, the product features and electrical performance, including load dump, of these fully qualified AEC-Q200 tantalum polymer capacitors will be provided. Also, the results of the initial evaluations for extending the operating temperature from 125°C to 150°C will be given.

**W.1 AEC-Q200 Document Revision Status & Discussion**

*Moderator: AEC Q200 Technical Committee*

**2.1 Stress Test EOS & ESD Pre-damage Study of A Power Device: Press-fit Rectifier Diode for Automotive Alternator**

*C. Lin, Actron Technology*

An in-depth study of EOS/ESD pre-damage in automotive press-fit rectifier (a typical silicon p/n junction diode; also a TVS diode) successfully reveals the subtle effects & signatures of certain reverse surge stress tests & ESD test, which can incur the latent failures in field, e.g., 0KM & warranty failures. The experimental study is performed on silicon p/n junction diodes (AC to DC rectifiers of automotive alternator), which is the most fundamental semiconductor power device. The findings of the subtle pre-damage by certain reverse surge stress tests widely required and used by some car-makers, Tier-1 alternator makers & most of the Tier-2 press-fit diode makers, load-dump tests, and also ESD zapping (simulated by ESD gun), can help a lot on the elimination of the occurrence, which paves the way of the last mile on reducing current field failure ppm (<0.5ppm) to the extreme goal of 0 ppb, since EOS & ESD often occupy 60~70% of the field failures. The study methodology (DOE adopted) and the statistically proven subtle pre-damage can also help the earlier identification & elimination of the possibly pre-damage induced field ppm, by the similar stress tests, required on some automotive ICs, with also the similar TVS diodes for the I/Os' ESD protection, and plenty of p/n junctions inside the ICs.

**2.2 Demonstrating GaN Power Switch Robustness**
*R. Barr, Transphorm Inc.*

GaN power switches can only be adopted by the automotive market when the fundamental failure modes, acceleration factors, and statistics can be demonstrated. In general, ultimate intrinsic lifetime is an important measure of product reliability and robustness. To the automotive market, however, the anticipated failure rate during a product's first 10 to 20 years of use is of particular interest as it has direct impact on warranty costs. Passing AEC-Q101 testing is a critical first step in gaining acceptance into automotive applications. But, it is not enough. Testing to failure of statistically significant samples of devices to determine early life failure rates must be conducted so that meaningful data on reproducibility of the manufacturing process can be demonstrated to the customer and the understanding applied to the product's mission profile. While all failure modes are important in the end, high voltage off-state testing is a particularly difficult test for GaN power devices to pass. As such, this paper will discuss the methods developed for measuring GaN reliability on large samples. Further, the paper will discuss how the resulting data can be used to supplement Q101 testing results when the failure modes and acceleration factors are well understood.

**2.3 Making Semiconductor Lasers Reliable For New Automotive Applications – Opportunities & Challenges**
*Dr. C. Jung, OSRAM*

Semiconductor lasers are highly complex products offering an excellent electro-optical performance as high wall-plug efficiency, high optical output power coherent light emission and low beam divergence. Thus semiconductor laser have the potential to become the future technology for head-up displays, headlamps or LIDAR for pre-crash sensing and adaptive cruise control (ACC). This presentation will start with a brief introduction of different laser packages (e.g., TO metal cans, SMD, plastic package, components with integrated converter and optics, etc.) which are used in automotive applications. The focus will be on the defined stress requirements in the current AEC Q102 with respect to application to all relevant laser packages. Also the differences between the testing requirements in AEC Q102 and the proposal for IEC-60810 will be discussed. Furthermore, the impact of the electrical driving mode (e.g., DC and pulsed operation) for visible and high power IR laser on the stress requirements will be discussed in detail as well as typical failure mechanism for semiconductor laser. Finally, limitations at the laser package characterization regarding the failure criteria judgement will be explained.

**W.2 AEC-Q101 Document Revision Status & Discussion**
*Moderator: AEC Q101 Technical Committee*

**W.3 AEC-Q102 LED Qualification Document Revision Status & Discussion**
*Moderator: L. Kappius, Hella KGaA and AEC-Q102 Sub-Committee*

### 3.1 Reliability Capability of Cu-wire in Automotive Electronics

*R. Rongen, NXP Semiconductors*

Over the past decade, Cu-wire bonding has been gradually industrialized. Meanwhile, it has become a mature technology. In 2015, the Automotive Electronics Council did publish the first version of a Cu-wire specific qualification standard, which was already revised in 2016 [1]. The content of this standard reflects the less mature experience with Cu-wire compared to Au-wire in automotive electronics. Knowledge on the fundamentals of the Physics-of-Fail and Physics-of-Degradation for Cu-wire has increased rapidly though in the last couple of years. This paper intends to show a comprehensive overview of these learnings concerning the reliability capability of Cu-wire. All phases of the "bathtub curve" will be addressed; from manufacturing control during chip assembly until early life and wear out performance. Emphasis will be on fracture and corrosion of first and second bond contacts. The relevance of assessing degradation aspects will clearly be demonstrated. In a first example, it will be shown how this resulted into the Cu-Al ball shear spec, lately published by JEDEC [2]. Also presented, are considerations on how to realize reliability robustness for automotive applications at elevated temperatures. Potential modifications in the future update of the AEC-Q006 [1], will be addressed in the final part of this paper.

References:

[1] Qualification Requirements for Components Using Copper (Cu) Wire Interconnections, AEC-Q006- rev (June 8, 2015) and rev A (July 1, 2016)

[2] Stress-Test- Driven Qualification of Integrated Circuits, JESD 47J (August 2017) and J.01 (September 2017)

### 3.2 Implementing AEC-Q006 in the Development and Qualification Process

*U. Abelein, Infineon Technologies AG*

The AEC-Q006 turned out to be the reliability related document with the most importance to the automotive semiconductor industry since the publication of AEC-Q100/101. With its release in June 2015 it aimed to provide a standardized and transparent way for the save qualification of Cu wire technology to automotive applications. But the efforts coming with the AEC-Q006 to the semiconductor suppliers are much more than just doubling the stress time. Introducing the standard to the development and qualification flow needs a structured approach by the responsible semiconductor company. The talk will give an overview of the impact of AEC-Q006 on the development and qualification processes. It will outline the necessary efforts at different points of the product life cycle. Taking these efforts and the reliability targets of the standard as boundary conditions it will furthermore sketch a successful executed introduction strategy into the business processes. The advantages for supplier and customer of this strategy will be highlighted. Finally the necessary framework to sustainably maintain the AEC-Q006 targets, mindset and regulations in the organization will be discussed.

### 3.3 Fast Transient Thermomechanical Stress for Lifetime Estimation of Sintering Die Attach Layer on Automotive Packages

*M. Santopa, STMicroelectronics*

Automotive applications show a challenging trend towards higher ambient temperatures and longer lifetime requirements. In fact, more complex functionality generating more heat losses, higher integration that worsens the cooling possibilities, mounting in more exposed areas near engines, extended lifetimes for electrification of power train are taking place in automotive IRD. For this reason, Silver (Ag) sintering technology for high temperature electronics packaging is becoming a wider spread used and more reliable alternative to soft solder in high temperature and high power density applications. With the diffusion of wide bad gap semiconductors (e.g., SiC), operation temperature has reached more than 200 °C; consequently, higher solder's strength and reliability performances (longer lifetime) are required for die attach materials (solder fatigue).

In this paper, Ag sintering pressure-assisted layer has been investigated when submitted to fast transient thermomechanical stress ($\Delta T/\Delta t > 100$ °C/min) for lifetime estimation on automotive packages. The die sintering is performed on Ag substrate metallization for improving adhesion performance. The stress is provided by thermal shocks in liquid-to-liquid ambient (PFPE - perfluoropolyether oil) using temperature range of -65 °C/+150 °C (3min cold/3min hot, 6min/cy). Fast transient thermomechanical stress with increasing sintering pressure has been investigated as well. Experimental data confirmed that using the assumptions identified by the finite element model for simulation, it's possible to reach extended reliability performance covering the mission profile of electric vehicles. At the end, failure analysis results showed that Thermal Shocks signature stress is almost comparable to Power Cycling's one in terms of wire bonding degradation and die attach layer creeping. See below pictures for reference.

### 3.4 Mechanism-Driven Solutions of Al-Cu Bond Pad Pitting for Ensuring High-Quality Automotive IC Products

*L. Sheng, ON Semiconductor*

The addition of Cu to Al for enhancing the EM performance in metallization inherently increases the susceptibility of Al-Cu films to corrosion. The pitting occurrences on Al-Cu alloy pads have been reported at wafer manufacturing and packaging processes, where galvanism was generally recognized with Cu cathodes and corroded Al anodes. However, the papers over the past decades mostly focused on searching the electrolyte sources needed to activate the Al-Cu micro-corrosion cells. On one of our automotive IC designs, pad pitting was randomly observed on the lots for the process Cpk analysis prior to product reliability qualification. Starting with a description of the issue, the presentation will mainly address the pad-dependent corrosion phenomena clarified for the first time by extensively reviewing a set of standing-alone components on SLMs. Our insights of networking corrosions have strongly suggested that the Al-Cu corrosion mechanism should be more broadly examined than the micro-corrosion on individual pits. Furthermore, the IC product, when integrated with these components, consistently exhibited a clearly enhanced corrosion mechanism on a specific pad, which provides the potentials of design-for-reliability added to process improvement. The unbiased and biased HAST results will also be presented by comparing between pitted and pitting-free samples.

### 4.1 Component Safe Launch in Today's Automotive Environment

*W. Chen, Macronix International Co., Ltd.*

With electronics experiencing tremendous growth in today's automotive market through new applications such as connected car, semi-autonomous driving and all-electric models, there is a need for evermore improvements in quality while at the same time introducing new components from lead edge technologies. This environment increases pressure on the component supplier to release products to the automotive market with shorter qualification windows and reduced data set. For this reason the component supplier must rethink the method of evaluating risk during new product introduction and must determine new ways to assure a 'safe launch' of new technologies for new automotive applications. This paper sets out to show the current industry practice of safe launch from the Tier 1 perspective and from the component supplier perspective. It will show the differences between the two safe launches and how they overlap. The paper will then focus on the key elements of a component safe launch plan. Many of these elements will need to be re-examined or changed to address the new demands on electronics in automotive. For example, manufacturing stability of new technologies is a key element of component release. However, many components are now being released to automotive without the necessary time to stabilize fab yield. In this case, how can the component supplier build a level of confidence to release a product? What are the risks? How can the risk be evaluated? The paper will show some examples of ways to evaluate risk under these circumstances. In summary, the paper will show how the safe launch concept should be an important part of each component supplier's new product release and new methods for evaluating and mitigating risk need to be considered during this safe launch period.

### 4.2 Meeting Automotive ESD and System Efficient ESD Design (SEED) Requirements with Lower Process Technology Node

*K. Semmoud, Xilinx*

Protection against ESD events is a key design parameter enabling automotive applications which require semiconductor components with high reliability and a long lifespan in hostile environments coupled with low return rates. With Moore's law, the scaling trend of the semiconductor industry leads to a reduction in component-level Electrostatic Discharge (ESD) immunity. The automotive industry is reluctant to accept the consequent scaling of component ESD immunity and continues to adhere to legacy ESD component targets. To address the widening gap between component and system ESD specifications, the industry came up with the new System Efficient ESD Design (SEED) methodology that calls for co-design of onboard and on-chip ESD protections to achieve the goals of system-level ESD robustness. Electronic equipment ESD safety is guaranteed with two levels of ESD protection: On-chip component level and system level. The latter is implemented with dedicated components mounted on a PCB. This paper describes ESD protection of the 16nm Zynq® UltraScale+™ MPSoC and highlights its advantages for integration into highly demanding automotive System Efficient ESD Design.

### 4.3 Using Automated Design Analysis to determine Solder Fatigue and Joint Cross Section Strategies

*M. Oxner, General Motors*

A PCB's response to Thermal Fatigue and Mechanical stresses are known to affect solder joints of the components populating the PCB which leads to failures in application. This presentation takes a look at using Automated Design Analysis tools to determine fatigue of solder joints, when they fail, and how long it takes to get there. It will also leverage the results of the analysis to drive an improved cross sectioning strategy to monitor joints following validation testing. The presentation will use examples of cross section joints from varying life cycles to determine the accuracy and benefit of the models results. The results show that utilizing an Automated Design Analysis tool hold a large value to teams as they develop PCBs for future applications. Utilizing a tool such as this can prevent premature validation failures which drives test time and potential delays in root causing. By performing this type of analysis early in development stages not only is the expected fatigue understood, but an effective strategy to examine other joints can be created as well.

## 5.1 Extended Lifetime Qualification based on Standard Mission Profiles

*U. Abelein, Infineon Technologies*

The current megatrends e-mobility, connectivity and autonomous driving are changing the game in the automotive industry. Novel operating states, e. g., charging of the vehicle, are coming with the applications developed within this framework. The results are significantly extended lifetime requirements. Regularly the AEC-Q100/101 stress test conditions are no longer suitable to qualify a according to these mission profiles. Therefore the number of customer specific qualifications which exceed the standard qualification is growing while the relevance of standard is continuously decreasing.

Depending when these customer specific requirements are placed their acceptance can lead to:

- prolonged time to market
- additional qualification efforts
- need for product changes

For the customer this leads to:

- reduced product availability
- increased costs
- risk for their development timeline

Therefore and extension of the standard to cover most of these extended lifetime requirements is beneficial for both supplier and user. This talk discusses a potential solution of extending the AEC-Q100 by standardized lifetime requirements, i. e., standard mission profiles. It will demonstrate the technical advantages of this approach compared to standardized test conditions, the qualification process (derived from the appendix 7 flow) and potential content of such standard mission profiles.

## 5.2 Latent Reliability Defects in Automotive Chip Packages

*S. Leeman, KLA-Tencor ICOS*

The expanding number of safety, comfort and connectivity features in cars is increasing the number of automotive chips. Infotainment and navigation systems, engine management, radar assisted cruise control, lane detection cameras and parking assist are now increasingly common features. Once only an idea found in a futuristic movie, fully autonomous driving is far enough along to be considered a reality. Automotive ICs are different than those found in most mobile devices, tablets and laptops. They have higher reliability requirements, in part, because they must be able to handle three different aspects of an extreme environment. Firstly, the automotive chip will be exposed to high temperature and humidity variations. For example, on a winter day the car may be parked outside at -20˚C, and then the driver will heat the interior to a comfortable +22˚C in a short time span. Secondly, while driving, these components experience significant shock and vibration on rough roads. Finally, it is expected that a car will be in operation for well over ten years, meaning the automotive chips must remain functional during this time span.

The increasing number of automotive chips in each car, and the unique challenges from the extreme environment, results in extra attention on chip quality, reliability and robustness. The standard packaging inspection flow already removes dies with obvious killer defects. This is not sufficient to meet the quality requirements for the automotive industry. Attention is needed on packaging defects that result in reliability issues, termed “latent defects.” Like with killer defects, the goal is to remove all components containing latent defects from the assembly line. We will describe a set of methodologies for component inspection to bring focus to this defect type. These methods will include automated visual component inspections focused on finding latent defects such as micro-cracks, burrs, or dirt on an electrical contact, because these defect types have a direct impact on chip reliability. We will show how implementation of these new inspection techniques can help identify and remove these components from the manufacturing line in order to meet aggressive automotive standards.

### 5.3 Evolution of Risk Mitigation: Testing with Deep and Machine Learning Application Based Analysis for Defect Exclusion

*K. Semmoud, Xilinx*

Advanced leading edge technologies have led to a need for evolutionary thinking around testing and the analysis of quality and reliability of components. We will discuss novel new approaches to testing and subsequent analysis methodologies. Burn-in elimination is a fact of life in the most advanced technologies as the risk of incidental damage far outweighs the risks of the intrinsic defects burn-in is tasked with eliminating. Further development of test strategies using application or use model based testing, as well as development of Deep Learning and Machine learning principles leveraging test data lead to high levels of defect detection, isolation, and risk mitigation.

### 5.4 Inline Defect Parts Average Testing (I-PAT)

*D. Price, KLA-Tencor Corp.*

The convergence of several significant trends in the automotive space is having a profound impact on the importance of process control for automotive semiconductors. Both IDMs and fabless/foundry manufacturing models are recognizing the need to make fundamental changes in their historical approach in order to respond to these trends and be successful in the competitive automotive market. One of the larger obstacles to success is the so-called "latent defect." These defects may be of a size or location that they do not initially kill the die, or they may lie in an untested area of the die (an increasing problem with complex SOCs). As a result, the die passes electrical test and "escapes" into the supply chain. The demanding automotive environment of high heat, humidity and vibration can subsequently "activate" a small portion of these defects, causing a premature failure.

Automotive semiconductor fabs have long used inline defect inspection to drive continuous improvement (defect reduction) and excursion monitoring. More recently, fabs have begun to use inline defect inspection for die-level screening of large ("macro") level defects. While effective for large defects, this method is inadequate alone for latent defects. At the 2017 AEC Conference, KLA-Tencor introduced a new methodology which applies the 20-year-old automotive industry technique of Parts Average Testing to inline defect data. Specifically, Inline Defect Parts Average Testing (I-PAT™), identifies outlier defect populations that are statistically more likely to contain the latent defects. We will provide an update on industry adoption of this methodology, including projected use cases, implementation schemes, and initial results.

### 6.1 Calculating Probability Metric for Random Hardware Failures (PMHF) in the new version of ISO-26262 Functional Safety – Methodology and Case Studies

*B. Knoell, NXP Semiconductors*

The Automotive Functional Safety standard ISO-26262 introduced a PMHF (Probabilistic Metric for random Hardware Failures) in Part 5 and Part 10 by calculating the system failure rates and assessing the ASIL (Automotive Safety and Integrity Level) for functional safety. The new version of the standard expands the PMHF concept by further promoting a new metric, "average probability of failure per hour over the operational lifetime of the item", which has not been commonly used by the reliability engineering community. In order to clarify how PMHF is calculated within the content of ISO-26262, this paper will discuss how to calculate both the failure rate and the average probability of failure per hour in terms of definitions, sources of the data, applications, and advantages and disadvantages. We will also present examples of calculating PMHF including the average probability of failure per hour for a nonexponentially distributed failure population as well as an example of a system with redundancy. Finally, we will present a method for evaluating the ASIL level based on the available information.

### 6.2 Failure Rates and Failure Distributions of Electronic Components for Functional Safety

*Dr. V. Tiederle, RELNETyX Consulting UG*

The functional safety specification is often a requirement for new sophisticated automotive electronics to ensure a robust and reliable product. This is also valid for autonomous driving and for this topic even more important. The new version of ISO-26262 for the evaluation of hardware 2 different methods are mentioned:

- Constant failure rate – that means random failure / handled mainly by standards
- Increasing failure rate – that means wear out failure / Handled by physics of failures

The use of standards for the constant failure rate is widely discussed. The problem is the actuality of these standards. Another problem is the fact that the failure rates and also the failure distributions cannot be verified by real facts from the field. On the other hand for the critical applications like autonomous driving the coverage of the safety mechanism should be proven by the approved metrics. In this metrics the most popular method is the use of constant failure rates. New technologies – not covered by any standards – are widely used in these critical applications. Those new technologies should be handled in the same manner from all competitor on the market. In this presentation some examples are shown to demonstrate the need for a harmonized understanding in these investigations. One of the examples will be the different types of ceramic capacitors.

### 6.3 Initiatives for Addressing ISO-26262 Hardware Risk Assessments

*K. Hodgson, Ford Motor Company*

The Road Vehicle Functional Safety Standard ISO-26262-2011 requires a risk assessment of safety related Electrical/ Electronic (E/E) hardware using a new, non-traditional metric called the Probabilistic Metric for (Random) Hardware Failures (PMHF). The underlying philosophy of this approach is that E/E failures are inevitable, and the PMHF metric is used to determine the degree of "Safety Mechanism(s)" needed to prevent failures from evolving into unsafe conditions for each safety critical element in a vehicle system. PMHF analysis starts with classical (1950 era) "Part Counting" reliability prediction from actuarial handbooks of historic, averaged failure rates for generic categories of E/E components such as US MIL-HDBK-217, German Siemens SN29500 and French Fides UTE C80-811. These methods compress complex failure histories into simple generic averages applied as a constant over the life of E/E components and systems. The US automotive OEMs abandon actuarial reliability predictions methods back in the 1990s as they were found to be inaccurate due to over simplification and flaws in the categorization of handbook failure data. The greatest shortcoming is that E/E technology evolves so fast, that by the time years of field failure rate data are compiled on a generation of E/E tech, the next generations of E/E components and materials being designed into new products will have different failure susceptibilities and failure rates so that failure rates from older tech is not applicable.

The soon to be published 2018 ISO-26262 update, recognizes using scientific, Physics of Failure (PoF) based Reliability Physics Analysis (RPA) implemented in Computer Aided Engineering (CAE) Durability Simulations as an alternative to purely actuarial-probabilistic methods. Instead of only identifying a failure risk metric, RPA identifies design and application specific failure risk early in the design cycle so that they can be designed out of new product. This Virtual Reliability Growth capability supports a reliability by design approach to preventing safety risks that will be especially important for Autonomous Vehicles which require new advanced, larger and hotter running ICs that will be susceptible to different failure characteristics and lack the years of field history needed for actuarial probabilistic predictions. This presentation summaries how RPA methods for circuit board assemblies outlined in SAE J-1211 and for Semiconductor in SAE ARP6338 can be applied in ISO-26262 PMHF risk analysis based on recent trials at Ford and will introduce a new project to develop a joint SAE Automotive and Aerospace standard to define the Reliability Physics Analysis process.

**W.4 Industry Review of AEC Relevant Papers**
*Moderator: Bob Knoell, NXP Semiconductors*

**W.5 AEC-Q100 Document Revision Status & New AEC Initiatives**
*Moderator: AEC Q100 Technical Committee*

**W.6 AEC-Q103-003 Microphone MEMs Activity Update & Discussion**
*Moderator: B. Atala, STMicroelectronics*

**W.7 AEC-Q004 Zero Defects Activity Update & Discussion**
*Moderator: AEC Q100 Technical Committee*