Automotive Electronics Council

Component Technical Committee

Technical Session Abstracts

(Agenda subject to change)

2017 - Nineteenth Annual Automotive Electronics Reliability Workshop

April 18, 19, & 20

Novi, MI
Sheraton Detroit Novi Hotel

1.1 Reliable SMD Fuses (Surface-Mounted Device) for Overcurrent Protection from 12VDC to 400VDC
P. Straub, Schurter AG

Fuses have to open an electric circuit in case of overcurrent and therefore help to protect equipment from damage, explosion or fire. All fuses incorporate an element which melt after some time in case of overcurrent and then vaporize. The resulting arc must be extinguished to achieve a proper interruption. Compact SMD fuses for DC voltage becoming more and more popular in automotive applications. SMD fuses and power transistor modules are mounted reliable and cost effective directly onto the surface of printed circuit boards. The presentation compares different modern SMD fuse construction under the aspect of performance and reliability. Failure mode of the different fuse constructions will be discussed and compared to each other. Fuse applications will be presented in the area of space, aviation, industry and automotive. The increasing fuse requirements for the electrification of cars will be presented and discussed. A qualification concept for automotive SMD fuses will be presented on the base of AEC-Q200 and fuse qualification standards.

1.2 Experimental Reproduction of Copper Dendrite Growth with Standard H3TRB-Chamber
V. Cavallaro, STMicroelectronics

The phenomenon of copper dendrite growth is well known for decade. The primary operating parameters that promote electro migration phenomenon are listed:

1. Moisture
2. Contamination on the insulator surface
3. Voltage difference between conductors
4. Narrow spacing widths
5. Elevated temperatures (at high relative humidity)

(Source: Simeon J. Krumbein, Metallic Electromigration Phenomena, AMP Incorporated, Harrisburg, Pennsylvania, 1987)

The prevention of the copper dendrite in the semiconductor industry is fundamental to avoid reliability failure. On the other side, the apparatus required to create the suitable environmental condition to induce the dendrite is complex and expensive. The present work describes an experimental method able to promote the copper dendrite inside the H3TRB chamber without inducing any contamination of the apparatus.

1.3 Gallium Nitride Power Switch Reliability
K. Smith, Transphorm, Inc.

Gallium Nitride based power devices have demonstrated significant advantages in efficiency and size reduction that are critical to automotive applications. While the reliability of GaN based electronics has been demonstrated with a high degree of confidence, market adoption depends in part on the ability of GaN technology to meet the Q101 qualification standards. These standards rely on the understanding of the acceleration factors of the underlying failure mechanisms that limit device lifetime. This paper will discuss the reliability testing that has demonstrated wear out of > 100years at very low failure rates for both the conducting and blocking operation of the GaN power switch. During conduction, the power device is limited by a temperature related mechanism identical to the limiting factor in RF devices that are in commercial and space applications. Blocking of high voltage is unique to GaN power switches and both temperature and voltage acceleration factors will be discussed.

W.1 AEC-Q200 Document Revision Status & Discussion
Moderator: AEC Q200 Technical Committee

W.2 AEC-Q101 Document Status & Discussion
Moderator: AEC Q101 Technical Committee

W.3a Overview of LED-Related Standards
Dr. P. Plathner, OSRAM

Over the past 10 years, the development and use of LED products has increased enormously. In parallel to the market penetration of these LED products, standards were and are being developed to enable market access and to support the industrial processes. This presentation will provide an overview of national, regional and international standards for LED products. It will cover standards for the different integration levels (e.g., LED chip, LED package, LED lamps, LED modules, LED luminaires) and the main fields of applications (e.g., general lighting, automotive, etc.). A summary of standards for both safety and performance aspects of these LED products will be presented. In addition, an overview of the main national and international committees working on LED standardization will be given. Standards related to LED reliability and standards related to automotive applications will be presented in more detail.

W.3b AEC-Q102 LED Qualification Review & Discussion
Moderator: L. Kappius, Hella KGaA and AEC-Q102 Sub-Committee

W.4a Microphone MEMs Activity Update
Moderator: B. Atala, STMicroelectronics

W.4b AEC-Q103-002 Pressure Sensor MEMs Qualification Update
Moderator: E. Fischer, Autoliv Electronics and AEC-Q103 Sub-Committee

W.5 EOS Mitigation and Communication Procedures
Moderators: L. Masseus, Infineon & B.Knoell, NXP Semiconductors

2.1 Juggling Knowledge Based and Standards Based Qualifications
B. Knoell, NXP Semiconductors

This compromise can also be between application-specific and stress-test based qualification methods or between physics-of-failure and right-censored testing. In one case, an application that fits, say, the 90th percentile of customer usage that utilizes one set of tests, conditions and durations versus one where the application determines a variable set of tests, conditions and durations. In the other case, a set of tests, conditions and durations that are based on the acceleration of known specific physical failure mechanisms versus a set of tests, conditions and durations based on a set of known stimuli such as temperature, humidity and mechanical stress experienced in the field. This tutorial will go through the advantages and limitations of each method to give the viewer an idea of when to utilize each for their qualification program.

2.2 Profound Incentives of Wafer-Level-Reliability (WLR) Monitoring for Ensuring High-Quality Manufacturing of Automotive-Grade ASIC Products
L. Sheng, ON Semiconductor

The rigid trend in semiconductor industry towards the “0-ppm” quality virtually requires no any reliability failure after delivering millions or even billions of parts, especially for those used in potentially life-threatening automotive applications. During a manufacturing lifespan up to several decades, the reliability of a qualified process inevitably fluctuates or degrades, which may significantly increase costs in handling field returns (RMAs) and impair our reputations as a premier supplier of Application-Specific-Integrated-Circuit (ASIC) products. Therefore, Wafer-Level-Reliability (WLR) monitoring has become a vital approach in highly variable and dynamic wafer-manufacturing environments. Our presentation will start with a brief introduction of the WLR monitor program installed across several sites over a decade. To vividly illustrate its profound incentives to the high-quality wafer-manufacturing, we will provide a case

study with a detailed trend chart intermittently affected with a P-specific gate oxide defectivity (D0) issue in one of our most advanced high-voltage mixed-signal production lines for automotive-grade ASIC products. A skew "bull's-eye" wafer-pattern with a good zone in the center of some WLR monitor wafers promptly detected an intricate galvanic corrosion and the problematic tool. Furthermore, the variety of test structures also facilitated the assessment of the D0 noise floor and reliability perspectives.

2.3 Best Known Methods for Latent Reliability Defect Control in 90nm – 14nm Semiconductor Fabs

R. Rathert, KLA-Tencor Corporation

The semiconductor content in automobiles continues to increase, despite already being the highest contributor to field returns. The vast majority of early-life failures point to random defectivity as the primary source of latent reliability defects. This paper will provide an overview of the most common techniques used by automotive fabs to control for latent reliability defects. These approaches generally fall into two categories:

- Baseline defect reduction strategies, which reduce the formation of all defect types (killer and latent defects) for all devices being processed at the fab. These include continuous improvement programs and baseline reduction targets.
- Automotive-specific inspection and metrology strategies. These higher sampling rates, more inspected layers, and the use of supplemental "inline screening" methodologies to identify die which may potentially pass electrical test but have a higher statistical probability for latent reliability defects.

The scope of the presented BKM's will include on-product defect inspections such as Broadband Plasma ("Brightfield"), Laser Scanning ("Darkfield"), E-Beam, and high-speed Macro/edge inspections, in addition to non-product monitor wafer inspections (e.g., "Surfscan" inspections). Fabs which employ these BKM's have demonstrated a superior ability to find latent defect excursions.

2.4 Guardbanding Based On Device Drift Behavior

H. Lewitschnig, Infineon Technologies

Certain electrical parameters of semiconductor devices can drift, i.e. they change their value continuously over time. We investigated such drift behavior at HTOL stress tests and identified several drift patterns. Semiconductors have to fulfill the specification over lifetime. Thus, electrical parameters should stay within the specified range throughout their specified operational lifetime. In order to avoid electrical parameters drifting out of their specified range, the typical countermeasure is to apply guard bands at the final tests of the semiconductor's production. This is test limits are tightened, such that any drift of electrical parameters over lifetime would still stay within the specified range. We investigated several mathematical methods to describe drift patterns. We considered drift data as longitudinal measurement data, based on censored data generated by the stress test. Using multivariate distributions and modeling their dependency structure by copulas, we could calculate optimal guard bands and minimize the probability that devices drift out of the specified range over their operational lifetime. We extended the model by describing the drift as a function of time. This allows us to estimate parameter distributions between HTOL readout times. We can also map drift distributions with usage profiles, which results in a refined model to optimize guard bands and minimize the probability for drifts out of the specified parameter ranges.

This work was supported by the ECSEL Joint Undertaking under grant agreement No. 662133 - Power-Base. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Belgium, Germany, Italy, Netherlands, Norway, Slovakia, Spain and United Kingdom.

Keynote: The Reliability Dilemma

W. Kanert, Infineon Technologies

The presentation takes a look at reliability from a general perspective, or meta-level, not intending to give an in-depth discussion of specific technical topics. The reliability dilemma arises from the conflict between the objective of reliability engineering and the forces acting counter to this objective, which are both

technical and economic in nature. It focuses on difficulties encountered with prediction of reliability, which is the ultimate objective of our endeavour. It also takes a glimpse at more fundamental issues that rarely receive consideration in discussions of reliability topics.

3.1 An IC Supplier Implementation of Automotive EIPD Customer Resolution Process

A. Righter, Analog Devices

The recent efforts of the USCAR Initiative group to define a process for OEM, Tier 1 and Supplier automotive customer resolution of EIPD (Electrically Induced Physical Damage) issues in components has become a major focus of automotive reliability. This presentation describes one supplier's approach of implementing the resolution process and in particular the communication among the various support stakeholders. Additionally it provides examples of automotive EIPD case studies addressed successfully using the process. It is emphasized that the best method of reducing EIPD effects is for all involved to collaborate together in order to quickly identify the source, replicate the conditions that created the damage whenever possible, and determine effective corrective actions to prevent future such damage.

3.2 A Hybrid Methodology for Fault Grading A Low-Medium Density FPGA

R. Sood, Lattice Semiconductor

Field Programmable Gate Array (FPGA) integrated circuits present unique challenges for fault grading due to their ability to be reprogrammed multiple times. Fault grading has to comprehend multiple test configurations to give an accurate account of test coverage. Many of the IP blocks under test within the FPGA are custom-designed outside of an RTL flow, so Automatic Test Pattern Generation (ATPG) is not always an option. As a result, directed functional tests need to be architected and fault graded for these custom blocks. Configuring the FPGA multiple times incurs a time cost for fault grade computation and manufacturing test. The computation time makes it impossible to fault grade on a full chip, and thus it is run on representative individual circuit and IP blocks and scaled up to full chip. Another challenge for determining fault coverage and forecasting outgoing quality (Defects Per Million or DPM) is caused by the low utilization of programmable cells for any single configuration. As a result of these factors, a hybrid methodology has been developed that allows multiple fault coverage metrics to be applied to the FPGA to guarantee test coverage and product quality in a manner that correlates with DPM targets and automotive requirements.

3.3 A Possible Latch-up Concern Induced by Active Layer Particles During FAB Process

T. Chien, ISSI

Latch-up is defined as the creation of an unintentional, low impedance path between power supply and ground in bulk CMOS integrated circuits (ICs). When an N-MOS is in close proximity to a p-MOS, the coupling of the NPN and PNP parasitic bipolar transistors can cause the triggering of the parasitic PNPN (or NPNPN) SCR structure. The latch-up in an IC can be destructive if the current is not restricted, hence it should be avoided at all costs. The activation of a parasitic SCR can be initiated by sources such as hot carriers, ground bounces, transmission line reflections, signal mismatching at the outputs of the circuits, etc. This kind of latch-up is characterized as internal latch-up [1]. In this paper, a new latch-up source that is found due to a particle issue on the active layer which is also able to activate the parasitic SCR will be discussed. In high density SRAM, the cell layout is so dense that even a small particle dropped on the memory array may reduce product yield; therefore, the redundancy circuit is indispensable. However, a repaired circuit could result in product malfunction in the field after a certain period of service. In this study, it was found that an active layer particle could activate the parasitic SCR to cause leakage even after repair of the redundancy circuit. This is a potential problem for customer's use in the field. It is highly recommended that the supplier should not do any redundancy repair but to dispose of the IC as bad die to reduce potential defectives.

[1] R.R. Troutman – IBM Corp. - "Latch-up in CMOS Technology - The problem and Its Cure", Kluwer Academic Publishers, 1986

3.4 IPC Standards Development Efforts for Printed Board Performance and Assembly in Automotive Applications

J. Perry & T. Rowe, IPC

For years, IPC standards provided design requirements and acceptance criteria for bare and assembled printed boards by way of Performance Classes intended to reflect differences in producibility, complexity, functional performance and verification frequencies. It has historically been left to the OEM to determine which IPC Performance Class their products should adhere to. Recently, however, IPC has been developing Addendums to our primary standards that provide requirements to be used in addition to, and in some cases, in place of, those published in existing IPC standards. This began with addressing products used in space flight and military avionics applications. An Addendum to IPC's rigid printed board performance specification for automotive applications was released in 2016. IPC is looking to not only revise the automotive addendum for printed boards but also to develop addendums for our printed board assembly workmanship standards used within the automotive industry. There are currently efforts underway for press-fit pint technology and acceptance of electronic assemblies with additional planned documents based on industry need. IPC is looking to bring in additional fabricators, contract assemblers and OEMs within the automotive industry towards this effort. In addition to a brief overview of IPC and its history, this presentation outlines such efforts and seeks input on the best ways to advance such standards.

4.1 E-Mobility and Autonomous Driving – New Functions, New Requirements To Automotive Electronics

U. Abelein, Infineon Technologies

The field of automotive electronics went through an impressive evolution over the last decades. But the introduction of hybrid and electric drivetrain as well as novel applications like advanced driver assistant systems up to self-driving vehicles lead to really revolutionary changes. The switching to electric mobility establishes new operating conditions for electronics (like charging the battery) and the introduction of new functions accelerates the introduction of new technologies in automotive electronics. Both affect reliability engineering tremendously. Today we are facing mission profile based customer requirements on reliability which by far exceed the coverage of the test conditions described in the AEC-Q100/101. Furthermore the introduction of new technologies introduces new failure modes which might be accelerated in a quite different manner and by a quite different combination of stressors compared to conventional silicon technology failure modes. The talk will briefly discuss the background leading to this change in requirements. It will then give an overview of the trends in reliability requirements from the perspective of an automotive semiconductor supplier. Finally some ideas will be sketched, how to react to these changes as a standardization organization.

4.2 Scan-Based Checksum Generation for High Diagnostic Coverage in Safety-Critical ICs

J. Schat, NXP Semiconductors

For safety-critical devices, ISO 26262 mandates repeated in-situ tests during application, mainly in order to detect alterations of register contents due to Single Event Upsets (SEUs). In ICs which contain a large number of quasi-static registers, a checksum over the registers' contents can be calculated; if the checksum changes between write accesses, this can only be because an SEU has modified a register. The existing scan-test infrastructure can be re-used to shift out the registers contents and feed it to a checksum generator. As this shifting destroys the registers' contents, the scan chain outputs are fed back into the scan chain inputs, such that the scan chains' contents is reconstructed after having read out the complete register chain. This solution is for many ICs a good trade-off between interruption time of the application mode (only some µs), area overhead (much less than 1%) and data transfer volume out of the IC (only the few bytes of the check-sum). Moreover, the solution allows for a very easy calculation of the Diagnostic Coverage, i.e. the percentage of detected SEUs according to the ISO 26262 requirements.

4.3 TRACE (Technology Readiness Process for Consumer Electronics) Enabling for Intelligent Mobility and Intelligent Infrastructure

P. Wurster, Daimler

TRACE is a project funded by the European Union and is attended by semiconductor manufacturers (NXP, STM and ams), OEMs (Volvo, BMW, VW and Daimler), 1. Tiers (e. g. Siemens and Continental) and various universities and institutes. The project intends to develop methods and processes to enable a qualified and secure transfer of leading-edge micro- and nano-electronic technologies from the consumer domain to the automotive and industrial domains.

5.1 Zero Defect Approach for Semiconductors, Used In BMW Vehicles - BMW Requirements

R. Stadler, BMW Group

Although a lot of electronic components have been replaced and moved into more complex semiconductors (e.g. SOC, SIP, new technologies), the demand of semiconductors for BMW vehicles is still growing. On the other hand, the quality requirements on system level have been tightened, e.g. control limit for an average ECU is 10ppm within 24month. Therefore BMW has to ensure that only "automotive capable" semiconductor devices with zero defect approach are used in order to support the challenging system requirements. Consequently BMW Group has developed a semiconductor standard in 2013 (new revision since 2015) which is part of the purchasing contract for each electronic system and has to be applied over the whole supply chain. First, in this workshop BMW will show an overview about dominating semiconductor related failure modes. The database for the overview is derived from several thousand 8D reports, which have been analyzed and structured according to semiconductor relevant failure modes. The so called „Failure Landscape" helps to understand the nature of dominant 0km and field failures. This data set than is partitioned into root cause categories to get a Pareto of why semiconductors are failing in the car in early life time. The knowledge helps to set the focus on important topics and to support an adequate refinement of automotive semiconductors requirements. Second, the heart of the BMW semiconductor requirements, known as „Automotive Puzzle" will be presented. Very important topics of each chapter with significant influence to the quality level will be highlighted. Finally, the need to establish an AEC task for a zero defect guideline should be discussed.

5.2 Knowledge-Based-Qualification: A Winning and Robust Approach for ADAS and Internal/Cockpit Application

I. Hsu, Intel

While traditional qualification approaches for semiconductor industry were established using legacy and standards-based methods (SBQ), first utilized by military sector, advancements in material, processing, and ultimately package technology have shown that those methods alone are inadequate to provide the right formula on reliability test that meets today's customer and applications. Many commercial OEMs have gradually migrated to a Knowledge-Based-Qualification (KBQ) approach that brings a myriad of techniques such as Physics-of-Failure (PoF), Failure Mode Effects Analysis (FMEA), and use-conditions data to develop reliability assessment plans. Additionally, characterization tests have gained popularity to supplant historical stress tests that contained binary outcomes, and both modeling and simulation have been applied to better understand the effect and sensitivity of key properties. This paper will provide an illustration on KBQ application conducted by Intel on thermal cycling risk assessment ADAS application and internal/cockpit BGAs that expand beyond the traditional qualification effort. Through KBQ implementation, the qualification requirements were able to account for package geometry, system requirements (such as the board material properties), as well as the ambient and use conditions environment. Usage of Finite Element Analysis (FEA) modeling to achieve a greater intrinsic understanding of the package technology and its inherent behavior will be shown. Finally, a comparison between KBQ and SBQ will be shared to highlight the potential shortcomings of SBQ that may not truly reconcile the needs of the customer and/or lead to designs that are less economically attractive.

5.3 Handling of Hardware Components in Automotive Functional Safety Spec ISO26262
Dr. V. Tiederle, RELNETyX Consulting UG

The functional safety specification is often used as a requirement for sophisticated automotive electronics to ensure a robust and reliable product. This specification – ISO26262 – is to be updated in the near future. The draft of this version is already existing. In this new version an additional part is created where the handling of semiconductors is described in detail. This updated specification of ISO26262 is also giving some advices how to get valid numbers for the constant failure rate. There are different approaches to cover the reliability prognostics of electronic hardware:

- Constant failure rate – that means random failure
- Increasing failure rate – that means wear out failure

The presentation will give an overview of this new part concept of the automotive specification for the handling of electronic components, especially semiconductors.

W.6 AEC-Q104 Multi-Chip Module (MCM)/Hybrid Qualification Update
Moderator: T. Lawler, Lattice Semiconductor and AEC-Q103 Sub-Committee

6.1 Semiconductor Assembly, Modular and SMT Materials Reliability for Evolving Automotive Electronics Applications
A. Mackie, Indium Corporation

Major changes in the nature, complexity and criticality of electronics in automotive usage are creating new challenges in semiconductor assembly materials and processes in ensuring finished device reliability. This paper will review changes foreseen for the automotive industry, their impact on electronics in automotive, and how materials suppliers are rising to meet these challenges. Topics to be discussed:

- Challenges to materials suppliers developing and testing materials for the automotive semiconductor assembly industry
- High temperature Pb-free solder paste for die-attach in discrete components and modules
- Sintering materials for die-attach for wide-band gap (GaN and SiC) devices
- High reliability SMT solder paste for modules and SMT
- Bondline thickness control in IGBT module die-attach using solder preforms

6.2 Multiple Reflow Test Analysis on Flip Chip BGA Packages for PPM Assessment at Post Assembly Step
T. Dambruoso, STMicroelectronics

The increasing complexity of ASIC pushed the industry to innovative packaging solutions that are very challenging versus high automotive quality targets. This study is based on the risk assessment about a specific low-k crack failure mode that happens during assembly process for advanced Flip Chip BGA packages. Die silicon is submitted to high stress during soldering reflow performed before under fill step; coefficient thermal expansion (CTE) mismatch between Si and organic substrate can easily transfer stresses to the fragile low-k layer causing cracks. This failure mode is clearly visible with Sonoscan technique (CSAM) but, due to localized crack and/or metal line redundancy, screening at ATE is not always 100% effective; thus some impacted devices could be potentially shipped to customer. The stress test selected for failure mechanism activation is the Multiple Reflow Test (MRT); it consists in repeating the solder reflow step several times and checking the occurrence of low-k cracks through CSAM. A new work flow based on combination of MRT, CSAM and ATE data has been defined to perform the ppm extrapolation of post assembled not screened units affected by low-k crack. This methodology is used to perform a more accurate failure rate prediction on Flip Chip products for automotive applications.

6.3 Mechanism to Improve The Reliability of Cu Wire Bonding by Pd-Coating of The Wire

W. Qin, ON Semiconductor

Coating of the Cu bond wire with Pd has been a rather widely accepted method for semiconductor packaging technology to improve the wire bonding reliability. Based on comparison of a Cu bond wire and a Pd-coated Cu bond wire on AlCu pads that had passed HAST, new insight into the mechanism of the reliability improvement is gained. Our analysis showed the dominant Cu-rich intermetallics (IMC) were Cu3Al2 for the Cu wire, and (CuPdx)Al for the Pd-coated wire. The results have verified the Cu-rich IMC being suppressed by the Pd-coating, which has been extensively reported in literature. Binary phase diagrams of Al, Cu, and Pd indicate that the addition of Pd elevates the melting point, bond strength and activation energy for the corrosion of (CuPdx)Al compared with CuAl that formed with the bare Cu wire. The improvements are expected to decrease the kinetics of phase transformation toward the more Cu-rich IMC, and reduce the corrosion rate of (CuPdx)Al. The corrosion resistance of the wire bonding is enhanced and the wire bonding reliability improved. We find that Ni behaves thermodynamically quite similar to Pd in the ternary system of Cu wire bonding, and therefore possesses the potential to similarly improve the corrosion resistance.

6.4 Bond Ball Lift Failure Mode Category - Criteria for Post Stress Assessment of WBP Tests

Dr. M. Blyzniuk, Melexis

ICs bonding reliability at High Temperature (HT) application is considered. Namely results of investigations of bond ball lift failure mode category at post HT stresses Wire Bond Pull (WBP) tests for AlAu intermetallic interface at HT (>150degC) application are presented in submitted paper. Reasons of such kind of investigations are explained by the fact that nowadays demand for qualification of high temperature application products according to severe customers' mission profiles requires performing of extended life tests over specified duration in AEC-Q100 at Tamb garter than specified for Grade 0 part operating temperature. It leads to needs in using and development of additional tests criteria for proper assessment of product reliability, especially to bonding system reliability as major limitation factor. One of such criteria for proper assessment of bonding reliability is pass/fails criteria of post stress WBP tests. Correct assessment of post stress WBP tests results including failure modes became more and more relevant, especially it is related to bond ball lift failure mode after high temperature stress which can be differently interpreted and considered as fail criterion even if it does not lead to significant degradation of pull force (e.g., if it is still in limits of MIL standard), and does not lead to reliability risk. Developed in additional PASS/FAIL criteria for post stress WBP tests like mean value of pull force over three times of minimum individual value according to MIL 883;M.2011, and +/- 20% of stability of mean value of pull force over life time allows to consider bond ball lift category as accepted failure mode. Applying of above mentioned post stress WBP criteria at bond ball lift failure mode category had been used for reliability risk assessment of AlAu intermetallic interface degradation at HT and degradation prediction depending on different groups of factors, namely:

1. Time and Temperature
2. Kind of used Au wires
3. Outcome of bonding parameters settings and its using for prediction of post stress critical bond ball lift category
4. Kind of used mold compound

Matrix of above mentioned factors (taking into account their interactions) with impact on bonding reliability evaluation on the base of critical bond ball lift categories at WBP after HT stress test will be presented. Activation energy of critical bond ball lift categories at certain combinations of factors is defined.

7.1 Procedure for Determining a Package Size Below Which CDM Testing Is Not Required
R. Ashton, ON Semiconductor

Charged Device Model (CDM) is considered the most important device level ESD test to ensure adequate ESD robustness in automated assembly operations. However, difficulties exist with CDM testing of small devices due to the challenge of holding them in place during testing and the very fast pulses created during a CDM event involving a small package. The challenge of testing small devices often appears to be wasted effort, since small devices seldom fail the CDM test. Establishing a device size below which CDM testing can be eliminated is difficult due to the wide range of issues which affect CDM robustness, including technology, design style and the type of ESD protection employed. The joint JEDEC/ESDA CDM working group is developing a procedure for reducing unnecessary testing of small devices. This presentation will review field-induced CDM testing, discuss the issues of CDM testing of small devices and outline the procedure that the joint JEDEC/ESDA CDM working group is developing for CDM standard JS-002. The procedure determines a device to field plate capacitance below which CDM testing may be eliminated for a particular technology, design flow and ESD protection library. Adoption of this small package CDM procedure into Q100-011 is also being discussed.

7.2 A Different Concept for Improvement of Wafer Testing A Memory Device
CC Hung, ISSI

The performance improvement of DRAM products depend highly on fab process. In this study, a different concept is adopted to effectively reduce failures caused by fab process defects. Two specific fab process defects are addressed in this paper. For defect #1 (defective metal-1 lines), some dies with this type of defects receive laser repair during chip probing(CP) test. But these are prone to failure because electrical deterioration may develop around defect area later during field service. In addition to the Fab's effort to reduce defects, a new concept to keep track of special failure patterns on wafer and screening out weak dies without repairing are introduced. Therefore, preventing defect related failures in the first place. Another fab process defect (a pattern-missing defect on contact or metal-0 layer) was also studied. Again, it is found that the defect would show a special failure pattern during wafer testing. With this same approach, the defect rate of DRAM product was reduced successfully. We recommend to adopt this new concept in parallel with the Fab's effort on defect reduction to fabricate high quality, low ppm memory products.

7.3 AEC-Q100 and Q101 Implementation / Procedure Using the New JS-002 CDM Platform: A Document Overview
A. Righter, Analog Devices

The AEC ESD-CDM Subteam has been tasked with creating revision drafts of the AEC Q100-011 and Q101-005 CDM standard documents for integrated circuits and discrete devices, respectively. These documents will incorporate ANSI/ESDA/JEDEC JS-002 as the AEC's new CDM ESD reference test platform, replacing the Q100-011 method that was adopted from the ESDA S5.3.1 CDM standard (obsoleted). Compared to this previously referenced ESDA CDM standard, the new JS-002 standard has improved calibration methodology, hardware/metrology specifications, and a greater range of test condition stress levels described in waveform parameters (corresponding to test condition classification levels). This presentation provides a look into proposed AEC implementation and CDM test conditions for automotive Integrated Circuits (IC) and discrete devices, reviewing Q100-011 draft proposed sections. AEC harmonization using JS-002 will streamline supplier CDM testing into one tester platform, one standard method and help to ease the transition of commercial components to automotive applications.

W.7 AEC-Q100 Document Status & New AEC Initiatives
Moderator: AEC Q100 Technical Committee